Hot-carrier-induced on-resistance degradation of step gate oxide NLDMOS*

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Abstract: The hot-carrier-induced on-resistance degradations of step gate oxide NLDMOS (SG-NLDMOS) transistors are investigated in detail by a DC voltage stress experiment, a TCAD simulation and a charge pumping test. For different stress conditions, degradation behaviors of SG-NLDMOS transistors are analyzed and degradation mechanisms are presented. Then the effect of various doses of n-type drain drift (NDD) region implant on R_{on} degradation is investigated. Experimental results show that a lower NDD dosage can reduce the hot-carrier induced R_{on} degradation effectively, which is different from uniform gate oxide NLDMOS (UG-NLDMOS) transistors.

Key words: SG-NLDMOS; R_{on} degradation; charge-pumping; interface state; positive oxide-trapped charge
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1. Introduction

NLDMOS transistors have been widely used in power management IC (PMIC), owing to the low on-resistance R_{on}, high breakdown voltage, and flexibility in being easily integrated into standard low-voltage CMOS processes. When the NLDMOS transistor is applied in switching applications, hot carrier injection may occur because of the high electric field near the drain and source, which may gradually "wear out" the device. Thus, the hot-carrier reliability of LDMOS devices has attracted wide attention.

The hot carrier effect of uniform gate oxide NLDMOS (UG-NLDMOS) transistors has been widely researched[1, 2]. However, the hot carrier effect of step gate oxide NLDMOS (SG-NLDMOS) transistors is less well documented. This paper mainly researches the degradation behaviors and mechanisms of SG-NLDMOS transistors under different stress conditions. In addition, improved methods to reduce the R_{on} degradation are also presented.

2. Device description

Figure 1 shows the cross-section of a SG-NLDMOS transistor. The device is processed by a 0.35 μm CMOS compatible BCD technology. The gate oxide thickness is 70 Å. Different from UG-NLDMOS, the oxide thickness over the drift region is thicker than the gate oxide. This region is called thick oxide overlapped drift region ('to' for short), and the thick oxide thickness is about 500–800 Å. The operational voltages of the device are 20 V for drain (V_d) and 3.3 V for gate (V_g), respectively. The device has a threshold voltage of 0.7 V and an off-state avalanche breakdown voltage of 30 V. The other details of the structure can be seen in Table 1.

3. DC voltage stress experiment

As a power transistor, R_{on} is the prime parameter. Figure 2 shows the R_{on} degradation of the SG-NLDMOS under different stress conditions. When V_{gs} is fixed at 1.7 V, we could observe that the R_{on} degradation at V_{ds} = 28 V is worse than V_{ds} = 26 V. It is interesting to note that the degradation is negative, i.e. the R_{on} decreases at the early stress stage when the stress time increases at V_{gs} = 1.7 V, V_{ds} = 28 V. And it is clear that the R_{on} degradation curve is power law in nature with increasing stress time, and the slope rate of the device under V_{gs} = 1.7 V is larger than that under V_{gs} = 3.3 V. Thus, the medium V_{gs} stress condition corresponds to the worst stress condition that leads to the largest degradation. Figure 3 shows the V_{th} degradation of SG-NLDMOS under different stress conditions. However, a small shift in V_{th} is measured and can be neglected. Thus, the R_{on} degradation is independent of the V_{th} shift.

4. TCAD simulation

In order to understand Fig. 2 and identify the physical mechanism responsible for the R_{on} degradation, detailed 2-D TCAD simulations are performed. Figure 4 shows the simulated impact ionization (ii) rate along the Si/SiO_2 interface when the device is biased at V_{gs} = 1.7 V, V_{ds} = 26 V and V_{gs} = 3.3 V, V_{ds} = 26 V, respectively. For V_{gs} = 1.7 V, the ii rate peak value at the junction of accumulation region and thick oxide region increases, the other ii rate peak value at the junction of thick oxide and spacer regions decreases, both of which generate a mass of hot carriers. And for V_{gs} = 3.3 V, the ii rate near

Table 1. Detailed structure of the proposed device.

Item	Full name
NLDD	N-type lightly doped drain
Ndd	N-type drain drift region
HVNW	High voltage n-type well
ch	Channel region
acc	Accumulation region
to	Thick oxide overlapped drift region
spacer	Spacer region
drift	N-type drift region

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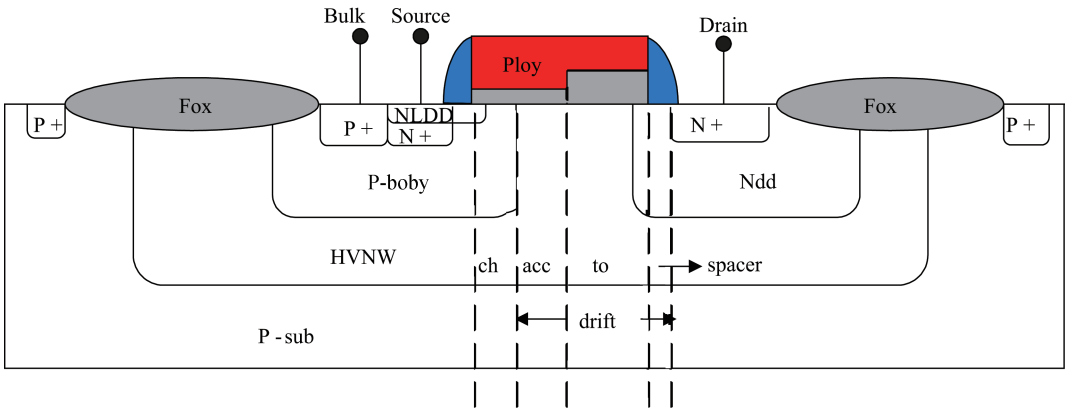

Fig. 1. Schematic cross-section of the SG-NLDMOS.

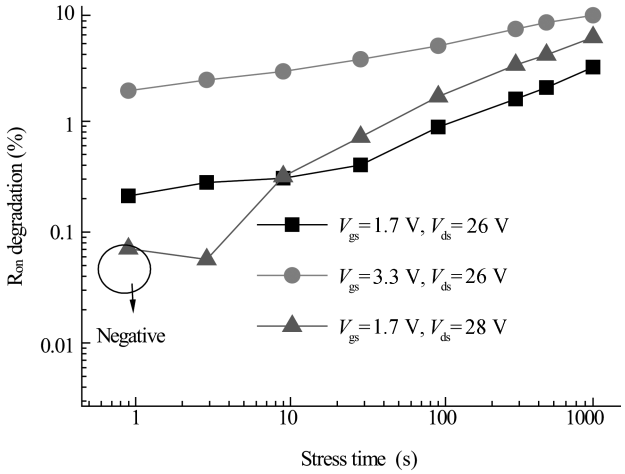

Fig. 2. R_{on} degradation of the SG-NLDMOS under different stress conditions.

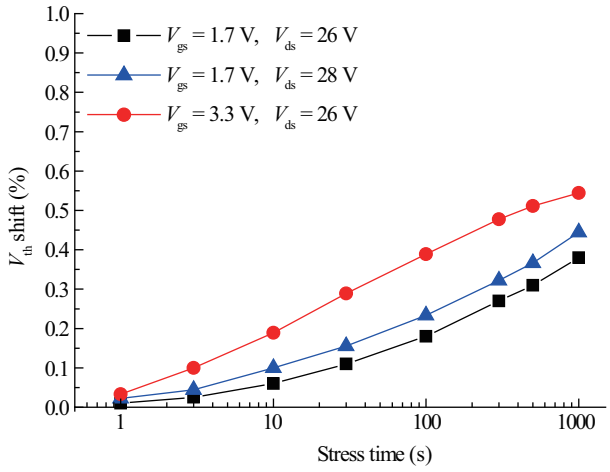

Fig. 3. V_{th} degradation of the SG-NLDMOS under different stress conditions.

the source decreases, and the ii rate near the drain increases. This phenomenon can be explained by the Kirk effect. Because current increases with increasing V_{gs}, so the electric field peak

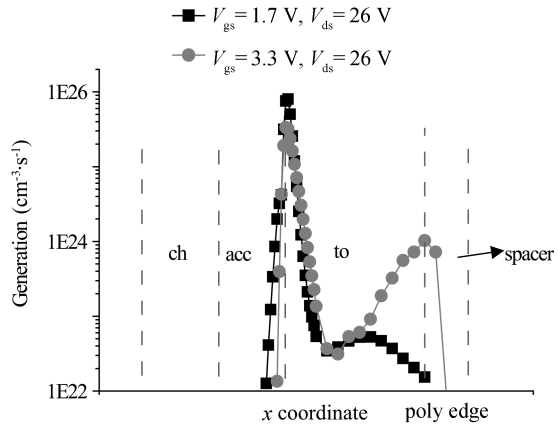

Fig. 4. Simulated ii rate along the Si/SiO_2 interface when the device is biased at V_{gs} = 1.7 V, V_{ds} = 26 V and V_{gs} = 3.3 V, V_{ds} = 26 V, respectively.

shifts toward the drain, leading to the increase in the ii rate near the drain[3].

Generally speaking, interface states are generated in the high impact ionization rate region. Thus, interface states generation may happen in the whole drift region.

Figure 5 shows the simulated electric fields along the Si/SiO_2 interface perpendicular to the interface for SG-NLDMOS at V_{gs} = 1.7 V, V_{ds} = 26 V and V_{gs} = 3.3 V, V_{ds} = 26 V, respectively. The electric field is positive in the channel region and negative in the drift region. For V_{gs} = 1.7 V, two electric field peak values exist in the drift region. The one peak value exists at the junction of the accumulation region and the thick oxide region, and the other exists at the edge of the polysilicon near the spacer region, which are favorable for hole injection. The injection of hot holes may result in positive oxide-trapped charges, or interface state generation. But for V_{gs} = 3.3 V, the electric field at the accumulation region decreases significantly, which is induced by the Kirk effect.

5. Charge pumping test

In order to gain more detailed information about the R_{on} degradation mechanism and determine the Si–SiO_2 interface state density directly, a charge pumping (CP) test is per-

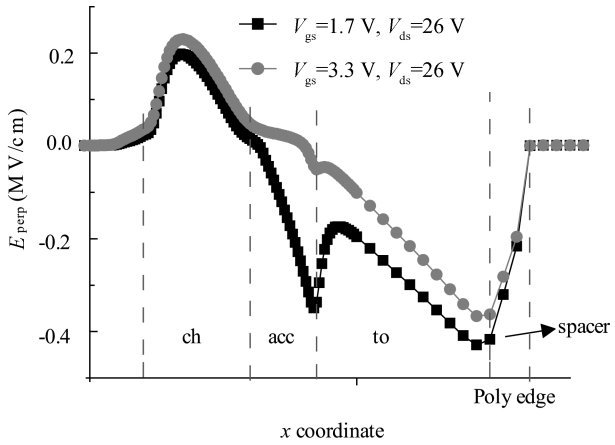

Fig. 5. Simulated electric fields along the Si/SiO_2 interface perpendicular to the interface for SG-NLDMOS at V_{gs} = 1.7 V, V_{ds} = 26 V and V_{gs} = 3.3 V, V_{ds} = 26 V, respectively.

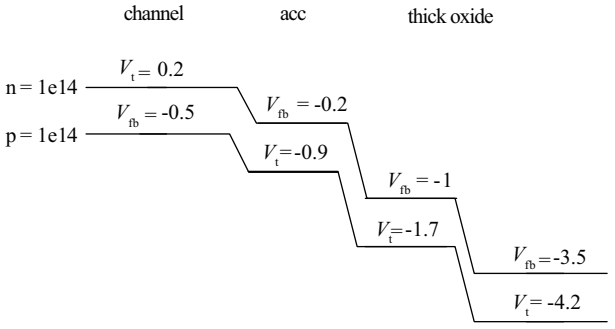

Fig. 6. Simulated values of V_t and V_{fb} along the Si/SiO_2 interface for SG-NLDMOS.

formed[4]. The CP current is measured at the body contact while pulsing the gate and grounding the source and drain. The pulse base level is varied from –4 to 0.5 V, with the pulse amplitude fixed at 1.5 V and the frequency at 5 MHz. The rise and fall times of the pulse train are 0.1 μs. As shown in Fig. 1, the polysilicon gate extends over the channel region, accumulation region and thick oxide region, so all three regions contribute to the CP current.

Figure 6 shows the simulated values of V_t and V_{fb} along the Si/SiO_2 interface. For the channel region, the threshold voltage V_t is defined as the voltage at which the electron concentration of the surface reaches 1×10^{14} cm^{-3}; the flat band voltage V_{fb} is defined as the voltage at which the hole concentration of the surface reaches 1×10^{14} cm^{-3}. For the drift region, V_t is defined as the voltage at which the hole concentration of the surface reaches 1×10^{14} cm^{-3}; V_{fb} is defined as the voltage at which the electron concentration of the surface reaches 1×10^{14} cm^{-3}[5].

Through the simulating values of V_t and V_{fb} along the Si/SiO_2 interface, the values of the pulse base level that can generate CP current in different regions can be concluded as:

Channel region: from −1.3 to −0.5 V;

Accumulation region: from −1.7 to −0.9 V;

The front end of thick oxide region: from −2.5 to −1.7 V;

The back end of thick oxide region: from −5.0 to −4.2 V.

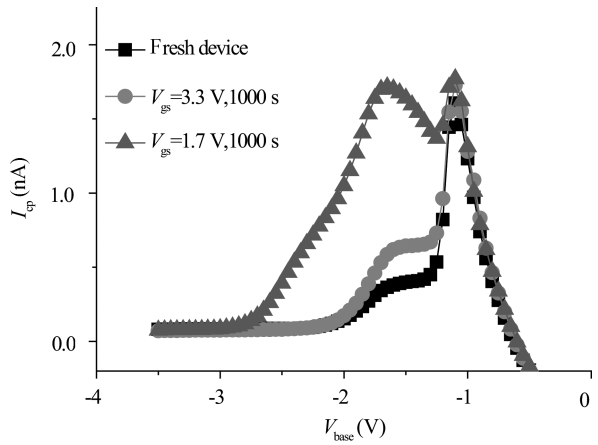

Fig. 7. I_{cp} data measured for the fresh device and devices stress at V_{gs} = 1.7 V, V_{ds} = 26 V and V_{gs} = 3.3 V, V_{ds} = 26 V for 1000 s.

In order to prevent the avalanche breakdown between the gate and the source, the pulse base level cannot be less than −4 V.

Figure 7 shows the CP curves measured for the fresh device and devices stress at V_{gs} = 1.7 V, V_{ds} = 26 V and V_{gs} = 3.3 V, V_{ds} = 26 V for 1000 s. It is clear that the CP curves of the channel region don't vary much. Thus little damage occurs in the channel region. For V_{gs} = 3.3 V, the amplitude of the CP curve in the accumulation region increases, which demonstrates the generation of the interface state[6]. And the lateral movement of the CP curve at the rising edge is negligible, so the interface state is of the acceptor type. In addition, the effect of positive oxide-trapped charge in the accumulation region is not significant. For V_{gs} = 1.7 V, the amplitude of the CP curve in the accumulation region increases significantly, and the whole curve shifts to the left, which demonstrates the generation of interface state and positive oxide-trapped charge. Moreover, the enhancement of interface state damage in the front end of the thick oxide region is also proved by the increase of the CP curve. Although the pulse base level cannot be less than −4 V, it can be concluded that there must exist another degradation region near the drain affected by the Kirk effect.

6. Discussion

Through the DC voltage stress experiment, TCAD simulation and charge pumping test, we can find that different mechanisms dominate the degradation of SG-NLDMOS under different gate voltage stress conditions.

6.1. Medium V_{gs} stress condition

There are two competing degradation mechanisms. (1) Generation of positive oxide-trapped charge in the accumulation region. A reduction in R_{on} is observed at the beginning of stress, which demonstrates the severe effect of positive oxide-trapped charge directly. Because trapping of holes in oxide induces negative mirror charges at the Si/SiO_2 interface in the drift region, resulting in an effective increase in drift region concentration. As a result, R_{on} decreases[7]. (2) Formation of interface state in the accumulation region and the front end of thick oxide region. For long stress times, the generation of in-

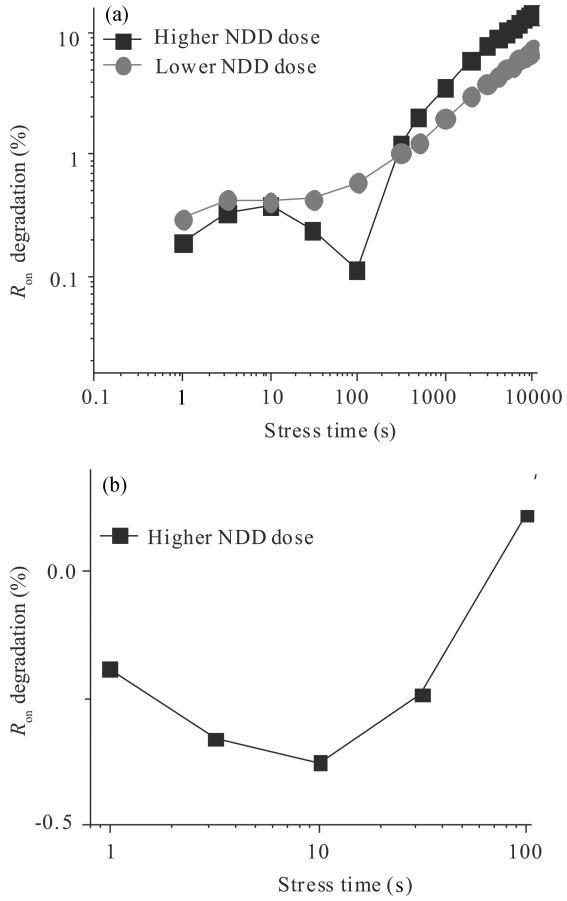

Fig. 8. (a) Effect of various NDD dosage on R_{on} degradation (V_{gs} = 1.7 V, V_{ds} = 26 V). (b) Effect of higher NDD dosage on R_{on} degradation before 100 s.

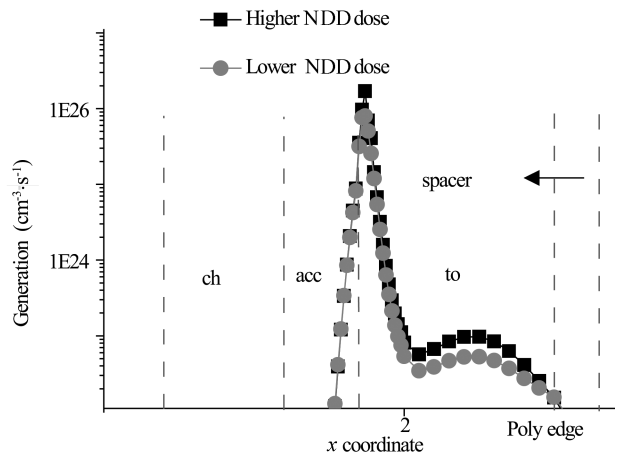

Fig. 9. Effect of various NDD dosages on the simulated ii rate along the Si/SiO_2 interface (V_{gs} = 1.7 V, V_{ds} = 26 V).

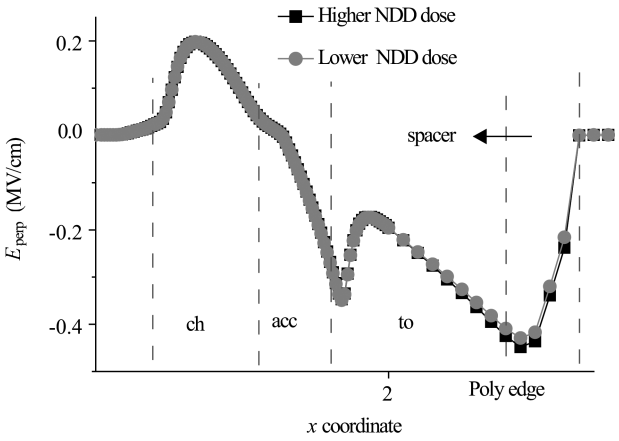

Fig. 10. Effect of various NDD dosages on the simulated electric fields along the Si/SiO_2 interface perpendicular to the interface (V_{gs} = 1.7 V, V_{ds} = 26 V).

terface state dominates the degradation. R_{on} increases because of mobility degradation.

6.2. High V_{gs} stress condition

(1) Formation of interface state in the accumulation region. The CP test results show that the amplitude of CP curve in the accumulation region increases. (2) Formation of interface state and generation of positive oxide-trapped charge in the spacer region near drain. This mechanism has not been proved by CP test. But we can conclude the existence of it from DC voltage stress experiment and TCAD simulation results reasonably.

7. Improved method and discussion

From the above measurement and discussion results, it can be determined that the medium V_{gs} stress condition corresponds to the worst stress condition. Then SG-NLDMOS device with various dosages of n-type drain drift (NDD) region implant are investigated, which are stressed under the medium V_{gs} stress condition.

Figure 8 shows the effect of various NDD dosage on R_{on} degradation when the device is biased at V_{gs} = 1.7 V, V_{ds} = 26 V. Higher dosage is twice the lower dosage. For the device with higher NDD dosage, it can be observed that the degradation is negative i.e. the R_{on} decreases at the early stress stage when the stress time increases. But after 100 s, it is surprised to find that higher NDD dosage leads to much more R_{on} degradation than lower dosage. This phenomenon is different from UG-NLDMOS[8].

Figure 9 shows the effect of various NDD dosage on the simulated ii rate along the Si/SiO_2 interface when the device is biased at V_{gs} = 1.7 V, V_{ds} = 26 V. And Figure 10 shows the effect of various NDD dosage on the simulated electric fields along the Si/SiO_2 interface perpendicular to the interface for SG-NLDMOS at V_{gs} = 1.7 V, V_{ds} = 26 V. It can be seen from the figures that higher NDD dosage leads to higher ii rate in the accumulation region and higher perpendicular electric field at the edge of polysilicon near spacer region.

From the TCAD simulation results, we can see that the step gate oxide structure introduces two electric field peak values in the drift region. High NDD dosage and low V_{gs} will cause the high electric field to shift from drain to source, leading to the increasing of ii rate in the accumulation region. The accumulation region is the mainly degradation region, thus the hot carrier effect increase. At the beginning of stress, the effect of positive oxide-trapped charge dominates the degradation. But then the effect of interface state is more severe than positive oxide-trapped charge, so R_{on} increases. Thus, for SG-

NLDMOS, higher NDD dosage produces much more degradation. In other words, lower NDD dosage can reduce R_{on} degradation.

In addition, increasing the NDD length is also effective for improving the hot-carrier reliability.

8. Conclusion

In this paper, a DC voltage stress experiment, a TCAD simulation and a charge pumping test are used to analyze the hot-carrier-induced R_{on} degradation mechanism of SG-NLDMOS. Research results have shown that the degradation of the device under medium gate voltage stress conditions mainly occurs in the accumulation region, positive oxide-trapped charge and interface state dominate it. For a device under high gate voltage stress conditions, the degradation mainly occurs in the spacer region, the formation of interface state dominates it. But little degradation occurs in the channel region. Improved methods to reduce the R_{on} degradation are presented. Lower n-type drain drift region implant dosage and longer drift-region length can improve the hot-carrier reliability of SG-NLDMOS transistor effectively. Finally, the results of the DC voltage stress experiment, the TCAD simulation and the charge pumping test are consistent with theoretical analysis.

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