A low noise CMOS RF front-end for UWB 6–9 GHz applications*

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Abstract: An integrated fully differential ultra-wideband CMOS RF front-end for 6-9 GHz is presented. A resistive feedback low noise amplifier and a gain controllable IQ merged folded quadrature mixer are integrated as the RF front-end. The ESD protected chip is fabricated in a TSMC 0.13 μm RF CMOS process and achieves a maximum voltage gain of 23–26 dB and a minimum voltage gain of 16–19 dB, an averaged total noise figure of 3.3–4.6 dB while operating in the high gain mode and an in-band IIP3 of –12.6 dBm while in the low gain mode. This RF front-end consumes 17 mA from a 1.2 V supply voltage.

Key words: CMOS; ultra-wideband; resistive feedback low noise amplifier; folded quadrature mixer; noise figure; linearity

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1. Introduction

With the development of technology for high speed wireless communications, ultra-wideband (UWB) technology with high data rates and low power becomes more and more attractive and is regarded as a new pioneer technology for future work. The FCC has allocated an exceptionally large spectrum of 3.1–10.6 GHz for the unlicensed use of UWB devices[1]. Compared to the FCC in USA, the regulatory bodies in Europe decided on more stringent emission masks and specific restrictions in band group 1 (3–5 GHz); the frequency range with an unrestricted maximum mean equivalent isotropic radiated power density of –41.3 dBm/MHz is from 6 to 8.5 GHz only, mapping to WiMedia band group 3. Meanwhile in Japan and Korea, only band group 6 (7–9 GHz) is released without restriction. In addition, China's standard for the UWB spectrum whose band group 2 is 6–9 GHz will be allocated soon. Thus, for UWB systems with worldwide interoperability, the frequency range of 6–9 GHz is of most interest.

In this paper, the requirements and architecture of the RF front-end are analyzed, the design of LNA and mixer is described, and the experimental results and conclusions are presented.

2. Specifications

In consideration of the power consumption and convenience of single-chip integration, a direct-conversion architecture receiver is usually adopted, as shown in Fig. 1. This paper will focus on the design and implementation of the RF front-end block.

From the Friis formula, the noise figure of the RF front-end will dominate the SNR of the receiver. A moderate conversion gain should be assigned to the RF front-end block in order to suppress the noise contributions from the cascading blocks in the receiver. Good input matching of the RF front-end block is absolutely necessary for maximum power transfer from antenna. Linearity in the RF front-end block is not so critical as that in analog baseband processing. Based on the analysis above, the specifications of the RF front-end are listed in Table 1.

3. RF front-end design

3.1. Low noise amplifier

Figure 2 shows the proposed schematic of the LNA, which employs resistive shunt feedback architecture[2−4]. The bonding wire inductance L_{bonding} and ESD capacitance, together

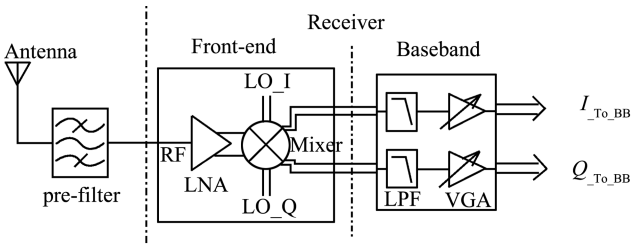

Fig. 1. Direct-conversion architecture of UWB receiver.

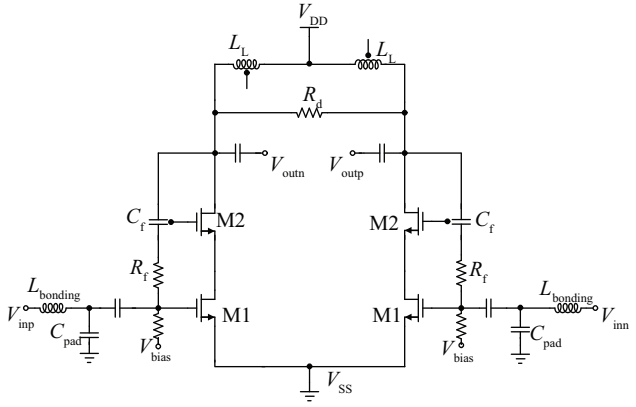

Fig. 2. The proposed resistive shunt feedback LNA.

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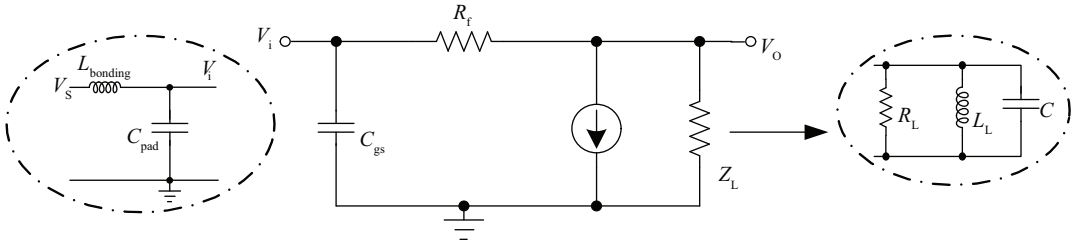


Fig. 3. Small-signal equivalent circuit at the input.

Table 1. Major specifications of the RF front-end.

Parameter	Specification
RF frequency (GHz)	6–9
IF frequency (MHz)	1–264
Noise figure (dB)	< 4.5
Input matching (dB)	< –10
Conversion gain (dB)	25±1.5
In band IIP3 (dBm)	–15

with the PAD capacitance C_{pad}, are co-designed with other on-chip components. The load stage is an R–L–C tank. The load inductor L_L can be replaced by a differential inductor to get a smaller area. However, we split it into two symmetrical inductors for the convenience of cascading with the mixer in the layout.

As illustrated in Fig. 3, let us neglect the bonding wire induction $L_{bonding}$ and the PAD capacitance C_{pad} first and simplify the load R–L–C tank as Z_L. We may get the input impedance as

$$Z_{in} = \frac{R_f + Z_L}{1 + g_m Z_L} // \frac{1}{sC_{gs}} = \frac{Z_L + R_f}{1 + g_m Z_L + (Z_L + R_f)C_{gs}s}. \tag{1}$$

Equation (1) reveals that input impedance is dominated by the feedback resistor, the load network and the transconductance of M1 in the low frequency in the way of $Z_{in} = (R_f + Z_L)/(1 + g_m Z_L)$. As the frequency increases, the parasitic capacitance C_{gs} will play a dominant role in Eq. (1), which will decrease the real part of Z_{in} and make input matching more difficult. If we replace Z_L in Eq. (1) with a real R–L–C tank, that is, $(sR_L L)/(s^2 R_L LC + sL + R_L)$, the input impedance will be depicted as Eq. (2), where C represents the parasitical capacitance at the output port, including the subsequent mixers' gate-to-source capacitance. Equation (2) shows that the load $R-L-C$ tank introduces two zeroes, which could reduce the impact of C_{gs} and make input matching better. By carefully adjusting the value of the resistor and the inductor, we may get good input matching with two resonate points.

$$\begin{aligned} Z_{in} &= \left[R_L Ls/(s^2 R_L LC + Ls + R_L) + R_f\right] \\ &\quad \times \left\{1 + g_m R_L Ls/(s^2 R_L LC + Ls + R_L) \right. \\ &\quad \left. + [(R_L Ls)/s^2 R_L LC + Ls + R_L + R_f]C_{gs}s\right\}^{-1} \\ &= \left[s^2 R_L R_f LC + s(R_L + R_f)L + R_L R_f\right]\left[s^3 R_L R_f LC_{gs}C \right. \\ &\quad + s^2(R_L LC + R_L LC_{gs} + R_f LC_{gs}) + s(L + g_m R_L L \\ &\quad \left. + R_L R_f C_{gs}) + R_L\right]^{-1}. \end{aligned} \tag{2}$$

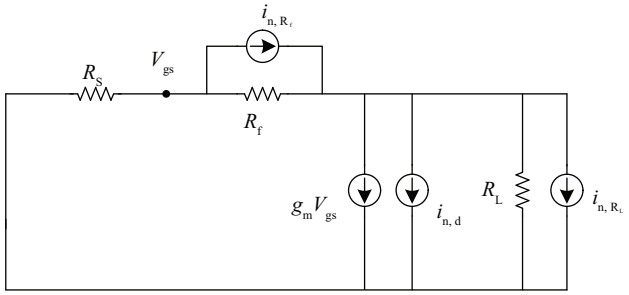


Fig. 4. Small-signal equivalent circuit for noise source.

Using a small-signal model for each noise source, as shown in Fig. 4, the noise factor can be represented as Eq. (3). The first part in the numerator represents the contribution of the channel noise of M1, the second is due to the feedback resistor's thermal noise and the last part is for the resistor in the load network. Increase the transconductance of M1 and the value of the two resistors can reduce the noise figure significantly, as Figure 5 shows. However, we should also pay attention to balancing the input matching and bandwidth. A large transconductance of M1 will introduce large capacitance, and this will deteriorate the input matching, the large resistor will enlarge the Q factor and this will limit the bandwidth. With careful consideration of the design tradeoff among the noise figure, input matching and power gain, we finally implement a LNA for 6–9 GHz with a fairly low noise figure as 2.4–2.9 dB, and moderate power gain and input matching.

$$\begin{aligned} \mathrm{NF} &= 1 + \frac{V_{n,tot}^2}{A_{V,S}^2 \times 4kTR_S} \\ &= 1 + \frac{(R_S + R_f)^2 \gamma g_m + (1 + g_m R_S)^2 R_f + (R_S + R_f)^2/R_L}{(1 - g_m R_f)^2 R_S}. \end{aligned} \tag{3}$$

3.2. Gain controllable IQ merged folded quadrature mixer

Figure 6 shows the proposed gain controllable IQ merged folded quadrature mixer. The folded topology offers a key advantage over traditional Gilbert Cell topology on the voltage headroom. The purpose of exploring merged architecture for the quadrature mixer is to minimize the capacitive load on the LNA[5]. As the requirement described in "system design", the variable gain control should be available in the front-end part in order to handle a large range of signal amplitude. Transistor M3 is designed to achieve a variable gain. While the port V_b is

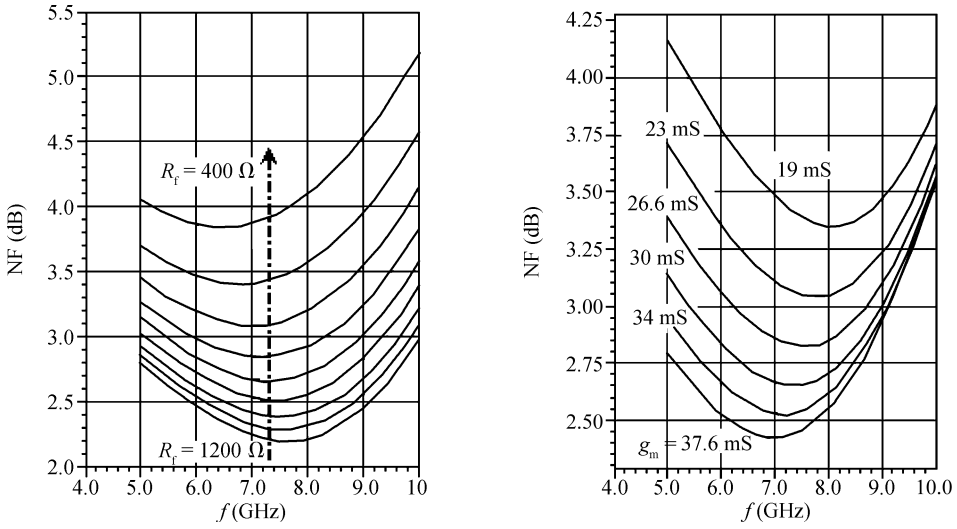


Fig. 5. Influence of R_f and g_m on the NF.

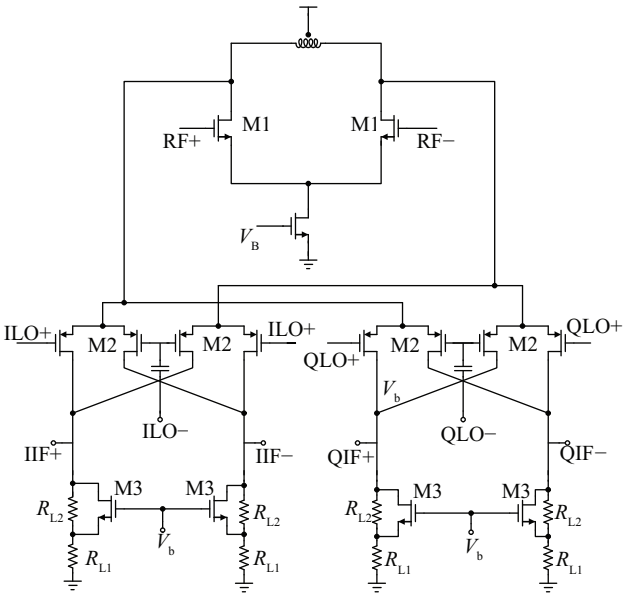


Fig. 6. The proposed gain controllable IQ merged folded quadrature mixer.

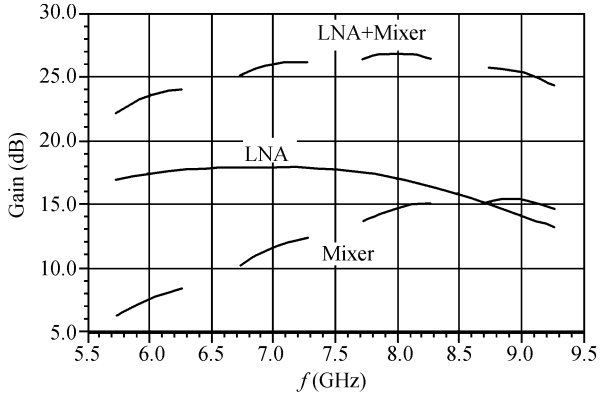


Fig. 7. Co-design of the gain of the LNA and the mixer (high gain mode).

set to be at a low voltage level, M3 is shut down and the load resistor for the mixer is $R_{L1} + R_{L2}$, which is obviously high gain mode. In contrast, if the port V_b is set to a high voltage level, M3 will be turned on and the load resistor R_{L2} will be paralleled by r_o of M3, which is very small, and the load resistor will be approximate as R_{L1}, which is now low gain mode.

The output-referred noise of the quadrature mixer is mainly contributed by the channel noise of M1 and the load resistor's thermal noise. With similar conversion gain and linearity to a pair of Gilbert mixers, the proposed mixer can be designed to have a noise advantage over a pair of Gilbert mixers by proper relative sizing of the mixer core and the transconductor transistors[5].

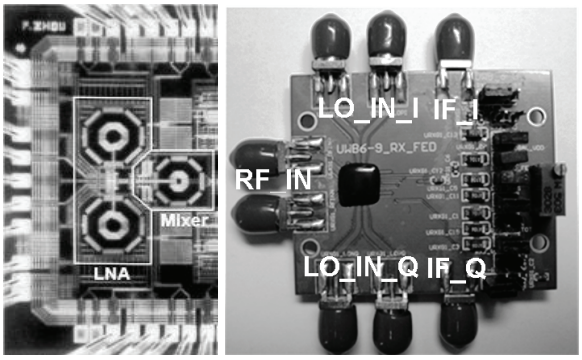
This proposed mixer is optimized to provide a 5 dB conversion gain and 3 dBm IIP3 in the low gain mode, with a 10 dB conversion gain and a 10 dB noise figure in the high gain mode.

As to the co-designing of the LNA and mixer, we mainly focused on the voltage gain of the front-end. As depicted above, we used inductors to resonate with the parasitic capacitance, both in the LNA and in the mixer. However, if we made the resonant frequency of both the LNA and the mixer at the centre of the frequency band that we are interested in, the gain flatness might not meet our requirements. In this work, we made the resonant frequencies of the LNA and the mixer at the low and high frequency bands, respectively, and this led to a good gain flatness for the whole band within 3 dB, as Figure 7 shows.

4. Experimental results

The proposed RF front-end for the MB-OFDM UWB application is fabricated by a TSMC 0.13 μm 1P8M RF CMOS process. Figure 8(a) shows the die photograph. The total die area with pads is 0.82×1.42 mm^2. The chip is directly bonded onto a PCB test board, as shown in Fig. 8(b).

Figure 9 illustrates the experimental results of the input return loss (S_{11}) at the RF input port, which is lower than –10 dB over the frequency range of 6–9 GHz. Figure 10 shows the



(a) (b)

Fig. 8. (a) Die photography. (b) PCB test board.

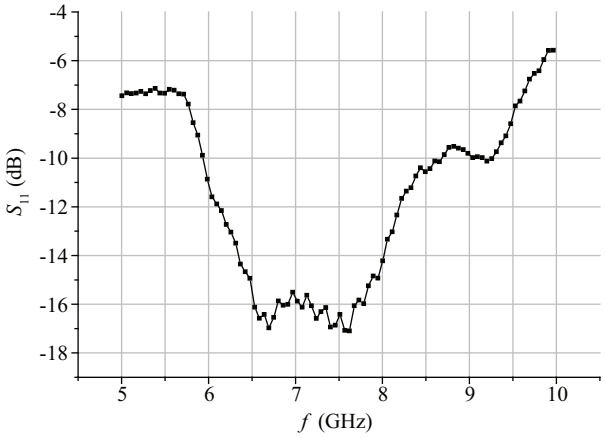


Fig. 9. Measured S_{11} versus frequency.

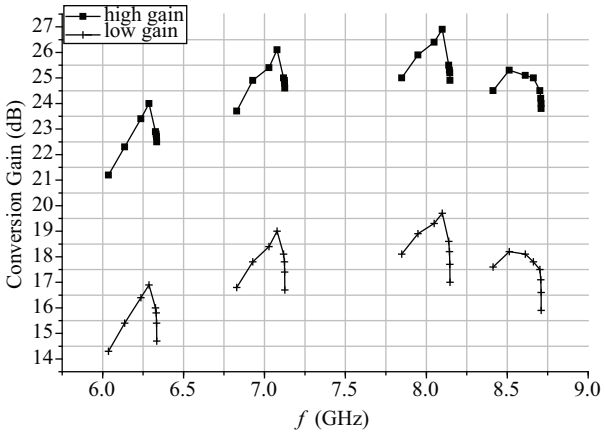


Fig. 10. Measured CG versus frequency.

measured conversion gain versus the frequency at both high gain and low gain modes. The average high gain is 23–26 dB and the average low gain is 16–19 dB, which is 1 dB lower than that of the simulations in both cases. However, $\pm$1.5 dB gain ripple occurs in both high and low gain mode due to the loading effect of the cascading stage LPF and the parasitic capacitance of the AC capacitance between the mixer and the LPF. This capacitance is nearly 500 fF, which deteriorates the IF bandwidth greatly and the conversion gain of the mixer a little.

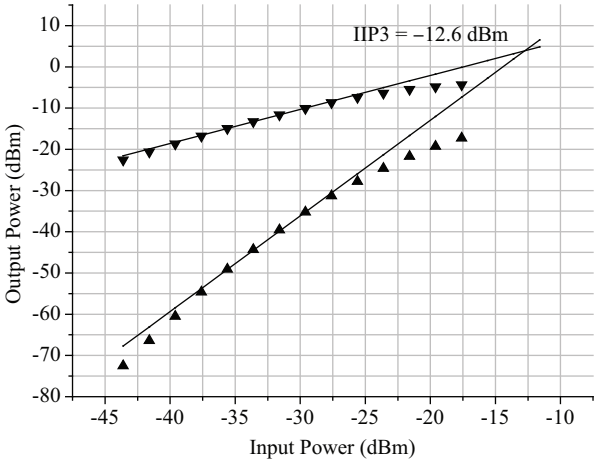


Fig. 11. Measured in-band IIP3.

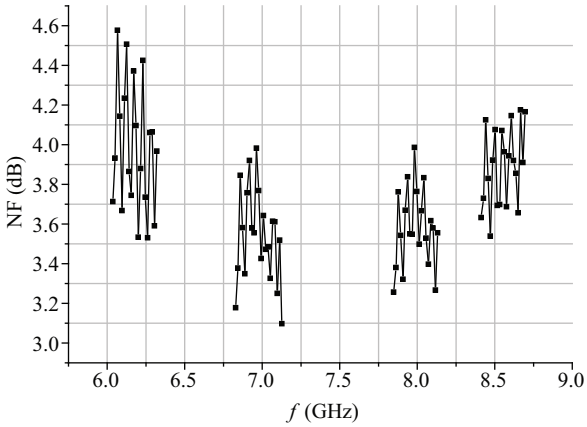


Fig. 12. Measured NF versus frequency.

Figure 11 shows the measurement result of in-band IIP3 at low gain mode at 8.148 GHz by applying the two-tone intermodulation test. The result is –12.6 dBm. Figure 12 reveals the measured noise figure versus the frequency. It achieves 3.3–4.6 dB within the 6–9 GHz frequency band while working in the high gain mode. However, the noise in each 300 MHz band is not very flat, as shown in Fig. 12. The reason for this may be the uneven conversion gain in each IF frequency band. However, this noise figure is still more competitive than in the recent reported works.

With a 1.2 V voltage supply, this RF front-end consumes 17 mA current. Table 2 presents a performance comparison with the recently reported RF front-end for wideband applications. Comparison shows that the RF front-end in this paper is high performance and competitive in the band that we are interested in.

5. Conclusion

A high performance RF front-end for ultra-wideband 6–9 GHz is presented. LNA employs the resistive shunt feedback architecture, and the folded mixer is quadrature and gain controllable. The measurement results show the S_{11} of the front-end lower than –10 dB within the band. The high conversion gain is 23–26 dB while the low gain is 16–19 dB. The DSB

Table 2. Performance comparison.

Parameter	Ref. [6]*, 2008	Ref. [7], 2009	Ref. [8], 2006	This work
Technology	0.13 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
RF freq (GHz)	3–10	3–10	3–8**	6–9
S_{11} (dB)	< –10	< –7	< –8	< –10
Gain (dB)	26.3–28.7	24.3–29.1	20.2–22.8	23–26***
DSB NF (dB)	4.8–6.2	4.9–8.8	5.2–7.7	3.3–4.6
IIP3 (dBm)	–13.6	–13.5	–3.5	–12.6
Power (mW)	1.5 × 27	1.5 × 22	1.8 × 10	1.2 × 17
Total area (mm^2)	n/a	2.4	1.7	1.16

*: Post-layout simulation results. **: Without caring about the frequency band 4.752–6.336 GHz. ***: Gain controllable, and the low gain is 16–19 dB.

noise figure is 3.3–4.6 dB in the high gain mode and in band IIP3 is –12.6 dBm while operating in the low gain mode. The total power consumption is 20.4 mW with the 1.2 V supply voltage.

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