Electroplated indium bump arrays and the bonding reliability*

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Abstract: A novel electroplating indium bumping process is described, as a result of which indium bump arrays with a pitch of 100 μm and a diameter of 40 μm were successfully prepared. UBM (under bump metallization) for indium bumping was investigated with an XRD technique. The experimental results indicate that Ti/Pt (300 Å / 200 Å) has an excellent barrier effect both at room temperature and at 200 ℃. The bonding reliability of the indium bumps was evaluated by a shear test. Results show that the shear strength of the indium bump significantly increases after the first reflow and then changes slowly with increasing reflow times. Such a phenomenon may be caused by the change in textures of the indium after reflow. The corresponding flip-chip process is also discussed in this paper.

Key words: bumping; under bump metallization; shear test; bonding reliability
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1. Introduction

Hybrid pixel detectors are widely used in many fields, including military, environment, industry and medical treatment. When integrating such a detector, a vertical connection technique called flip-chip bonding is almost the only way to realize the high-density interconnection between the FPAs (focal plane arrays) and the ROICs (read-out integrated circuits). Such bonding can offer high-density I/O and a short interconnect distance, which can make the resulting device show excellent performance. The solder adopted to bond the FPAs and ROICs is also very important because some special requirements must be fulfilled in such an interconnection. For instance, the cooled infrared FPA device mainly works in the liquid nitrogen environment after integration at a relatively high temperature, e.g., above room temperature. In such an interconnection, indium is almost the only mating material that can be used because indium can stay ductile even at liquid helium temperature and form a good bond just at room temperature. So it can provide a flexible interconnection when integrating the FPA detector and avoid high-temperature bonding. Its relative ease of making very small solder bumps is another advantage, which makes the very high-density connection possible. Indium bump arrays of 7 μm in diameter and 20 μm in pitch have been reported. The standard industrial processes (e.g. the IBM C4 process) cannot prepare the bump arrays with such density[1−4].

Nowadays, two primary methods can be employed to fabricate indium bumps: a vaporation method and an electroplating technique (also called UV-LIGA). In the evaporation technique, indium is firstly deposited onto the substrate and then a lift-off process is performed. Such a process has been researched extensively and is usually used in the indium bumping method[3−5]. In the electroplating method, indium is electrodeposited onto the "desired" locations after lithography. Comparatively, the electroplating method is a cost effective, flexible indium bumping method, but research on it is very limited[4].

There are still many problems in electroplated indium bumping. The most difficult one is how to remove the seed layer after finishing indium electroplating. As is well known, Ti/Pt/Au, Ti/Ni/Au and Cr/Au are usually used as UBM (under bump metallization) in the indium bumping process[3,5]. In this experiment, Ti/Pt/Au is used as UBM for the indium bumps, which is also set as seed layer. Empirical experience indicates that it is impossible to remove the "stubborn" Ti/Pt/Au seed layer by chemical etching and IBE (ion beam etching) without changing the integrity of the indium bump because indium is a very active and fragile metal. That is to say, the traditional electroplated bumping approach, e.g. the electroplated SnAg bumping, etc, can not be used to prepare the indium bump arrays[6]. Such difficulty also won not appear in the evaporation bumping method, which is a traditional means of preparing indium bump arrays[3]. To overcome such a difficulty, a novel electroplating process should be adopted.

UBM processing is another important issue for indium bumping because it has a close relationship with bonding reliability and device performance. Normally, UBM plays the roles of adhesion to substrate, barrier and wetting to solder and constituting the ohm contact. For the UBM used in this experiment, Au is the wetting layer, Ti/Pt not only offers good adhesion character with the substrate, e.g. GaAs, SiO_2, but also provides an excellent barrier effect to the indium solder[7−9]. However, the barrier effect of UBM on the indium solder is still an open question. In this paper, the barrier effect of Ti/Pt/Au is investigated both at room temperature and 200 ℃, considering that the reflowed or un-reflowed indium bump arrays are used

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Table 1. Configurations and thermal conditions adopted to evaluate the barrier effect of Ti/Pt in the experiment.

Sample	Configuration/thickness (Å)	Thermal condition
A	Ti/Pt/Au/In ($10^2/10^2/10^3/10^4$)	Placed at room temperature for 30 days
B	Ti/Au/Ti/Pt/Au/In ($10^2/3\times10^3/10^2/10^2/10^3/10^4$)	Placed at room temperature for 30 days
C	Ti/Au/Ti/Pt/Au/In ($10^2/3\times10^3/10^2/10^2/10^3/10^4$)	Placed at room temperature for 60 days
D	Ti/Au/Ti/Pt/Au/In ($10^2/3\times10^3/10^2/10^2/10^3/10^4$)	Reflowed at 200 ℃ for10 min
E	Ti/Au/Ti/Pt/Au/In ($10^2/3\times10^3/2\times10^2/2\times10^2/10^3/10^4$)	Reflowed at 200 ℃ for10 min
F	Ti/Au/Ti/Pt/Au/In ($10^2/3\times10^3/3\times10^2/2\times10^2/10^3/10^4$)	Reflowed at 200 ℃ for10 min

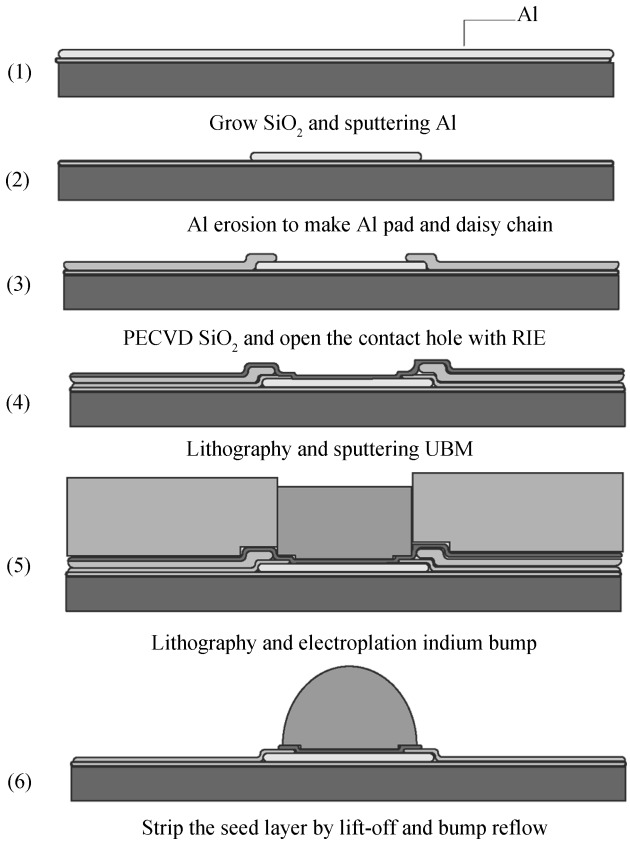

Fig. 1. Schematic process flow for electroplated indium bumping.

in the FPA device.

The reliability of indium solder bumps is evaluated by shear tests, and the internal mechanism for the change trend of shear strength with reflow times is discussed. The flip-chip bonding process is also discussed.

2. Experimental details

A novel indium bumping method is adopted in this experiment, as shown in Fig. 1. The details can be described as follows. (1) SiO_2 is grown on the Si (100) wafer by thermal oxidation and then Al is sputtered onto it via magnetron sputtering, with a thickness of 5000 Å for both SiO_2 and Al. (2) An Al pad and daisy chain are fabricated with phosphoric acid erosion followed by lithography. A photoresist S1912 with a thickness of 1.7 μm is used. (3) A SiO_2 passivation layer is deposited on the wafer with PECVD (plasma-enhanced chemical vapor), then lithography and RIE (reaction ion etching) erosion with CF_4 by step are performed to make the contact holes. (4) Lithography followed by deposition of a Ti/Pt/Au seed layer is carried out, which is also set as UBM. (5) Lithography of the AZ9260 with a thickness of 30 μm is carried out and then indium electroplating is performed in an indium plating bath. (6) The seed layer is stripped with a lift-off process by putting the wafer into hot acetone for 3 h. After stripping the seed layer, the indium bump is reflowed. In such a flow, a lift-off process is adopted to remove the seed layer, which is very different from the traditional electroplated bumping process[6].

To study the Ti/Pt/Au UBM, six samples, named A, B, C, D, E and F, were prepared and then subjected to different thermal processes, as listed in Table 1. Ti/Au/Ti/Pt/Au was deposited onto the Si (100) wafer sequentially in a vacuum of 10^{-6} Pa by magnetron sputtering, and then about 1 μm indium was electro-deposited onto the Au layer and then diced into 1 $\times$ 1.5 cm^2 chips. The thickness of the Ti, Pt and Au was monitored with a quartz-crystal oscillator and that of indium was controlled by lithography and a surface profiler. The adoption of the structure of Ti/Au/Ti/Pt/Au/In can be explained as follows. In this configuration, Ti/Pt is set as the barrier layer. If the Ti/Pt cannot efficiently block the indium, the indium will quickly react with the Au and then the Au layer under Ti/Pt will quickly disappear. So, by checking the existence of this Au layer, its barrier effect can be evaluated.

Based on the design of the multi-layer configuration, the key point is how to detect the existence of Au. Several methods can be adopted, such as XTEM (cross-sectional transmission electron microcopy), RBS (Rutherford backscattering spectrometry) and XRD (X-ray diffraction XRD)[8, 9]. Compared with XTEM and RBS, XRD is an easy and effective method. So, in this experiment, a CuKα1 X-ray source with 40 kV and 40 mA was used and XRD in the 2θ range 25°–90° with a step size of 0.02° was adopted to scan the surfaces of the samples. Considering the measurement accuracy of XRD, the thickness of the Au layer under Ti/Pt and the indium layer were controlled at 3000 Å and 1 μm, respectively.

A shear test was used to evaluate the strength of the indium bumps. The shear speed was 100 μm/s and the shear height was about 8 μm. At least 30 bumps were measured for every sample.

3. Results and discussion

3.1. Result of indium bump array fabrication

Figure 2 shows the indium bump arrays after reflow at 200 ℃ for 30 s. The figure indicates the high-quality of indium bump arrays fabricated using the process illustrated in Fig. 1. Uniformity is a critical index to evaluate the quality of a bump array. To investigate the uniformity of the indium bumps prepared in experiments, the heights of more than 240 indium

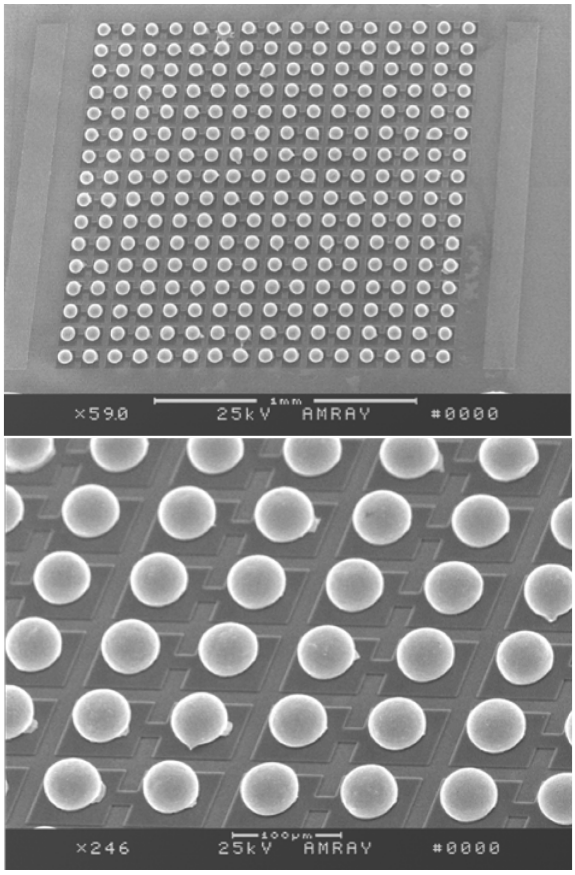

Fig. 2. A reflowed 16 × 16 indium bump array with 40 μm diameter and 100 μm pitch.

bumps were measured on six different areas of wafer with an Olympus STM6. The heights of the indium bumps at the edge of the wafer were generally greater than that at its center, which may be caused by the current density distribution when electroplating. The average height of the indium bumps was 43.4 μm and the uniformity was about 8.2% for the whole wafer. In a 16×16 BGA chip, the uniformity was about 1.5%–3.5%. The uniformity is calculated with the formula

$$\text{uniformity} = (H_{\max} - H_{\min})/(H_{\max} + H_{\min}), \qquad (1)$$

where H is the height of indium bump. After dicing, the dimension of the BGA (ball grid array) chip is about 2.2 × 2.2 mm^2. Such results indicate that indium bumps with good uniformity can be fabricated with the electroplating method.

3.2. Investigation of Ti/Pt/Au UBM

Figure 3 shows the XRD patterns for the samples Ti/Pt/Au/In (100 Å/100 Å/1000 Å/1μm), Ti/Au/Ti/Pt/Au/In (100 Å/3000 Å/100 Å/100 Å/1000 Å/1μm), Ti/Au/Ti/Pt/Au/In (100 Å/3000 Å/100 Å/100 Å/1000 Å/1 μm), named A, B and C, which were captured after being left in air at room temperature for 30 days, 30 days and 60 days respectively. It shows that sample A does not show any reflection peaks of Au but $AuIn_2$ (PDF#03-0939), indium (PDF#05-0642) and Si (004). This indicates that Au has been fully transformed into $AuIn_2$ IMC, which is consistent with Refs. [10, 12]. In the XRD pattern of sample B, not only $AuIn_2$ and indium but also Au reflection peaks appeared. Obviously, these are generated by the existence of Au under the Ti/Pt layer. The XRD result from sample C is similar to that of sample B, just different in the intensity of the reflection peaks. Such results indicate that Ti/Pt (100 Å / 100 Å) is an effective barrier to indium solder at room temperature. It is hard to identify the pure Ti and Ti-contained compounds in the XRD spectra because either the amount of Ti is very small or the peak positions are very close to those of the Au-In IMC.

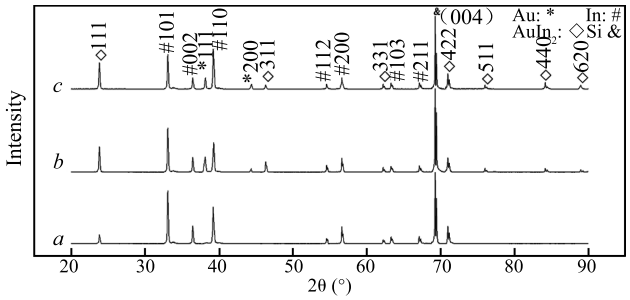

Fig. 3. XRD patterns for samples (*a*) A, (*b*) B and (*c*) C aging at room temperature for 30 days, 30 days and 60 days, respectively.

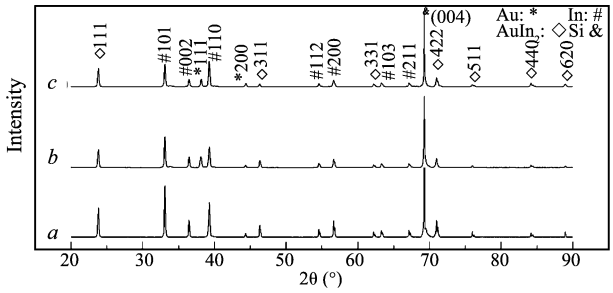

Fig. 4. XRD patterns for samples (*a*) D, (*b*) E and (*c*) F after reflow at 200 ℃ for 10 min.

However, it is also important to note whether the Ti/Pt (100 Å/100 Å) layer has a good barrier effect for melting indium because it may be reflowed in indium bumping[5, 6]. In order to evaluate the barrier of the Ti/Pt layer at reflow temperature, another Ti/Au/Ti/Pt/Au/In (100 Å/3000 Å/100 Å/100 Å/1 μm) sample, named D, was annealed in a flowing N_2 ambient at a temperature of 200 ℃ for 10 min, just simulating the imposed reflow process. The related XRD pattern is shown in Fig. 4(a), with the feature that the diffraction peaks of Au have disappeared. Such a result indicates that the Ti/Pt (100 Å/100 Å) layer is no longer a good barrier layer to indium under the 200 ℃/10 min reflow conditions.

One possible way to improve the barrier effect is to thicken the Ti/Pt layer. So the samples with the configuration of Ti/ Au/Ti/Pt/Au/In (100 Å/3000 Å/200 Å/200 Å/1000 Å/1 μm) and Ti/Au/Ti/Pt/Au/In (100 Å/3000 Å/300 Å/200 Å/1000 Å/1 μm), named E and F, were prepared and then annealed at 200 ℃ for 10 min. The related XRD result is shown in Figs. 4(b) and 4(c). The diffraction peaks of Au appear in both XRD patterns. Such result indicates that Ti/Pt (200 Å/200 Å) and Ti/Pt (300 Å/200 Å) can prevent indium from penetrating through them for more than 10 min at 200 ℃.

In the FPA application, indium solder may experience two

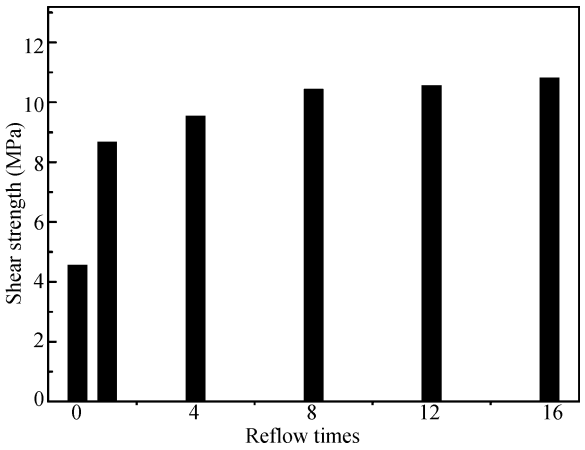

Fig. 5. Shear strength of indium bump after multi-reflows. The reflow condition is 200 ℃/30 s for each time.

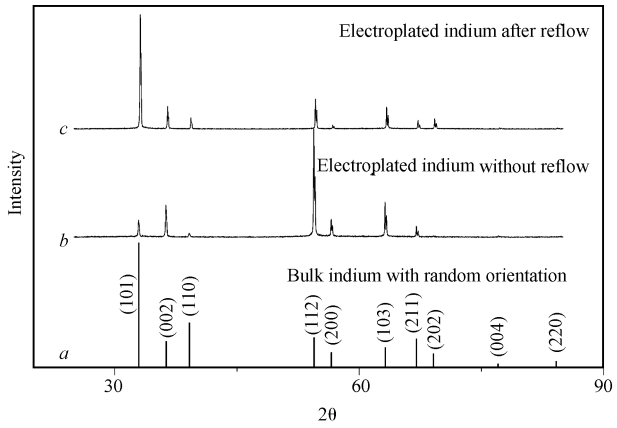

Fig. 6. XRD patterns of (*a*) bulk indium with random orientation electroplated indium (*b*) without reflow and (*c*) after reflow at 200 ℃ for 30 s.

stages of the reflow process. One is in indium bumping; the other is during flip-chip bonding. However, the total time spent in these two steps is less than 10 min and the temperature is below 200 ℃. After integration, indium mainly works at a very low temperature, such as in a liquid nitrogen or liquid helium environment[5, 6]. Considering the performance of the Ti/Pt barrier layer both at room temperature and at 200 ℃, it is estimated that Ti/Pt (300 Å/200 Å) as a barrier layer to indium can be used in FPA application.

3.3. Shear test for indium bump

Figure 5 shows the shear strength of the indium bumps for different reflow times, with the reflow condition of 200 ℃/30 s for each time. It shows that the shear strength of the indium bumps significantly increases after the first reflow, and then changes little with increasing reflow times.

As is well known, the shear strength closely relates to the grain size and texture of materials, especially for elementary metals[10, 11]. The yield stress with the grain size can be described by the Hall-pitch[12],

$$\sigma_{\rm s} = \sigma_0 + kd^{-1/2}, \tag{2}$$

where $\sigma_{\rm s}$ is the yield stress, σ_0 and k are material constants and d is the grain size. According to the Hall-pitch equation, the smaller grain size will result in the higher shear strength. The grain size of indium should increase after reflow because reflow is a thermal process, so the shear strength should decrease. However, the result of the shear test is opposite to the analysis above. So the change in the shear strength is likely caused by the texture in indium.

The XRD technique is an easy way to determine whether texture exists in a metal[13]. Two 1 × 1.5 cm^2 Ti/Pt/Au/Ep In (300Å/200 Å/1000 Å/30 μm) samples, which were captured just after finishing electroplating and reflowed at 200 ℃ for 30 s, respectively, were measured with XRD in the experiment. The related XRD patterns are shown in Figs. 6(b) and 6(c), respectively. Figure 6(a) shows the diffraction peaks for the stand indium with random orientation (PDF#05-0642). As shown in Figs. 6(a) and 6(b), the three strongest peaks appears at (112), (103) and (002) for electroplated indium without reflow while at (101), (110) and (112) for the standard bulk indium sample with random orientation. Such a result indicates that obvious texture exists in the sample without reflow. To characterize its preferred crystal orientation, a coefficient of texture is cited, as in the following formula[13],

$$C_{\rm m}(hkl) = \frac{I_{\rm m}(hkl)}{I_0(hkl)} \Big/ \frac{1}{n}\sum_{\rm n=1}^{n} \frac{I_{\rm m}(hkl)}{I_0(hkl)}, \tag{3}$$

where $I_{\rm m}(hkl)$ is the relative diffraction intensity of the measured sample and $I_0(hkl)$ is that of the standard sample.

Table 2. Relative intensity (I_0) of standard bulk, relative intensity and coefficients of texture of crystal planes for the sample without reflow ($I_{\rm m}, C_{\rm m}$) and after reflow at 200 ℃ for 30 s ($I'_{\rm m}, C'_{\rm m}$).

Crystal plane *(hkl)*	I_0	$I_{\rm m}$	$I'_{\rm m}$	$C_{\rm m}$	$C'_{\rm m}$
In(101)	100	16.15	100	0.112	1.347
In(110)	36	4.2	10.01	0.081	0.374
In(112)	24	100	26.35	2.899	1.479
In(211)	23	10.64	7.73	0.321	0.452
In(002)	21	30.2	20.04	1.000	1.286
In(103)	16	32.7	19.54	1.422	1.645
In(200)	12	20	3.68	1.159	0.413

The texture coefficients for these two samples are shown in Table 2. This shows that the largest value is 2.899, corresponding to the (112) plane for the electroplated indium without reflow. For the sample after reflow at 200 ℃ for 30 s, it becomes 1.479. Such results indicate that an obvious texture appears in the electroplated indium without reflow and the (112) preferred orientation is significantly weakened after reflow. The result of the shear test can be explained as follows. After the first reflow, the texture in electroplated indium is significantly weakened, which leads to the great change in shear strength. Increasing the reflow times after that, the texture in indium changes little, so the shear strength has no obvious change. (100) preferred orientation appears in the evaporation-deposited indium on Au film and the change trend of the shear strength with the reflow process for the indium bump is consistent with the result of this experiment[11].

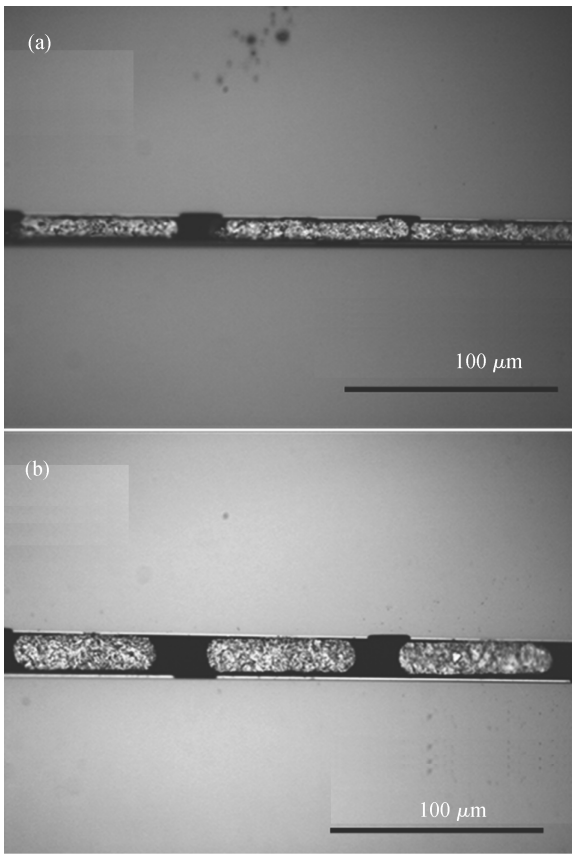

Fig. 7. Cross-section for the sample after flip-chip with the pressure at (a) 3 kg and (b) 1 kg.

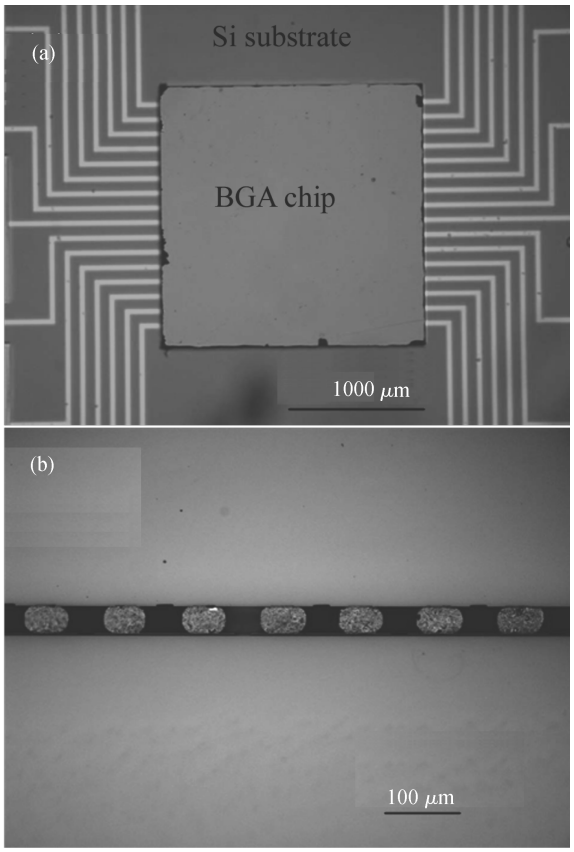

Fig. 8. (a) Integrated chip by flip-chip bonding. (b) Cross-section of the integrated chip.

3.4. Flip-chip bonding for indium bump array

An indium bump array chip is bonded to the Si substrate via the flip-chip process with SEC410 in this experiment. As is well known, the temperature and pressure are the most crucial factors in such a process. Considering the excellent plasticity of indium, the flip-chip process was performed at room temperature. The pressure of 3 kg and 1 kg, corresponding to 11.7 g and 3.9 g per bump, were tried in the experiment. The related cross-sections are shown in Figs. 7(a) and 7(b). It can be seen that 3 kg pressure can make the two adjacent indium bumps stick together. Compared with 3 kg pressure, 1 kg pressure is relatively suitable for this flip-chip bonding process. Further study indicates that pressure of about 3–5 g per bump is suitable for flip-chip bonding of indium in this experiment. To get high-quality bonding, 5RMA flux is also used in experiment and the integrated chip is reflowed. Figures 8(a) and (b) show the integrated chip and its corresponding cross-section, respectively.

4. Conclusions

Some issues about electroplated indium bumping, such as the fabrication process, the barrier effect of Ti/Pt/Au UBM and the change in the shear strength, are discussed in this paper. Some conclusions can be summarized, as follows:

(1) Indium bump arrays can be successfully prepared with the electroplating method. The "stubborn" seed layer can be successfully removed via a lift-off process.

(2) A Ti/Pt (300 Å/200 Å) layer can be used in indium bumping because it has an excellent barrier effect, both at room temperature and at 200 ℃.

(3) There is a significant increase in the shear strength of the indium bump after the first reflow. Such a phenomenon may be caused by the change in the texture of the electroplated indium solder. To get higher shear strength, the indium bump should be reflowed.

(4) Due to the excellent plasticity of the indium solder, the flip-chip process for an indium bump array can be performed at room temperature with low pressure. 3–5 g pressure per bump is enough for the indium flip-chip bonding in this experiment.

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