Density-controllable nonvolatile memory devices having metal nanocrystals through chemical synthesis and assembled by spin-coating technique

Wang Guangli(王广利), Chen Yubin(陈裕斌), Shi Yi(施毅)†, Pu Lin(濮林), Pan Lijia(潘力嘉), Zhang Rong(张荣), and Zheng Youdou(郑有炓)

(School of Electronic Science and Technology and National Laboratory of Solid State Microstructures, Nanjing University, Nanjing 210093, China)

Abstract: A novel two-step method is employed, for the first time, to fabricate nonvolatile memory devices that have metal nanocrystals. First, size-averaged Au nanocrystals are synthesized chemically; second, they are assembled into memory devices by a spin-coating technique at room temperature. This attractive approach makes it possible to tailor the diameter and control the density of nanocrystals individually. In addition, processes at room temperature prevent Au diffusion, which is a main concern for the application of metal nanocrystal-based memory. The experimental results, both the morphology characterization and the electrical measurements, reveal that there is an optimum density of nanocrystal monolayer to balance between long data retention and a large hysteresis memory window. At the same time, density-controllable devices could also feed the preferential emphasis on either memory window or retention time. All these facts confirm the advantages and novelty of our two-step method.

Key words: metal nanocrystal; nonvolatile memory; self-assemble; spin-coating technique; conductance–voltage curve; memory window

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1. Introduction

In recent years, rapidly increasing demand for nonvolatile memory chips is being driven by blistering expansion of various electronic devices, especially consumer mobile electronics.[1]. Various kinds of memory technologies have been developed, such as nanocrystals[2], phase-change[3, 4], resistive switching[5], spin electrons[6, 7], organic[8] and even protein-based[9] memory devices, among which nanocrystal nonvolatile memory devices provide a commercially attractive and viable alternative to the conventional poly-Si floating gate flash memories. To improve the memory performance, there are mainly three approaches: importing new materials ($Ge_{1-x}Si_x$, metal and their alloy)[10, 11], proposing novel device structure (FinFET, double gate, split-gate, etc) and unconventional fabricating processes[12−18]. New devices do behave better compared to their conventional counterparts, which are fabricated mainly at temperatures higher than 800 ℃ through physical methods, and they usually show an uncontrollable nanocrystal density and a relatively small memory window. In this paper, two approaches are adopted. (1) Au nanocrystals are used as storage nodes. Compared to their semiconductor counterparts, there are fewer interface states between metal nanocrystals, and tunneling oxide—interface states will worsen the data retention[19]. In addition, the high density of states exists around the metal Fermi level and the work function could also be engineered easily by selecting various metal materials. As a result, strong reliability, high storage density and long data retention are promised[20, 21]. (2) A two-step fabrication process offers an attractive solution to optimize the storage characteristics owing to its ability to tailor the diameter and control the density of nanocrystals separately. First, mono-dispersed metal nanocrystals of average size are synthesized chemically[22, 23]. Second, a metal nanocrystal monolayer of variable density can be deposited on the tunneling oxide by a self-assembly method[24, 25], such as the spin-coating technique[26] adopted here. Another advantage of this two-step method is its compatibility with advanced CMOS processes at relatively low temperature to avoid metal Au diffusion, which is a main concern for the application of metal nanocrystal-based memory. Nonvolatile memory devices with materials of high dielectric constant, such as HfO_2, should also be fabricated at relatively low temperature, since they might suffer from crystallization during a high-temperature process. In brief, this hybrid bottom-up/top-down approach would lead to a novel strategy for device fabrication, which is impossible with the conventional top-down approach[27].

2. Experimental details

$HAuCl_4 \cdot xH_2O$ was purchased from Aldrich (99.99%). The other reagents were acquired from standard sources and then used directly. 1.5 g tetraoctylammonium bromide in 80 mL of toluene was added to 0.31g $HAuCl_4 \cdot xH_2O$ in 25 mL deionized water, and then stirred vigorously. The yellow $HAuCl_4 \cdot xH_2O$ aqueous solution quickly cleared and the toluene phase became orange-brown. After the organic phase was isolated, a certain amount of dodecanethiol was added and then the solution was stirred for 10 min at room temperature. $NaBH_4$ aqueous solution (0.38 mL $NaBH_4$: 25 mL deionized water) was then added to the solution and vigorously stirred for 3.5 h. The organic

† Corresponding author. Email: yshi@nju.edu.cn

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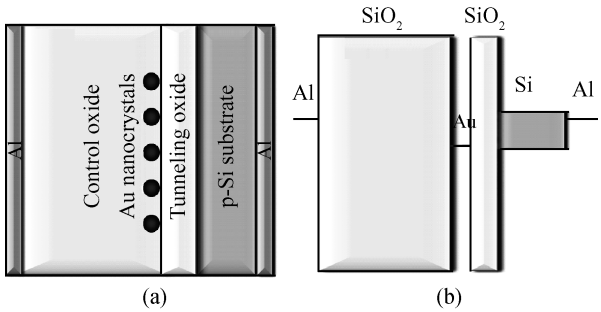

Fig. 1. (a) Schematic illustration and (b) energy band diagram of metal nanocrystal nonvolatile memory devices.

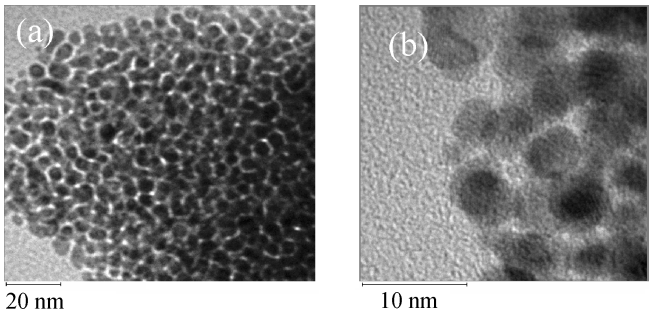

Fig. 2. (a) TEM and (b) HRTEM image of colloid Au nanocrystals.

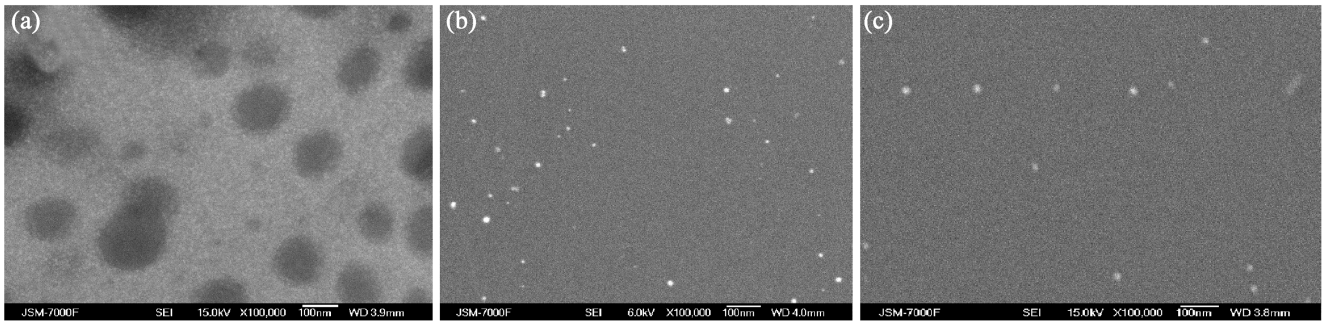

Fig. 3. SEM images of Au nanocrystal monolayer with (a) high density, (b) medium density and (c) low density.

phase solvent was removed with a rotary evaporator and the dark product was collected and suspended in 30 mL ethanol. The solution was sonicated to ensure complete dissolution of the by-products, then collected on a glass filtration frit and washed with at least 80 mL of ethanol and 150 mL of acetone. Finally, the black product, i.e., dodecanethiolate-protected Au nanocrystals, was dispersed in 20 mL hexane for the next process[28].

Colloid Au nanocrystals/hexane solvents of different concentrations were then dripped onto the 2.5 nm tunneling oxide to form a nanocrystal monolayer of three different densities by a spin-coating technique. The spin speed was 600 rpm in the first step, lasting 6 s, and was then increased to 2000 rpm in the second step for 30 s. Finally, 30 nm control oxide (SiO_2) and aluminum electrodes were deposited step by step to form sandwich-structure memory MOS capacitors.

Four reference samples were also fabricated with different concentrations of dodecanethiol/hexane solution without Au nanocrystals. Firstly, four dodecanethiol/hexane solutions were prepared with the volume ratio of dodecanethiol to hexane 0 : 100, 1 : 100, 10 : 100 and 100 : 0. Secondly, the four solutions were dripped onto the tunneling oxide by a spin-coating technique. Hexane solvent was evaporated and the leavings-organic molecule dodecanethiol-remained on the tunneling oxide. Finally, the control oxide and Al electrodes were deposited to form a sandwich device structure.

Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) were employed to observe the morphology of the samples. The electrical properties of the samples were measured by a HP 4284A precision LCR meter at room temperature.

3. Results and discussion

Figures 1(a) and 1(b) show the cross section diagram and energy band diagram of Au nanocrystal-based nonvolatile memory devices. Figure 2 shows the TEM and HRTEM images of Au nanocrystals with an average core diameter of 4.5 nm. Figure 3 shows an SEM image of an Au nanocrystal monolayer of three different densities deposited by a spin-coating technique on the tunneling oxide. The density of the sample with highly dense Au nanocrystal is far beyond 1×10^{12} cm^{-2}, perhaps due to that part of the metal nanocrystal array being a multi-layer structure. The density of the samples with medium and low density Au nanocrystal monolayer is 4.1×10^9 and 1.2×10^9 cm^{-2}, individually.

For practical memory applications, a wide memory window is essential to distinguish the programmed and erased states. We measured the capacitance response of the nanocrystal monolayer at 1 MHz as a function of voltage biased between top and bottom Al electrodes. The capacitance versus voltage curve (C–V) and conductance versus voltage curve (G–V) are obtained by sweeping the applied voltage from negative bias to positive bias, and back to negative bias at room temperature (the surface of p-type silicon substrate changes from accumulation region to inversion region, and back to accumulation region). Figures 4, 5 and 6 show C–V and G–V (inset) curves of samples with high density, medium density and low density Au nanocrystals, respectively. According to these C–V curves, the counter-clock memory windows of these samples are 2 V, 1 V and 0.8 V separately at the applied voltage of 10 V. And memory windows vary significantly at different applied voltages. The trend of G–V curves is similar to that of C–V curves.

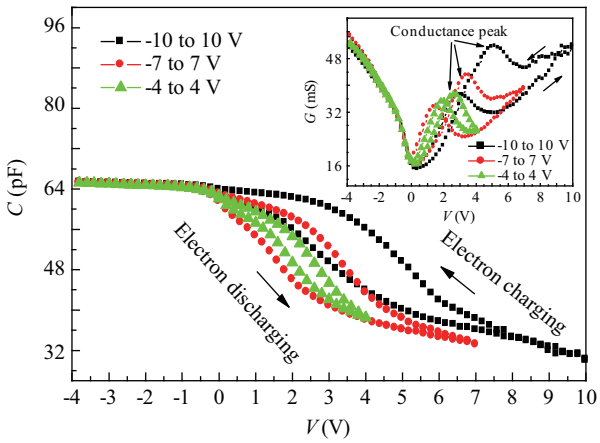

Fig. 4. C–V and G–V (inset) characteristics of memory devices with high density Au nanocrystal monolayer.

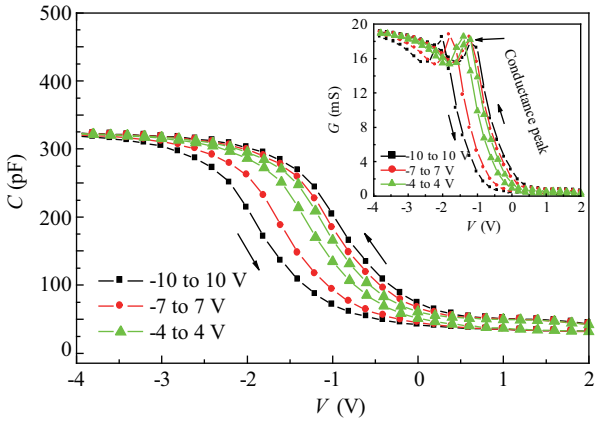

Fig. 5. C–V and G–V (inset) characteristics of memory devices with medium density Au nanocrystal monolayer.

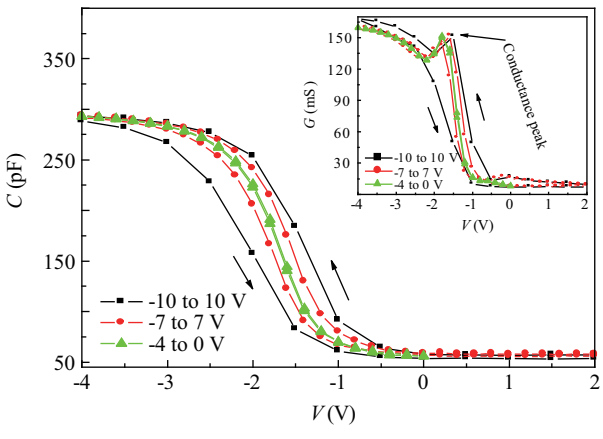

Fig. 6. C–V and G–V (inset) characteristics of memory devices with low density Au nanocrystal monolayer.

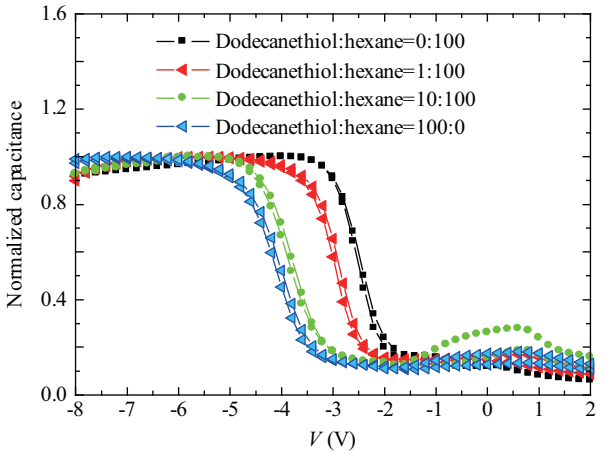

Fig. 7. C–V curve shift toward negative bias with increasing density of dodecanethiol molecules within the sandwich memory structure of four reference samples.

This phenomenon indicates that electrons are injected into Au nanocrystals and interfacial traps from a silicon substrate at applied positive voltage or pulled out reversely at applied negative voltage. Interfacial traps contain two kinds: one lying between control oxide and tunneling oxide, the other among Au nanocrystals and the surrounding oxide due to a dodecanethiol molecule monolayer on the surface of the Au nanocrystals. The well-ordered dodecanethiol molecule monolayer is conformed to be an insulator layer with EOT (effective oxide thickness) 1 nm[29].

According to Fig. 3, samples with medium and low density have very few Au nanocrystals, resulting in low coupling between the storage layer and the substrate. Question that whether Au nanocrystals or interfacial traps are injected electrons is yielded. To confirm this, four reference samples are fabricated, with different concentrations of dodecanethiol/hexane solution. The volume ratio of dodecanethiol to hexane was 0 : 100, 1 : 100, 10 : 100 and 100 : 0 individually. These reference samples had no charging effects as they showed negligible memory windows in the C–V curves (Fig. 7). So the conclusion can be drawn that the Au nanocrystals other than interfacial traps are mainly responsible for the storage, even in the case of low-density samples. The C–V curve shifts toward negative voltage with increasing density of dodecanethiol molecules on the tunneling oxide (or higher volume ratio of dodecanethiol), indicating that fixed positive charges have been introduced into the interface between the Au nanocrystals and the tunneling oxide, and they increase while raising the density of the dodecanethiol molecules on the tunneling oxide.

Another most important factor for the application of nonvolatile memory devices is their data retention. Figure 8 shows the data retention (capacitance–time curve or C–t curve) of memory structures with Au nanocrystal monolayers of different densities. The program transient is 10 V for 5 s, while the erase transient is –10 V for 5 s. The charge loss rate of injected electrons is much slower than that of injected holes, which could be explained using an energy band diagram of the memory structure in Fig. 1(b). Although the energy band difference between E_F (Fermi energy) of the Au nanocrystals and the E_C (conduction band energy level) of the tunneling oxide SiO_2 is comparable to the one between E_F of the Au nanocrystals and E_V (valence band energy level) of the SiO_2, the energy band difference between E_F of the Au nanocrystals and E_C of the

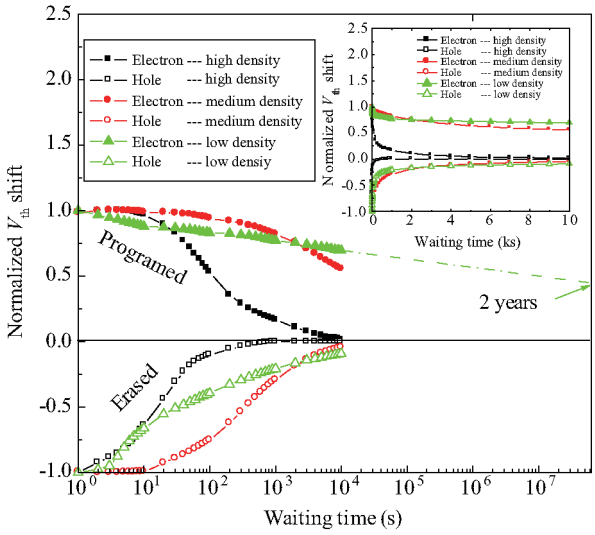

Fig. 8. Data retention of memory devices with Au nanocrystal monolayer of three different densities with a logarithmic and linear (inset) scale of horizontal axis.

Si substrate is much larger than the one between E_F of the Au nanocrystals and E_V of the Si substrate. So it is much more difficult for electrons to leak from E_F of the Au nanocrystals to the conduction band of the Si substrate than for holes to the E_V of the Si substrate, leading to longer data retention for electrons.

Various charge loss mechanisms have been introduced in detail in Ref. [30]. In our case, four of them—Coulomb repulsion induced charge loss, direct tunneling charge loss (DL), oxide defect induced charge loss (OL) and lateral charge loss (LL, the combination of DL and OL) as illustrated in Fig. 9—could be used here to explain the charge loss in Fig. 8. The inset of Fig. 8 shows two different capacitance decays for the three samples. The fast decay is due to Coulomb repulsion. Mass charges are injected into the Au nanocrystals from the Si substrate when memory devices are applied program voltage or erase voltage. After taking off the applied voltage, extra charges tunnel back to the Si substrate because of Coulomb repulsion. The following slower decay is the result of OL and DL, as illustrated in Fig. 9(b). In addition, the decay of nonvolatile memory structures with a high density Au nanocrystal monolayer, as illustrated in Fig. 9(a), is much faster than the other two samples. The reason is that the lateral charge loss, which can be neglected for a medium or low density nanocrystal monolayer, plays an important role among high density Au nanocrystal monolayers, and then LL accelerates OL. The memory device with a low density Au nanocrystal monolayer exhibits the best performance, with a charge loss of about 50% in the 2nd year long. It is evident that there is a nanocrystal monolayer of optimum, controllable density to provide a reasonable compromise between long data retention and large memory window.

4. Conclusion

To improve the performance of nanocrystal-based memory devices, it is important to study how to control the density of nanocrystals and how to maintain the memory retention before a successful and reliable implementation can be achieved. This

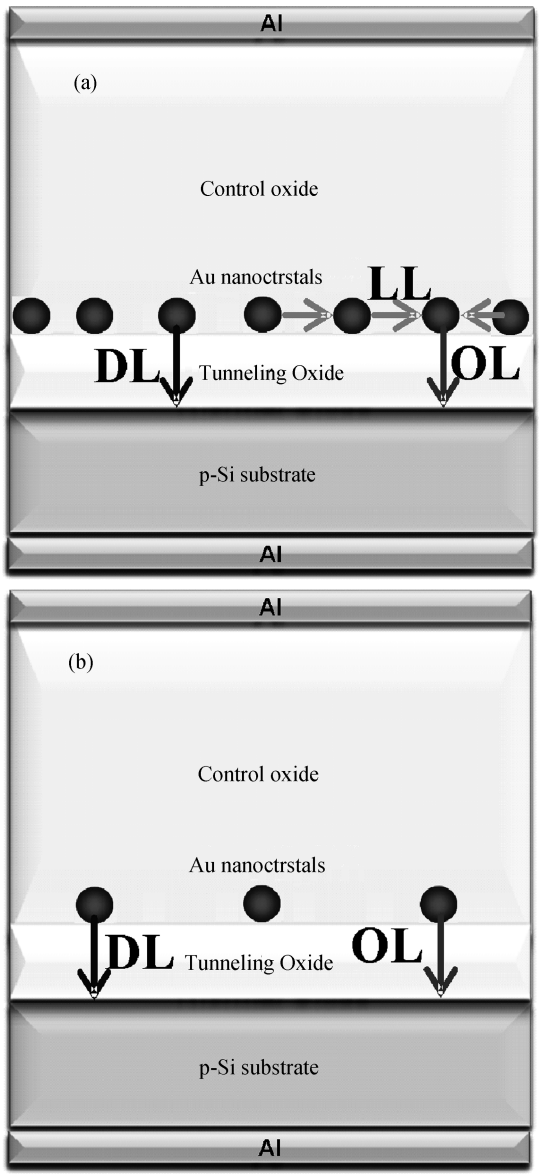

Fig. 9. Illustration of charge loss mechanisms of nonvolatile memory devices with (a) high density nanocrystals monolayer and (b) medium or low density nanocrystals monolayer.

paper offers a new method to make the Au nanocrystal monolayer memory devices with tailored performance. The charge storage characteristics of the samples indicate good storage capability. The counter-clock memory windows of the C–V curve are 2 V, 1 V and 0.8 V individually under double sweep –10 to10 V. The capacitance-time curves of these samples indicate that a nanocrystal monolayer of exorbitant density does behave unsatisfactorily in data retention although widening the counter-clock memory window. In the mean time, a nanocrystal monolayer of low density is beneficial for longer data retention. So it is important to embed nanocrystals of appropriate density in nonvolatile memory devices to balance between a larger memory window and longer data retention. In conclusion, the main contributions from this work are in the following three aspects. (1) A two-step method is employed to tailor the diameter and control the density of the nanocrystals separately. (2) Combination of chemical synthesis and spin-coating depo-

sition is performed at room temperature, preventing unwanted Au diffusion in memory devices. (3) It is found that there is optimum density of the nanocrystal monolayer to provide a reasonable compromise between longer data retention and larger memory window.

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