Influence of voltage on photo-electrochemical etching of n-type macroporous silicon arrays*

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Abstract: The influence of voltage on photo-electrochemical etching (PEC) of macroporous silicon arrays (MSA) was researched. According to the theory of the space charge region, I–V scan curves and the reaction mechanism of the n-type silicon anodic oxidation in HF solution under different current densities, the pore morphology influenced by the working voltage were studied and analyzed in detail. The results show that increasing the etching voltage will lead to distortion of the pore morphology, decreasing etching voltage will result in an increase in the blind porosity, and the constant etching voltage for a long time will cause gradual bifurcation. Through the optimization of the process parameters, the perfect MSA structure with a pore depth of 317 μm, a pore size of 3 μm and an aspect ratio of 105 was obtained.

Key words: etching voltage; macroporous silicon arrays; photo-electrochemical etching; blind porosity
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1. Introduction

Since the 1950s, Uhlir and Turner have reported the formation of porous silicon (PS) films under the conditions of anodic oxidation[1, 2], and much attention has been given to the study and application of PS. PS can be divided into 3 types according to its aperture size: macroporous silicon, mesoporous silicon and nanoporous silicon (sometimes also called microporous silicon). The pore size of macroporous silicon is about several micrometers. This has a pore-like and columnar structure, and can be obtained from low-doped n-type silicon. The pore size of mesoporous silicon is 10–500 nm. This can be obtained from heavily (degenerately) doped silicon substrate, either n-type or p-type. The pore size of microporous silicon is about several nanometers. This can be obtained either from low-doped p-type silicon or from low-doped n-type silicon. The pore size of PS can be controlled by the doping, the HF concentration, the etching time and the applied current density[3]. In 1972, Theunissen first reported the formation of n-type macroporous silicon arrays (MSAs) in HF aqueous solution[4]. In the 1990s, Lehmann and Föll *et al.* studied n-type MSA formation mechanism in detail, and fabricated an MSA structure with a high aspect ratio[5, 6]. Since then, MSAs have attracted widespread attention. Devices based on MSAs have become a research hotspot. MSAs can be applied to MEMS devices[7], signal interconnection among multi-layer semiconductor devices[8], microchannel heat transfer devices[9], micro-channel plate and photonic crystals in the infrared band[10−13].

The formation of n-type MSAs is a complex photo-electrochemical (PEC) reaction process. Although some papers have discussed the formation mechanism, and analyzed the macroporous silicon morphology affected by the etching current density, voltage, light, etching time, solution and other factors, little attention has been given to the systematic discussion of the influence of etching voltage. In this work, the influence of the etching voltage on the cross-section morphology of the macropores and blind porosity of MSAs was analyzed systematically. The process parameters were optimized and the perfect MSA structure with a high aspect ratio was fabricated.

2. Experiments

The electrochemical etching process for MSAs is shown in Fig. 1, which includes the preparation of an ohmic contact layer, SiO_2 masking film etching, induced pit corrosion, deep PEC etching of silicon and backside thinning. To meet the crystal orientation requirements of the induced pit process and PEC etching, an n-type silicon wafer was selected with ⟨100⟩ orientation, 4 inch diameter, 2–4 Ω·cm resistivity and 500 μm thickness.

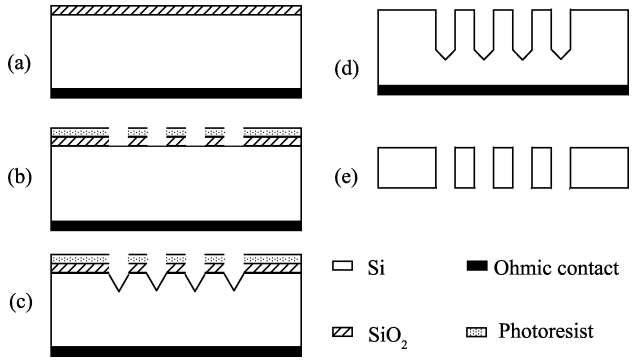

Fig. 1. Flow diagram of electrochemical etching process for MSAs. (a) Preparation of ohmic contact layer. (b) SiO_2 masking film etching. (c) Induced pit corrosion. (d) PEC etching. (e) Backside thinning.

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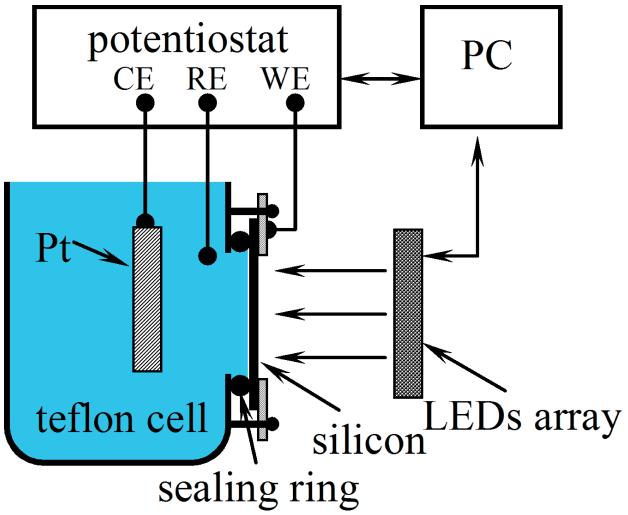


Fig. 2. PEC etching set-up.

Figure 2 shows the setup for PEC etching. One side of a teflon electrolytic cell is open to fix silicon. The LED array with a 850 nm wavelength is used as the light source in order to excite electron hole pairs on the backside of the silicon wafer. The wafer was the working electrode (WE). The counter electrode (CE) was prepared from the 25 cm^2 Pt wire grid and a saturated calomel electrode was the reference electrode (RE). The three electrodes were controlled by the integrated electrochemical test system of a PARSTAT 2273 produced by Princeton Applied Research Co. HF solution diluted with de-ionized water was used as the etching solution. All experiments were carried out at a temperature of 300 K.

3. Results and discussion

3.1. *I–V* scan curve analysis

Figure 3 shows the I–V scan curve of an n-type silicon wafer with induced pits in the process of PEC etching every 1 h. J_{PS} is the critical current density, denoting the transition from the charge-supply-limited to the mass-transport-limited case. The critical current J_{PS} and working voltage V are both gradually reduced in the etching process. This can be explained by the expression of J_{PS} (mA/cm^2)[6].

$$J_{PS} = Bc^{3/2}\exp(-E_a/K_0T), \tag{1}$$

where $B = 3.3 \times 10^9$ mA/cm^2, $E_a = 0.345$ eV for the reaction activation energy, $K_0 = 1.38 \times 10^{-23}$ J/K for the Boltzmann constant, c (wt%) for the HF concentration and T (K) as the solution temperature. Equation (1) indicates that J_{PS} will decrease with decreasing HF concentration. As the pore depth increases, mass transport becomes difficult, and the HF concentration continuously reduces, which causes J_{PS} to decrease gradually.

3.2. Influence of voltage on the macropore cross section morphology

The cross-section morphology of macropores etched at different voltages were observed with an optical microscope, as shown in Fig. 4. The etching current density remained 10 mA/cm^2 with an etching time of 1 h. With increasing voltage, the shape of the pore cross section gradually changed from a square to a circle, then to the astroid at 3 V, gradually bifurcating at 5 V. A single pore changed into a number of pores at 9 V. These experimental results are due to the different distributions of holes as the electric field changed at the pore tip.

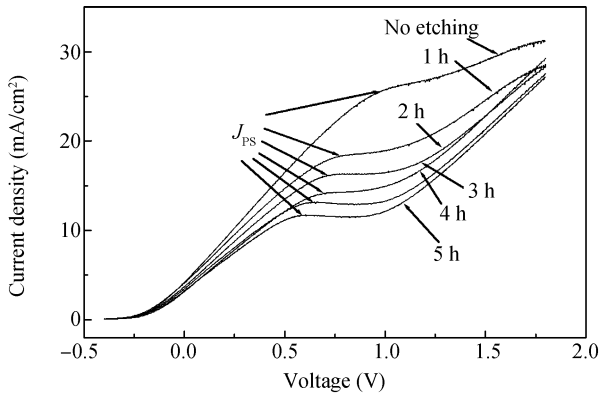


Fig. 3. Current–voltage scan curves for n-type silicon wafers with induced pits.

Figure 5 shows the metalloscope photographs of the MSA profile etched at 0.8 V for 8 h. It was found that etching at a constant voltage for a long time results in the pores gradually changing shape. Since the mass transport of HF solution becomes difficult as the pores grow, the HF concentration at the pore tip decreases, and the critical current J_{PS} and the corresponding voltage V decrease gradually. The pore distortion takes place gradually in etching at constant voltage because of the distribution of the holes changing. The etching voltage must be modulated based on the I–V curves and experience in order to keep the pore shape unchanged in the process, as shown in Fig. 8.

3.3. Influence of voltage on the blind porosity

Blind porosity is defined as the ratio of the number of not-pass-through pores to that of all the pores per unit area. The profiles of the MSAs with etching time of 1.5 h are shown in Fig. 6, where it was found that the blind porosity increased with decreasing voltage. The n-type silicon/solution interface can be considered approximately as a p^+n one-sided step junction. The potential difference occurs mainly across the semiconductor space charge region, and the relationship between the space charge region width and the voltage applied can be expressed as

$$W_{SCR} = \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}(V_D - V)}{qN_D}}, \tag{2}$$

where W_{SCR} is the space charge region width on the Si side of the Si/HF interface, and V is the etching voltage.

According to Eq. (2), the width of the space charge region decreases as the reverse bias voltage reduces. The hole number at the pore walls is much less than that on the pore tip, so the etching current density J is smaller than J_{PS}, and the porous silicon is formed on the wall. The reaction will be in accordance with Eq. (3)[14].

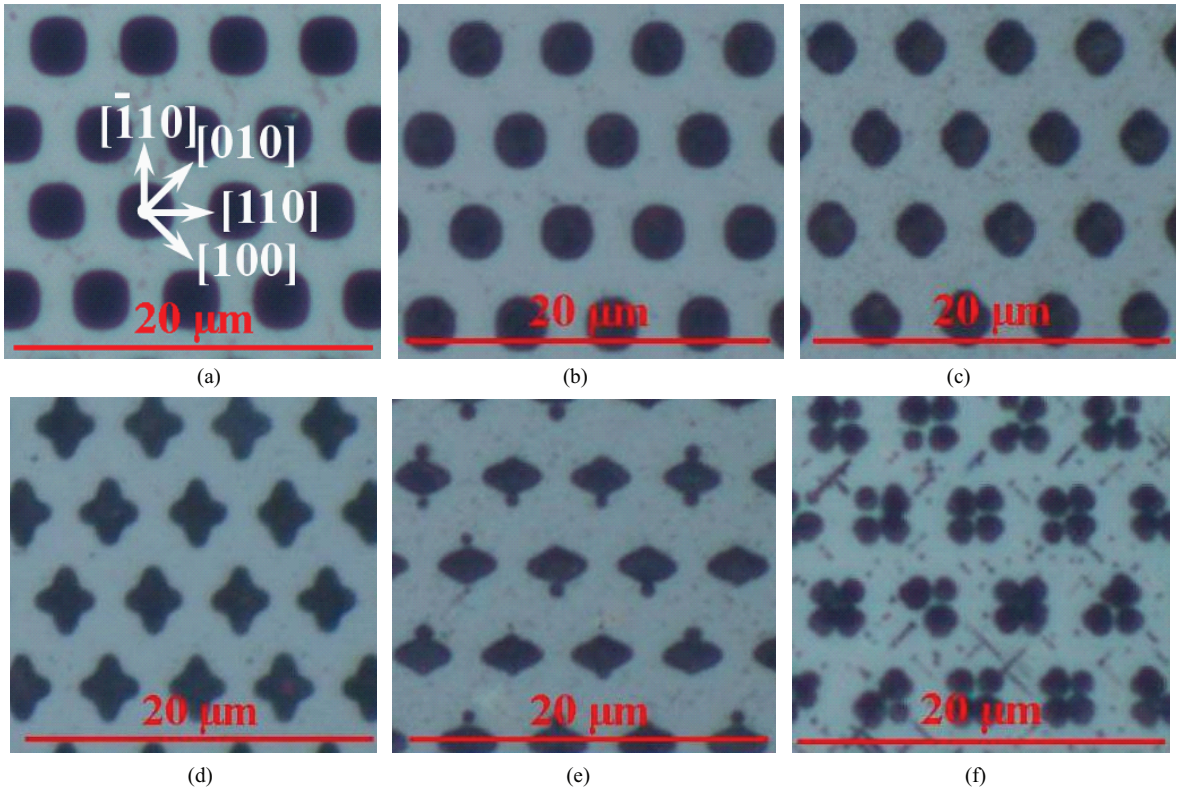


Fig. 4. Metalloscope photographs of the pore cross sections etched at different voltages. (a) 0.6 V. (b) 1.0 V. (c) 1.5 V. (d) 3.0 V. (e) 5.0 V. (f) 9.0 V.

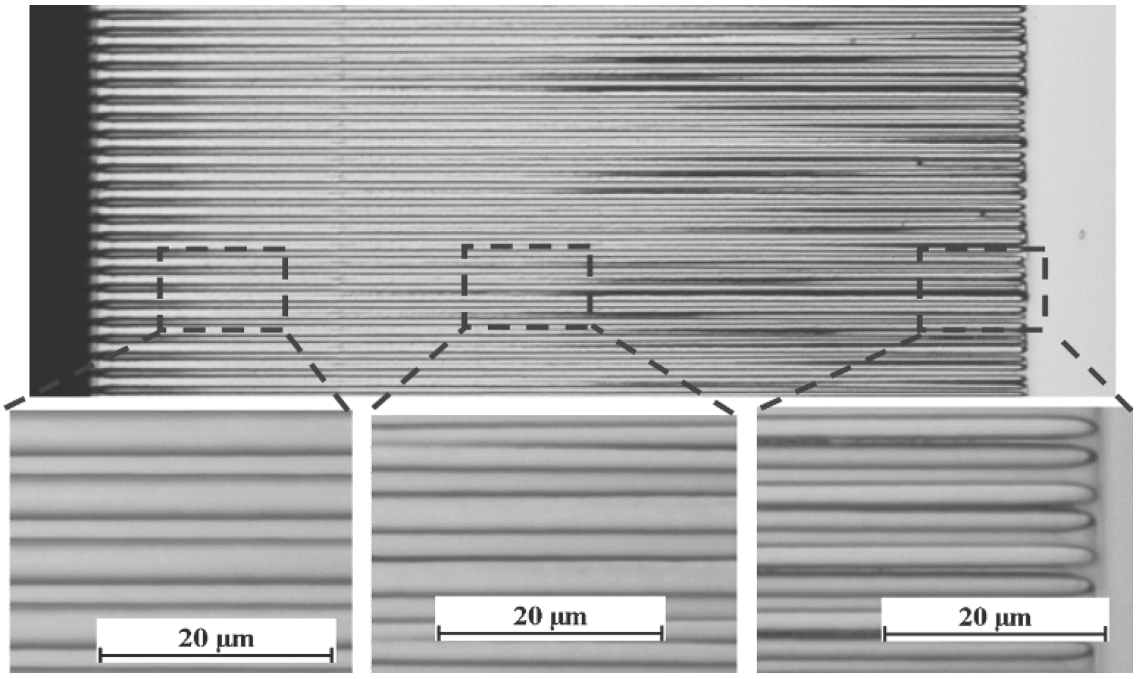
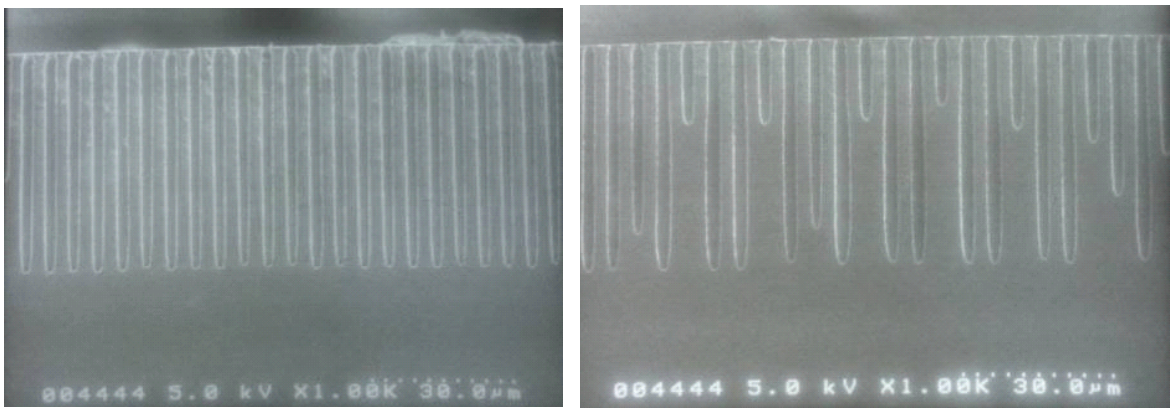


Fig. 5. Metalloscope photographs of the pore profiles etched at a constant voltage.

$$\mathrm{Si} + 4\mathrm{HF}_2^- + \mathrm{h}^+ \rightarrow \mathrm{SiF}_6^{2-} + 2\mathrm{HF} + \mathrm{H}_2 + \mathrm{e}^-. \quad (3)$$

From Eq. (3), the hydrogen gas occurs under the condition of $J < J_{\mathrm{PS}}$. It can be seen from Fig. 7 that the region of non-space-charge will widen as the space charge layer thins in the zone between the pores. So, the number of holes diffusing to the pore wall is significantly increased, the electrochemical reaction on the pore wall is enhanced and the release of hydrogen is increased in the pores. The pore etching will cease gradually and the blind porosity will increase because a large number of



(a) (b)

Fig. 6. SEM photograph of the pore profiles etched at different voltages. (a) 1.5 V. (b) 0.5 V.

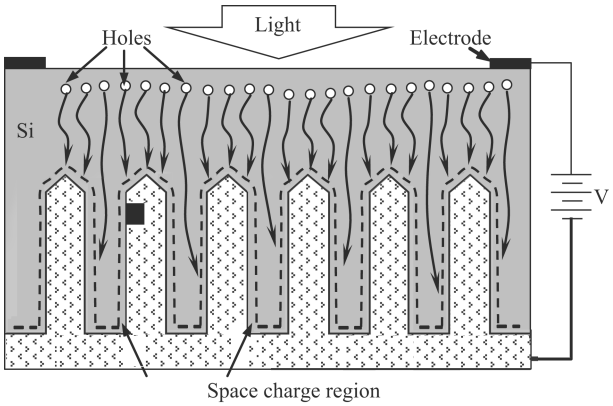


Fig. 7. Macropore formation mechanisms in n-type silicon with PEC etching.

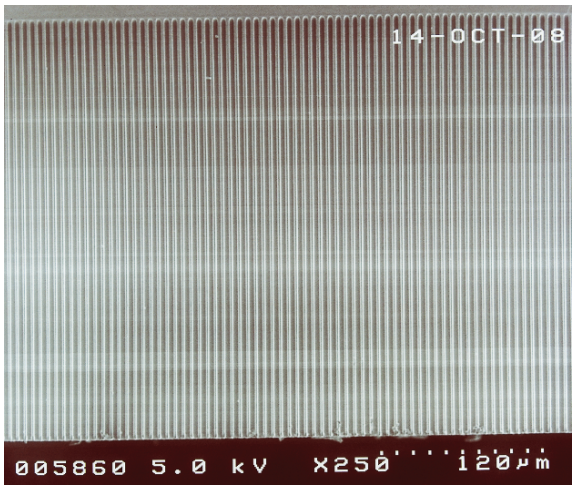


Fig. 8. Profile SEM photograph of MSAs with high aspect ratios.

hydrogen molecules plug the pore. Taking these factors into account, the surfactant (Triton X-100) was added to the etching solutions. The H_2 transport was enhanced and the blind porosity at low etching voltages was reduced.

In summary of this section, the etching voltage plays an important role in determining the cross-section shape of the pore and blind porosity. After process optimization, the perfect MSA structure was fabricated with the etching voltage from 0.8 V down to 0.3 V for 10 h, as shown in Fig. 8. In order to keep the diameter constant, a programmed etching current density was used, which has been described in detail elsewhere[15].

4. Conclusion

The I–V scan curves of the n-type silicon wafer with induced pits in the process of PEC were analyzed. A silicon PEC etching process was carried out at different voltages. The etching voltage played an important role in determining the shape of the pore cross-sections and blind porosity. Increasing the etching voltage led to the distortion of the pore morphology. Decreasing the etching voltage resulted in an increase in the blind porosity. A constant etching voltage for a long time caused gradual bifurcation. Through the optimization of the process parameters, the perfect MSA structure, with a pore depth of 317 μm, a pore size of 3 μm and an aspect ratio of 105, was obtained.

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