A digital calibration technique for an ultra high-speed wide-bandwidth folding and interpolating analog-to-digital converter in 0.18-μm CMOS technology*

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Abstract: A digital calibration technique for an ultra high-speed folding and interpolating analog-to-digital converter in 0.18-μm CMOS technology is presented. The similar digital calibration techniques are taken for high 3-bit flash converter and low 5-bit folding and interpolating converter, which are based on well-designed calibration reference, calibration DAC and comparators. The spice simulation and the measured results show the ADC produces 5.9 ENOB with calibration disabled and 7.2 ENOB with calibration enabled for high-frequency wide-bandwidth analog input.

Key words: ultra high-speed; wide-bandwidth; folding; interpolating; analog-to-digital converter
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1. Introduction

Ultra high-speed and wideband analog-to-digital converters (ADCs) are required in a wide range of receiver applications, including military radar, satellite, communication system, and test instrumentation. Although the flash architecture has the highest speed, it requires 2^N–1 comparators for N bits of resolution, resulting in area and power costs. Folding is a technique to reduce the number of comparators used in the flash architecture, with nearly the same conversion speed as flash. In Ref. [1], Lin proposed a 600 MS/s 6-bit folding and interpolating ADC, which can achieve 5.48 bits of ENOB at 1-MHz input with a 600-MS/s sampling rate. The disadvantage of folding is the larger susceptibility to device mismatch especially when implemented in CMOS technologies, which can be mitigated by digital calibration. Digital calibration techniques have been proved to be efficient for pipeline ADCs[2−4], folding and interpolation ADCs[5] in performance improvement.

This paper proposes a digital calibration technique for an ultra high-speed wide bandwidth folding and interpolation ADC (F&I ADC). The analog input rate can be up to 750 MHz, and sample rates up to 1.5 GSPS. The spice simulation and the measured results show the F&I ADC produces 5.9 ENOB with calibration disabled and 7.2 ENOB with calibration enabled at high frequency analog input.

2. F&I ADC architecture

The system block diagram of the proposed wide bandwidth ultra-high speed F&I ADC system is presented in Fig. 1. The F&I ADC mainly includes clock circuit, calibration resistance ladder, reference block, MUX, sample and hold, high 3-bit flash ADC, low 5-bit F&I ADC, digital encoder, calibration digital logic. The following part will discuss some main circuit components.

2.1. Input MUX

The proposed digital calibration is taken at power on. In order to apply the calibration reference signal, this requires an on-chip analog input MUX circuit, as shown in Fig. 2. The calibration switch SW2, SW3 only switches at the start and end of calibration. The switch is implemented by boostswitch with very low distortion at gigahertz input frequencies, to maintain good Nyquist performance.

2.2. S/H circuit

The function of the S/H circuit is to track/sample the difference analog input signal and to hold that value while subsequent circuitry digitizes it. The proposed S/H circuit employs a pseudo-differential architecture consisting of two single-ended S/H circuits, as shown in Fig. 3. The schematic of each single-ended S/H circuit is similar to the one used in Ref. [2]. To reduce the distortion caused by body effect, a PMOS source follower is used as the buffer. An important feature of this architecture is that it uses two interleaved track and hold (T/H) circuits operating at half of the sampling frequency. These are used in a time-interleaved manner to achieve one S/H function.

2.3. LOW 5-bit F&I ADC

Low 5-bit conversion is implemented by a folding and interpolation ADC. The input is a different volt signal from

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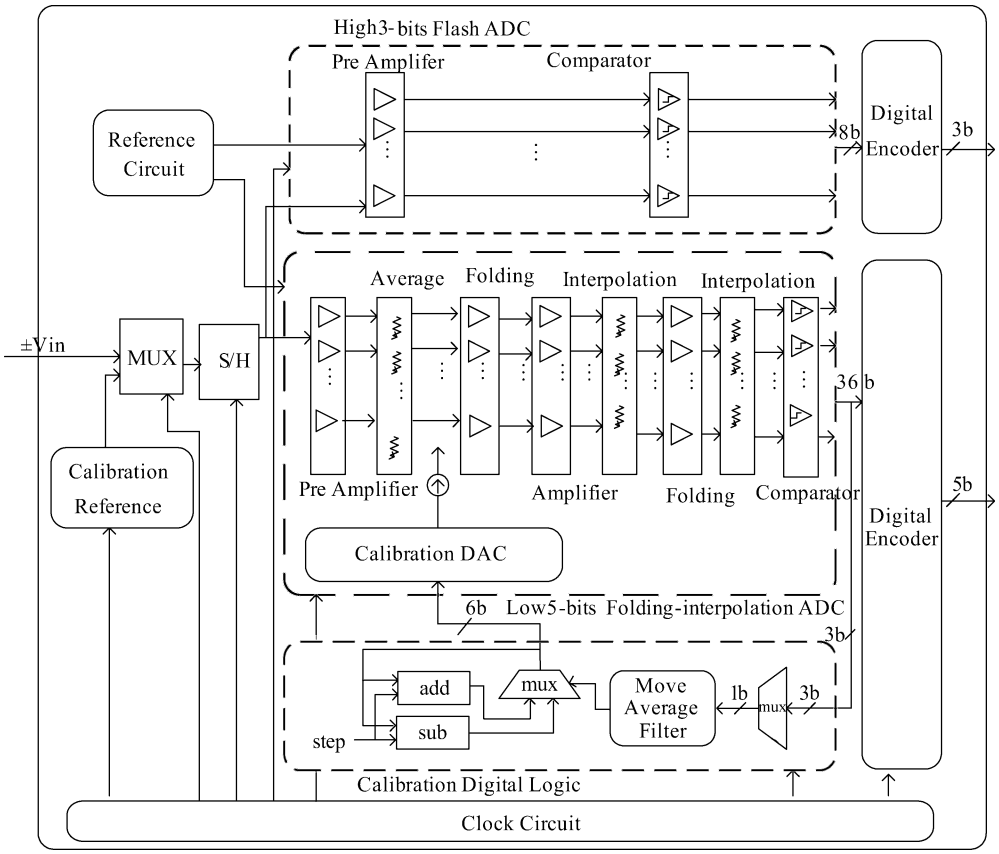

Fig. 1. Architecture of the ADC.

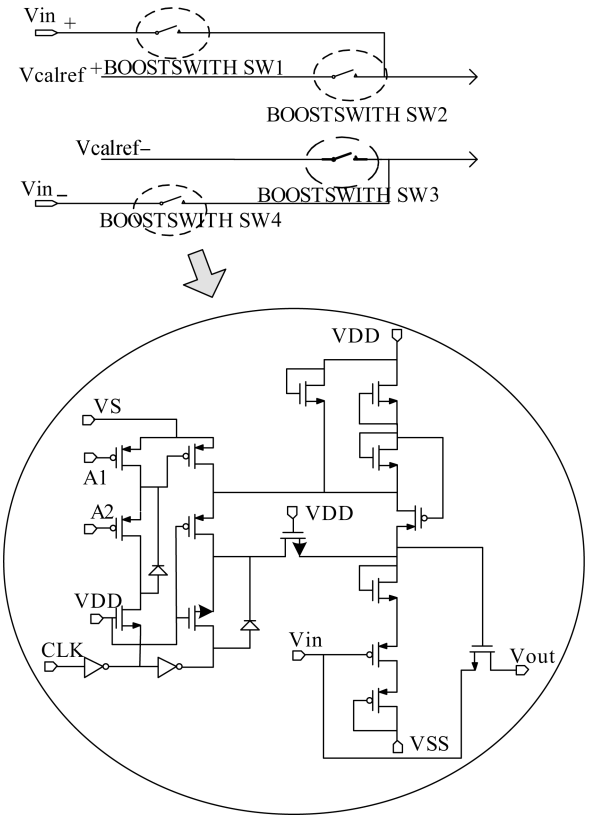

Fig. 2. Input Mux.

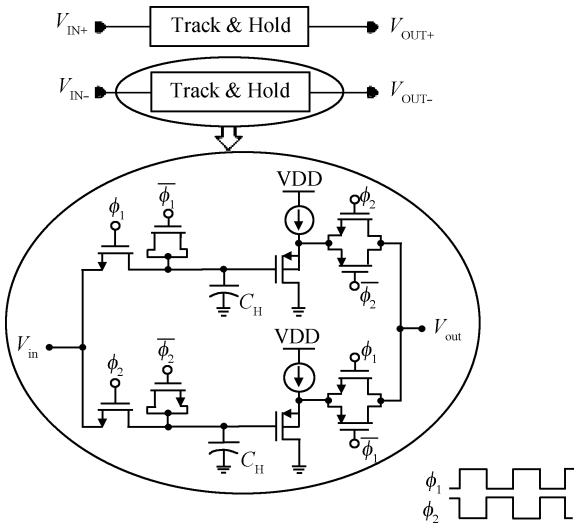

Fig. 3. S/H circuit.

the sample and hold block. The F&I ADC include 29 pre-amplifiers, average resistance array, 9 first-stage folding amplifies, 9 operational amplifiers, the first 3x interpolation resistance array, 9 second-stage folding amplifiers, the second-stage 4x interpolation resistance array and 36 comparators. Folding amplifiers[6] built with differential pairs have input–output transfer characteristics resembling a sinusoidal signal, which schematic is shown in Fig. 4, similar to the one used in Ref. [5].

In spice simulation transient analysis, the different analog

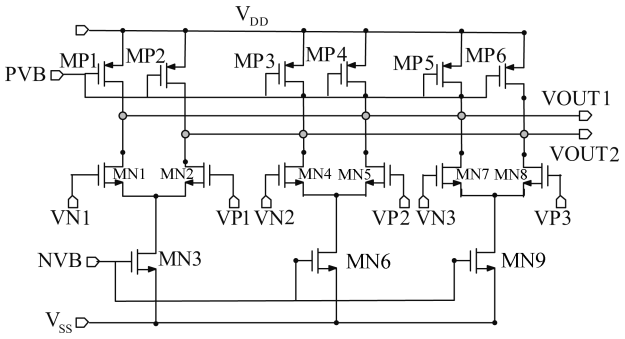

Fig. 4. Folding amplifier schematic.

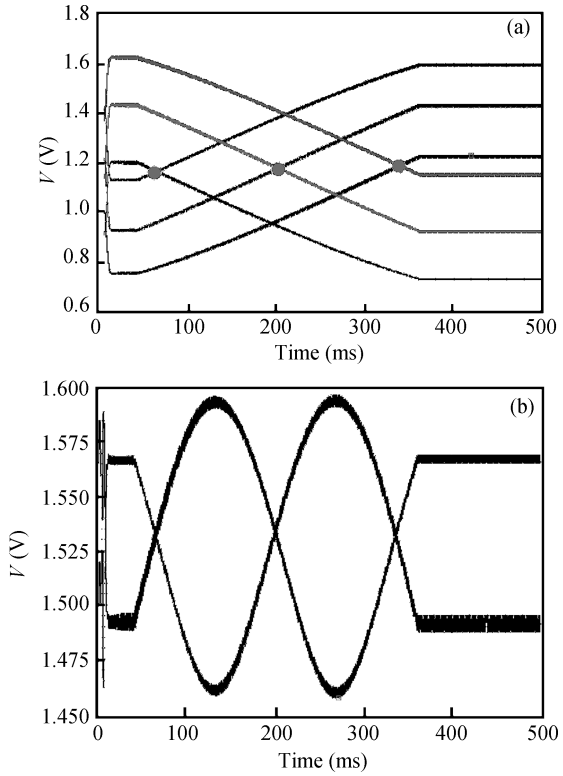

Fig. 5. Spice simulation waveform for folding amplifier. (a) Input waveform. (b) Output waveform.

input to folding amplifier is shown in Fig. 5. There are three common-mode cross points. The output of folding amplifier is shown in Fig. 5 as a different sinusoidal signal.

2.4. Encoder LOGIC

The code generated by the comparator bank in the high 3-bits flash A/D converter is thermometer code. Due to the folding and interpolating, the output code comparator bank in the low 5-bits folding and interpolation A/D converter is not thermometer code but cyclical thermometer code[7]. Cyclical thermometer code can be converted to gray code through pure XOR operation, as shown in Fig. 6.

The gray code is also converted to binary code through pure XOR operation, as shown in Fig. 7.

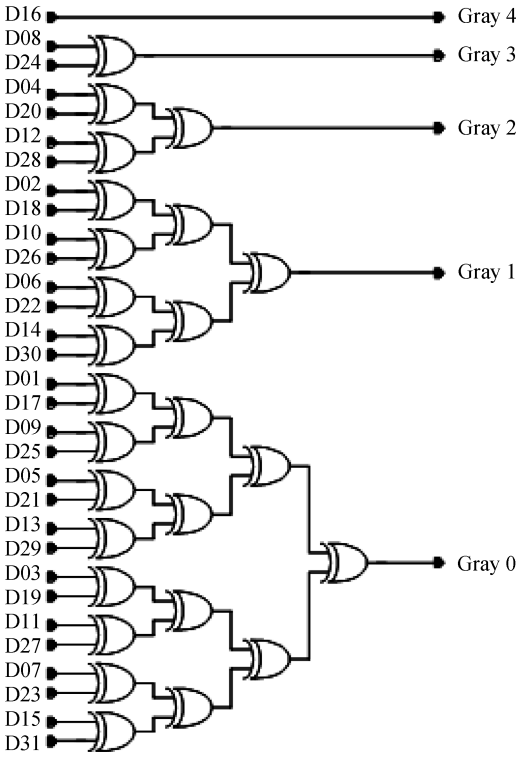

Fig. 6. Cyclical to gray code conversion.

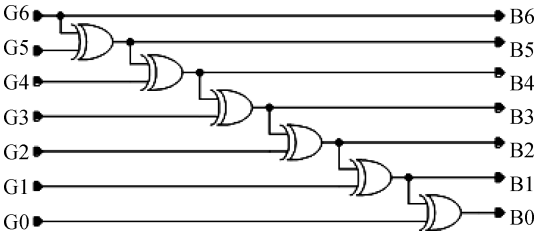

Fig. 7. Gray to binary code conversion.

3. Digital calibration technique

3.1. High 3-bit flash converter digital calibration

The digital calibration schematic for the high 3-bit flash converter is shown in Fig. 8, which mainly includes calibration circuit, converter digital encoder and calibration controller.

The calibration flow is shown in Fig. 9.

After power-on, the calibration controller selects the calibration reference voltage. Next the comparator output will be latched. The decision will be made as to whether the comparator output corresponds to logic 0. If not, the counter value will be decreased by 1, otherwise, the counter value will be increased by 1. The counter value will be sent to DAC block to decrease or increase the adjust voltage to operational amplifier. The operational amplifier schematic is shown in Fig. 10, where load $R_1 = R_2$. The DAC output is coupled to amplifier in a different manner. The differential output voltage is determined according to signals Vinp, Vrefp, Vinn, Verfn, and is further modified by DAC output to adjust for offset error.

With added offset to the flash converter schematic, the spice simulation waveform is shown in Fig. 11. It shows the

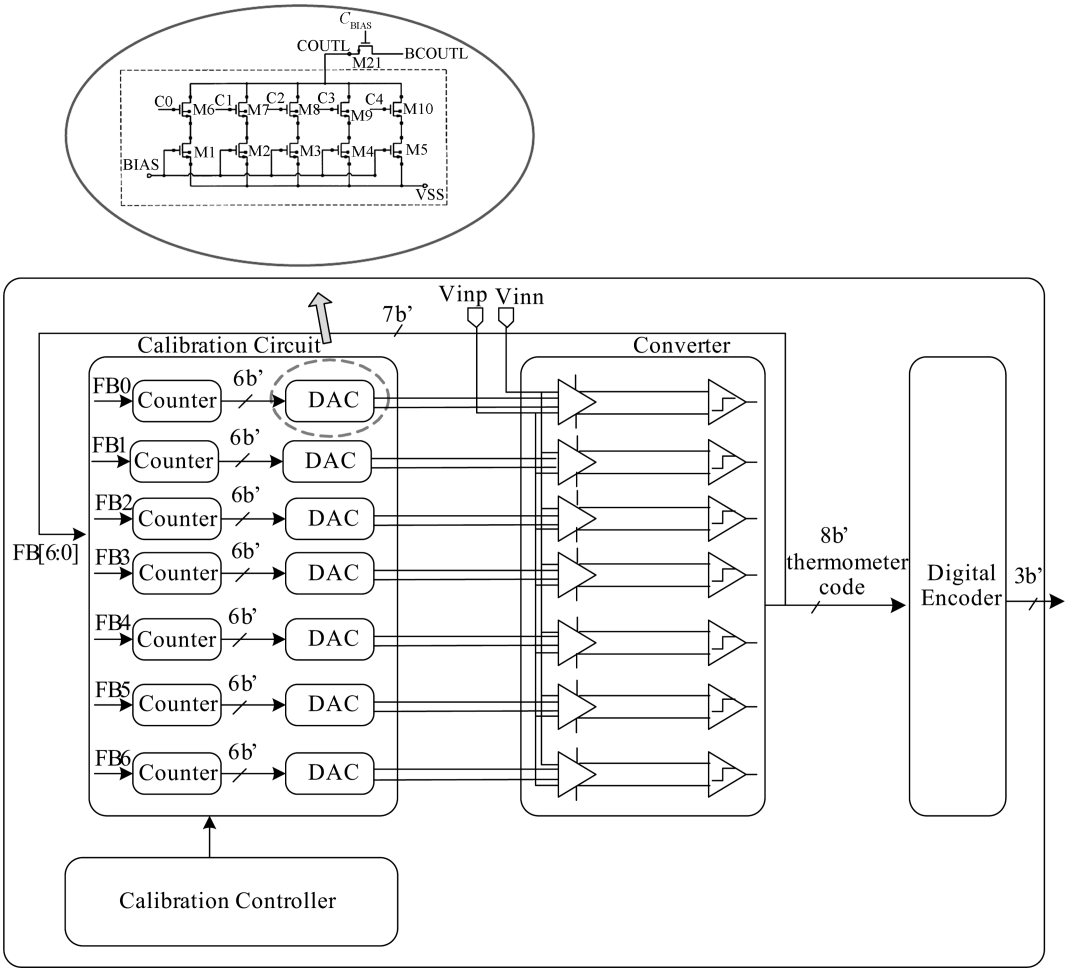

Fig. 8. Calibration schematic for flash converter.

proposed calibration technique can adjust the offset. Although offset error can result from multiple components, such as S/H circuit, voltage reference ladder, amplifier array, comparator, and mismatch in resistor values and current mirror ratios, the total offset error may be corrected at one point in the chain of components.

3.2. Low 5-bit F&I ADC digital calibration

Except the digital calibration to flash converter, we also take digital calibration for the low 5-bit F&I converter. Figure 12 shows the simple block diagram of the core of the folding A/D converter. It includes pre-amplifiers, folding amplifier and comparator.

Their outputs are illustrated in Fig. 13(a) with input voltage V_{in} increasing ideally, where V_{ref1}, V_{ref2}, V_{ref3} are precisely spaced voltages. Due to the non-ideality of the input MUX, sample/hold circuit and pre-amplifier, such as offset, non-linearity, gain error, the differential output zero cross of the pre-amplifier is not consistent to the differential reference voltage, resulting in the offset. The output is shown in Fig. 13(b). The output C of the comparator will send to digital encoder. The value deviating from ideal makes the DNL and INL worse, especially INL.

To improve the linearity of the ADC, digital calibration is introduced. The zero-crossings of the comparators are controlled by the zero-crossings of pre-amplifiers, where V_{in} equals to the reference voltage on ideal conditions. We can force the pre-amplifiers' input equal to the reference voltage, and add extra calibration voltages whose value can be changed to be the same as the outputs of the pre-amplifiers.

According to the feedback digital codes of the F&I ADC comparators, the calibration circuit changes the value of the extra calibration voltage, moves the zero-crossings of the pre-amplifiers, to move the comparator's zero-crossing to the reference voltages. The extra voltage is implemented by a small current DAC and a resistance, as illustrated in Fig. 14.

As show in Fig. 1, the calibration circuit consists of the clock block, calibration reference block and digital calibration circuit. The clock block can generate 23 calibration clocks with certain phase relation to open calibration references. Each calibration clock includes 16 short cycles and 4 long cycles, as shown in Fig. 15. The calibration reference block includes bandgap reference circuit, calibration resistor ladder and switches that are arranged to provide a plurality of precisely 23 spaced calibration voltages based on 23 calibration clocks. The calibration resistor ladder includes a plurality of precisely matched resistors to provide 23 spaced calibration voltages.

The digital calibration logic (shown in Fig. 16) includes moving-average filter, 6-bit adder, 6-bit subtracter, MUX and control logic. The calibration flow is shown in Fig. 16, where V_{cal_i} is the i calibration reference voltage, where i =1, 2, …, 23. The d_{DAC_i} is the i 6-bits DAC controlling code with initial

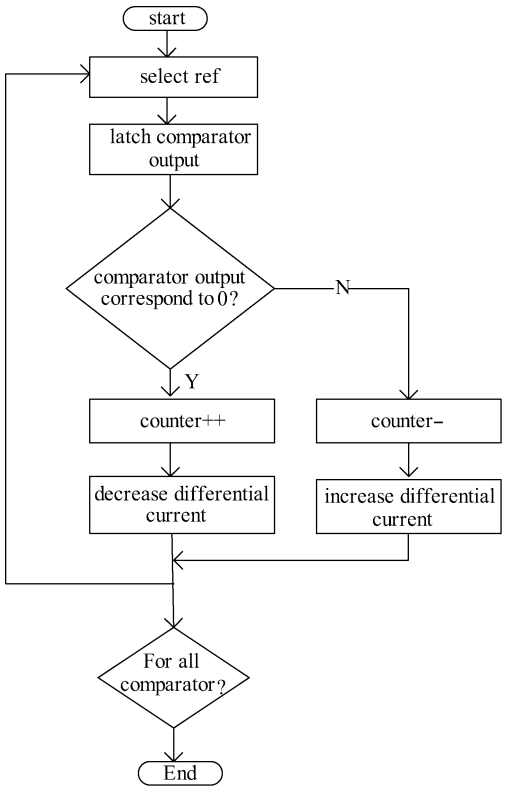

Fig. 9. Calibration flow for flash converter.

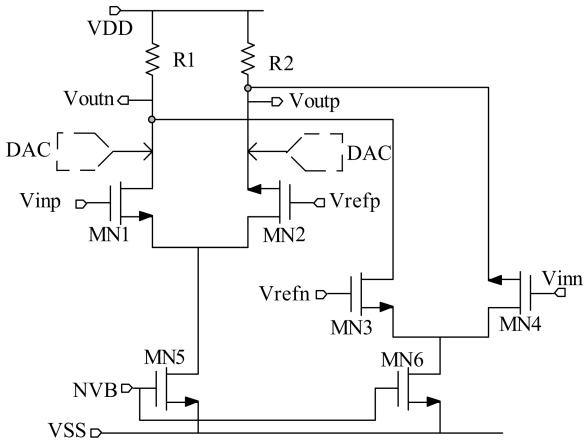

Fig. 10. Schematic of the operation amplifier.

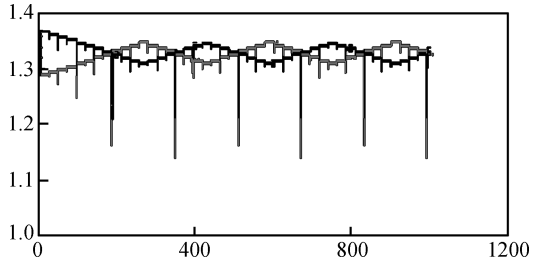

Fig. 11. Spice simulation waveform.

value 100000.

The C_y is the comparator y's output. The relation between pre amplifier (i) with calibration feedback signal (y) is shown

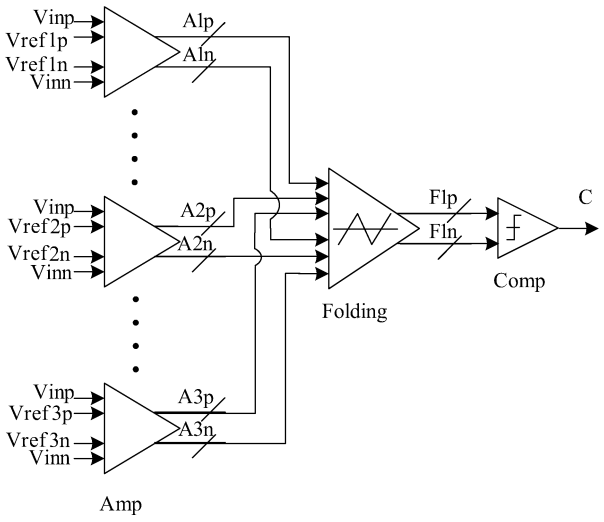

Fig. 12. Reduced model for F&I ADC.

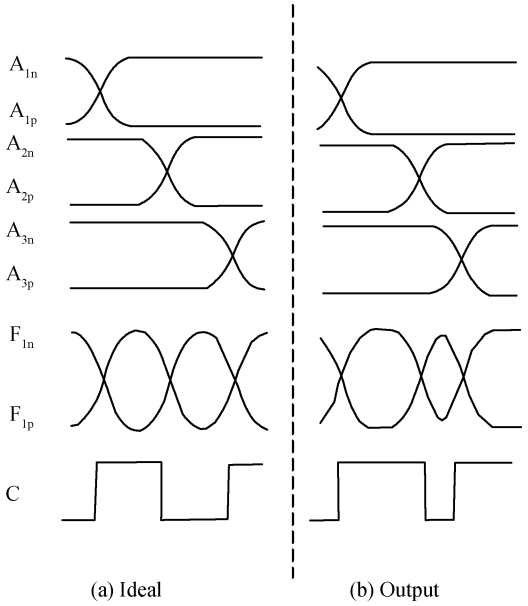

Fig. 13. Ideal and non-ideal outputs for F&I ADC.

Table 1. Relation between pre-amplifier with calibration feedback signal.

i	y
1, 4, 7, 10, 13, 16, 19, 22	12
2, 5, 8, 11, 14, 17, 20, 23	24
3, 6, 9, 12, 15, 18, 21	36

in Table 1.

The step is the changing-step value of adder and subtracter. The calibration process is controlled by calibration counter with initial value 0. After every calibration cycle finished, the counter's value is increased by 1. When counter's value equals to 20, calibration control logic shuts down all calibration clock. The whole calibration process is over and ADC switches to normal operation mode. In the every calibration cycle of the 20 calibration cycles, the step value of the d_{DAC_i} is gradually decreased, as shown in Table 2.

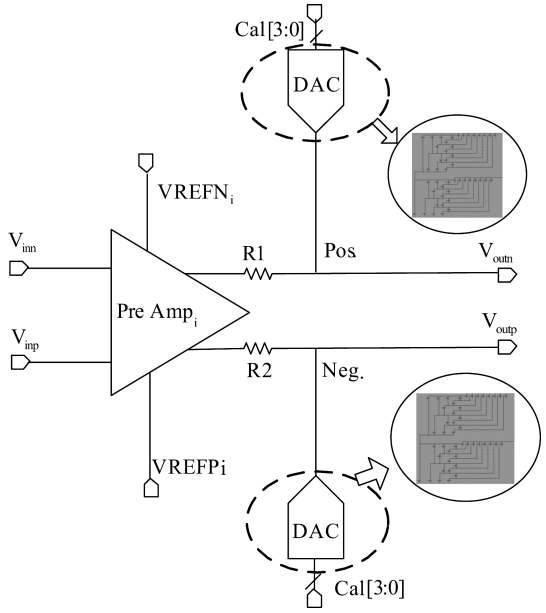

Fig. 14. Model of digital calibration.

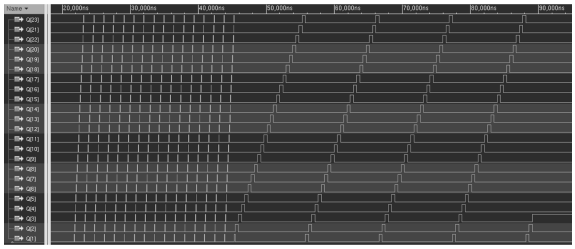

Fig. 15. 24 clock phase relation to open calibration reference voltages.

Table 2. Step value with calibration clock cycles.

Calibration clock cycle	Adder/subtracter step value
1，2，3，4	8
5，6，7，8	4
9，10，11，12	2
13，14，15，16，17，18，19，20	1

During every calibration cycle, the analog input is broken off and the calibration reference voltage is attached to the S/H circuit, which is configured to receive reference voltage during calibration. The F&I ADC will convert the calibration reference voltage to digital code. The comparator's output C_y will be filtered by the move average filter. If the output of the filter is 1, the d_{DAC_i} will be subtracted by step value. If the output of the filter is 0, the d_{DAC_i} will be added by step value. Then the next calibration reference voltage will be sampled by S/H circuit and take the calibration process for the next pre-amplifier until all the 23 comparators are calibrated. The relation between d_{DAC_i} codes and DAC output current is shown in Table 3. There are three points to be careful of. One is to reverse the output of the filter when calibrating even pre-amplifier. This is because of the folding characteristic of the F&I ADC. The second is overflow problem of the adder and subtracter. The output of the adder can be forced to be all 1 and the output of the subtracter can be forced to be all 0 when overflow happened. The third is that only high 4-bits output from counter

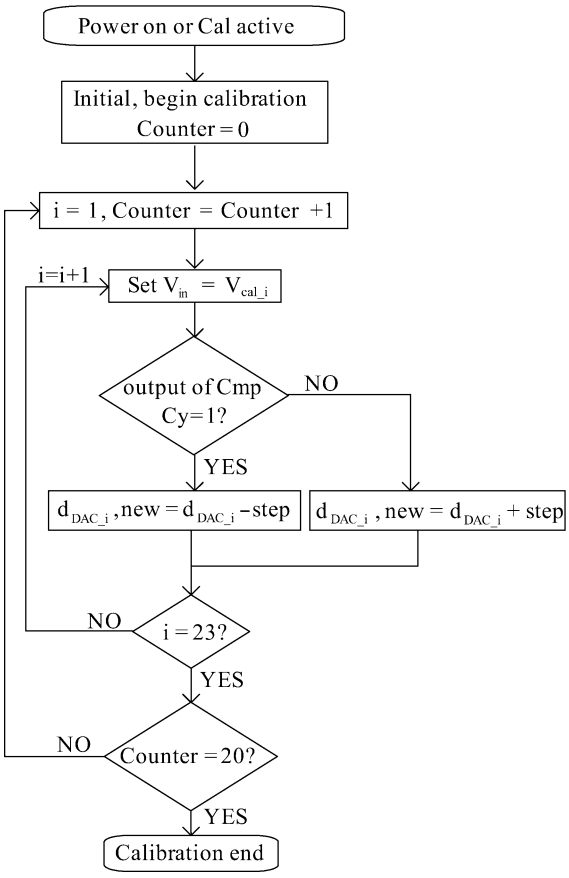

Fig. 16. Calibration flow.

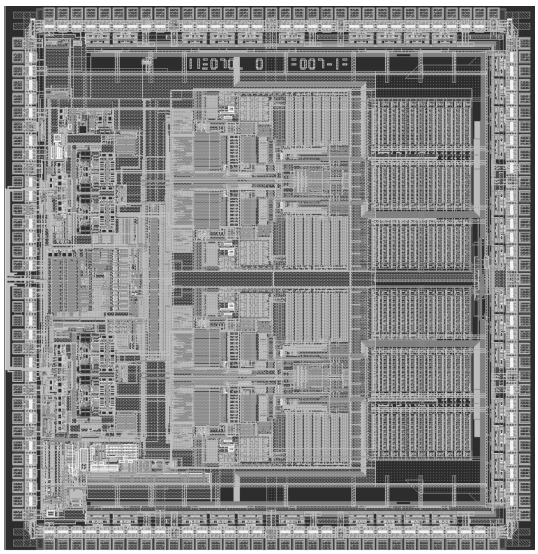

Fig. 17. Die of the ADC.

are used to generate calibration voltage by calibration DAC.

4. Design verification

The ultra high-speed ADC is designed in 0.18-μm CMOS technology. The area of die is 4.270 × 4.104 mm^2, shown in Fig. 17.

The frequency of the different analog input is up to be

Table 3. Relation between calibration current injecting to pre-amplifier output and calibration digital logic output codes.

d_{DAC_i}	Pos.	Neg.	d_{DAC_i}	Pos.	Neg.
0000	0	15I	1000	8I	7I
0001	1I	14I	1001	9I	6I
0010	2I	13I	1010	10I	5I
0011	3I	12I	1011	11I	4I
0100	4I	11I	1100	12I	3I
0101	5I	10I	1101	13I	2I
0110	6I	9I	1110	14I	1I
0111	7I	8I	1111	15I	0

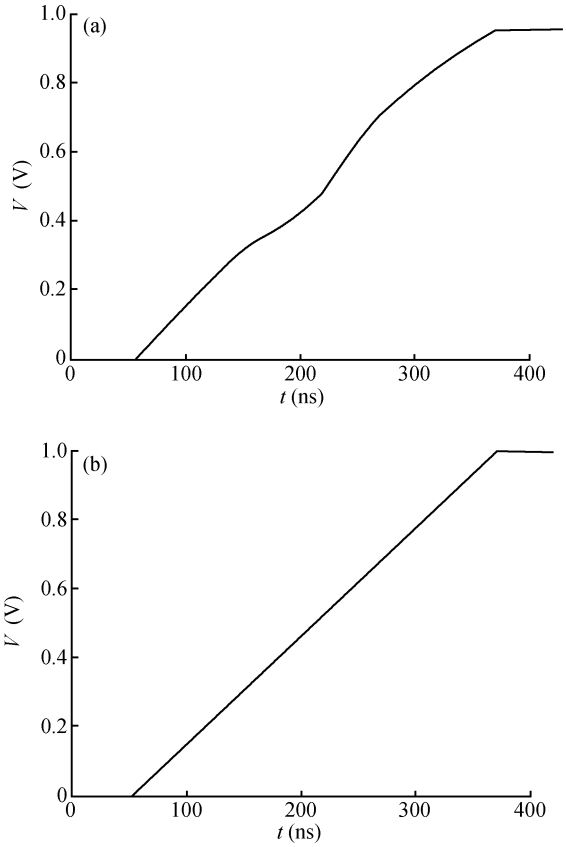

Fig. 18. Spice simulation results. (a) ADC output with calibration disabled. (b) ADC output with calibration enabled.

750 MHz and sample frequency 1.5 GSPS for the ADC. When adding some offset to the circuit, the spice simulation result with calibration disabled is shown in Fig. 18(a) of reconstructed slope analog input by ideal DAC. With calibration enabled, the simulation result is shown in Fig. 18(b). The linearity is greatly improved.

The test board is shown in Fig. 19.

The measured ADC electrical characteristics are shown in Table 4.

Figure 20 shows the differential nonlinearity (DNL$< \pm 0.5$ LSB) and integral nonlinearity (INL $< \pm$ 0.5) at 373 MHz analog input and 1.5 GSPS sample frequency.

Figure 21 shows the output spectrum of the reconstructed analog signal from ADC output by DAC. The SFDR is 60.5 dB, the SNR is 47 dB, and the ENOB is 7.4 bits at $F_{in} = 373$ MHz, $F_s = 1.5$ GSPS.

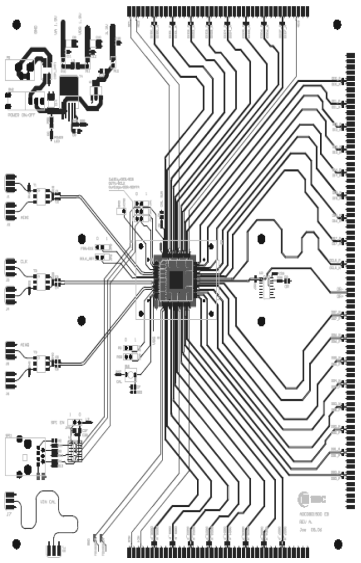

Fig. 19. Evaluation board for the F&I ADC.

Table 4. ADC electrical characteristics.

Parameter	Min	Typical	Max
Static characteristic			
INL (LSB)	–0.4		+0.31
DNL (LSB)	–0.21		+0.28
Offset error (LSB)		–0.43	
Analog input parameter			
V_{CMO} common mode output voltage (V)		1.23	
V_{bg} output voltage (V)		1.27	
Power output' parameter			
Analog input current, I_A (mA)		680	
PD = PDQ = Low			
PD = Low' PDQ = High		490	
PD = PDQ = High		1.5	
Digital driven current, I_{DR} (mA)			
PD = PDQ = Low		209	
PD = Low PDQ = High		125	
PD = PDQ = High		0.02	
Power P_D (mW) PD = PDQ = Low		1700	
PD = Low PDQ = High		11700	
PD = PDQ = High		2.9	
Dynamic characteristic (Normal mode)			
ENOB (bit) $F_{in} = 373$ MHz		7.4	
SINAD (dB) $F_{in} = 373$ MHz		46.5	
SNR (dB) $F_{in} = 373$ MHz	10	46.9	
THD (dB) $F_{in} = 373$ MHz		–57	
2nd Harm (dB) $F_{in} = 373$ MHz		–64	
3nd Harm (dB) $F_{in} = 373$ MHz		–60	
SFDR (dB) $F_{in} = 373$ MHz		60.5	

5. Conclusion

This paper proposed a digital calibration technique for an ultra high-speed wide-bandwidth folding and interpolating ADC. The chip is processed in 0.18-μm CMOS technology. The measured results show that the digital calibration technique can efficiently improve the F&I ADC characteristics, even at Nyquist.

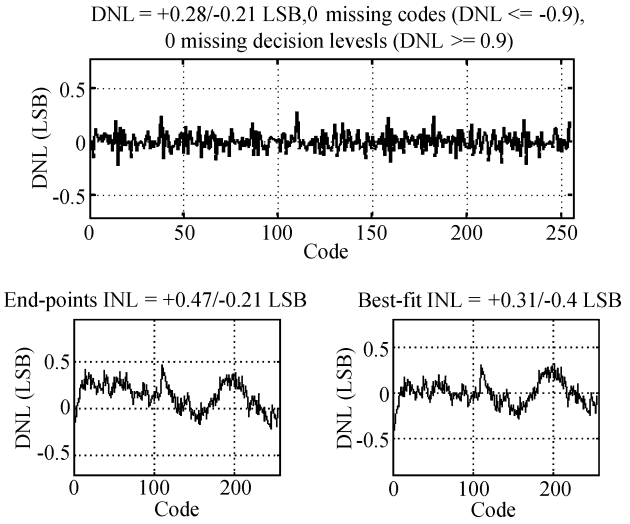

Fig. 20. DNL and INL at $F_{\text{in}} = 373$ MHz, $F_{\text{s}} = 1.5$ GSPS.

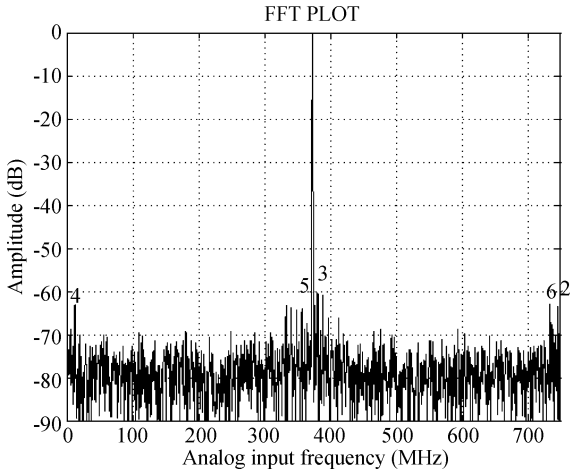

Fig. 21. SFDR at $F_{\text{in}} = 373$ MHz, $F_{\text{s}} = 1.5$ GSPS.

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