A 10-bit 50-MS/s subsampling pipelined ADC based on SMDAC and opamp sharing

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Abstract: This paper describes a 10-bit, 50-MS/s pipelined A/D converter (ADC) with proposed area- and power-efficient architecture. The conventional dedicated sample-hold-amplifier (SHA) is eliminated and the matching requirement between the first multiplying digital-to-analog converter (MDAC) and sub-ADC is also avoided by using the SHA merged with the first MDAC (SMDAC) architecture, which features low power and stabilization. Further reduction of power and area is achieved by sharing an opamp between two successive pipelined stages, in which the effect of opamp offset and crosstalk between stages is decreased. So the 10-bit pipelined ADC is realized using just four opamps. The ADC demonstrates a maximum signal-to-noise distortion ratio and spurious free dynamic range of 52.67 dB and 59.44 dB, respectively, with a Nyquist input at full sampling rate. Constant dynamic performance for input frequencies up to 49.7 MHz, which is the twofold Nyquist rate, is achieved at 50 MS/s. The ADC prototype only occupies an active area of 1.81 mm^2 in a 0.35 μm CMOS process, and consumes 133 mW when sampling at 50 MHz from a 3.3-V power supply.

Key words: analog-to-digital converter; pipelined; SMDAC; opamp-sharing
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1. Introduction

Many applications, ranging from wireless communication to digital TVs, call for 10-bit analog-to-digital converters (ADCs) sampling at around 50 MHz. Most of them require low power consumption as well as a small die area, and many of them also require high dynamic performance for Nyquist input frequencies or higher. It is a difficult task to achieve good dynamic performance for high input frequencies.

To ensure the first MDAC and sub-ADC see the same input, a front-end sample-hold-amplifier (SHA) is commonly used before the first pipelined stage. Since an SHA would be required to have a noise floor and distortion lower than that of the pipelined ADC following it, the power and area are increased by using a SHA. The dedicated SHA can be avoided by the methods that follow. One method is to eliminate the SHA directly. The aperture error caused by the mismatch between the first MDAC and the sub-flash ADC can be minimized by carefully matching the RC delays between them[1,2]. However, the aperture error increases with input frequency, so the ADC's maximum input frequency is limited. Thus the method is not suitable for subsampling applications. Another method is to merge the SHA with the first MDAC (SMDAC). Thus the SHA function is reserved and aperture error is avoided. However, the opamp would work in two closed loops and the feedback factors are different[3,4]. The stability of the closed loops should be optimized carefully. In this paper, the feedback factors are the same through choosing the appropriate SHA and MDAC, so the stability can easily be met in both closed loops.

In this paper, a 3.3 V 10-bit 50 MS/s pipelined ADC with a SMDAC is demonstrated, which can be used for subsampling applications. Sharing an opamp between two successive pipeline stages reduces the power and area further. This paper also describes the proposed architecture for 10-bit pipelined ADC, which is realized using just four opamps. Details of the circuit implementation are presented, followed by the measured results.

2. Proposed ADC architecture

The proposed pipelined ADC architecture is shown in Fig. 1. It consists of clock generator, a bandgap, an SMDAC, three 1.5 bit opamp-sharing stages, a 3-bit flash ADC and a digital correct. The clock generator supplies seven clock signals to make the ADC operate at different stations, as depicted in Fig. 2.

The bandgap provides bias current for every stage. The 2-bit digital outputs from each stage are added together with one bit overlapped between adjacent stages in a digital correction block. Thus the 17 bits turn to 10 bits at the output of the ADC.

3. Circuit design of the ADC

3.1. SMDAC

A front-end SHA is widely used in high speed ADCs because it minimizes the aperture error caused by the sampled signal mismatch between the first MDAC and the comparators of the sub-flash ADC in the first stage. To save power dissipation and area occupation, the dedicated SHA and the first MDAC are replaced by means of the following SMDAC without degrading the ADC's performance.

Figure 3 shows a schematic of the SMDAC, which works in three clock phases[3]: PSA/PSAP, PD and PH. During the PSA/PSAP phase, V_{in} is sampled on C_s. The bootstrapped

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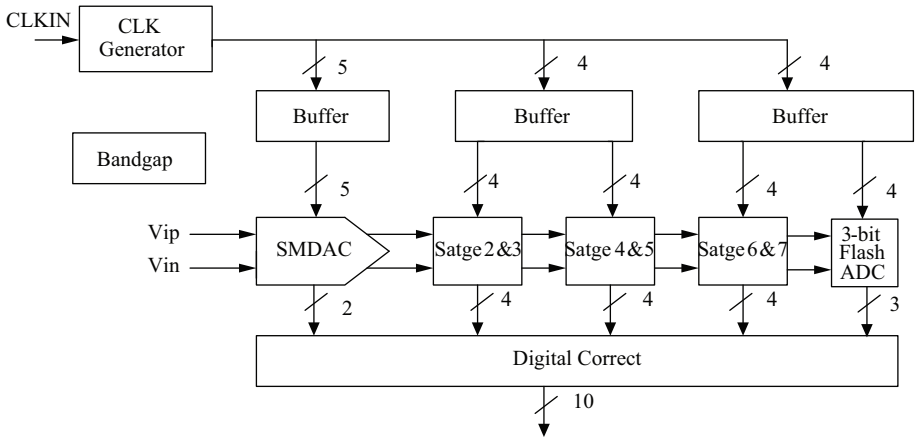

Fig. 1. Proposed ADC architecture.

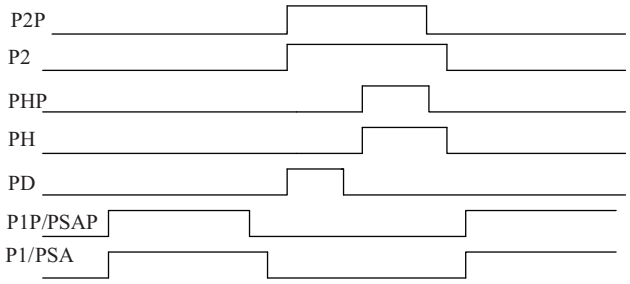

Fig. 2. Timing diagram of the ADC.

switches are employed to minimize the nonlinear distortion of the sampled inputs due to switch on resistance variations while sampling[4, 5]. During the PD phase, the opamp and C_{fs}, C_{ff} are discharged and C_s holds the input value. During the PH phase, the opamp, C_s and C_{fs}, C_{ff} turn to "charge transform" architecture SHA, the sampled charge on C_s is transformed to C_{fs}, C_{ff}. C_s is set to $2C_{fs}$ and $2C_{ff}$, V_{out} is equal to V_{in} and connects with the comparators in the sub-ADC. So, C_{fs} and C_{ff} hold the input information. During the PSA/PSAP phase again, C_s samples the next input, C_{ff} overrides the opamp and C_{fs} is connected to $\pm V_{ref}$ or 0, depending on the decision from sub-ADC. The opamp and C_{fs}, C_{ff} are changed to MDAC architecture to generate the residual for the next stage.

Two points should be noticed in the SMDAC architecture. First, during the hold phase, the outputs of the opamp do not connect with C_s of the next stage, so the total load of the opamp is less when compared with the traditional SHA. The total load of the opamp is

$$C_L = (1-\beta)C_f + C_{s\_next} + C_{com} + C_{out} + C_{cmfb}, \quad (1)$$

where β is the feedback factor, C_{s_next} is the sampling capacitor of next stage, C_{com} is the total capacitor of comparators in sub-ADC, C_{out} is the parasitic capacitance of the opamp output and C_{cmfb} is the capacitance of common-mode feedback circuit. In this design, $\beta = 0.5$, $C_f = 1.6$ pF, $C_{com} = 0.4$ pF, $C_{out}, C_{cmfb} = 0.4$ pF. If a conservative scaling ratio of 0.75 is applied from one stage to the next, $C_{s\_next} = 1.2375$ pF. So the total load is 40% less than that of the traditional SHA in this design, and the power consumption can be reduced. Second, the opamp works in two closed loops, and both feedback factors are 0.5, so the opamp can achieve fast-setting in each closed loop.

The designed SMDAC can complete the same function and save an opamp compared with the SHA and the first MDAC architecture. The SMDAC has the same feedback factors during two closed loops. Compared with other SMDAC architectures, which adopt "flip-around" SHA[3] or multi-bits/stage[4] and have different feedback factors in two closed loops, the designed SMDAC has better stability in both closed loops.

3.2. Opamp sharing

The successive stages in a pipelined ADC always work in different states. The opamp takes only half a clock cycle during the amplification state. Thus, one opamp can be shared between two consecutive pipelined stages by adding more switches, thereby significantly reducing the power consumption and the die area.

There are two drawbacks with the opamp sharing technique. First, the offset voltage of the opamp cannot be cancelled because the opamp is always in active mode. Second, there is a crosstalk path between the two stages through the switches connecting with the input nodes of the opamp, such as switches sw1–sw4 shown in the ellipses of Fig. 4. So, the signal fidelity of one stage will be influenced by the other one.

The first drawback is analyzed as follows[6]. Considering finite opamp gain and offset voltage, the output of the first stage is given by[7]

$$\begin{aligned} V_{out} &= \frac{\left(1+\frac{C_s}{C_f}\right)V_{in} - D\frac{C_s}{C_f}V_{ref} + \left(1+\frac{C_s+C_p}{C_f}\right)V_{os}}{1+\frac{C_s+C_f+C_p}{AC_f}} \\ &\approx 2V_{in} \pm DV_{ref} + \frac{A}{1+A\beta}V_{os}, \end{aligned} \quad (2)$$

where β is the feedback factor $\beta = \frac{C_f}{C_s+C_f+C_p}$, A is the gain of the opamp and V_{os} is the offset voltage. The offset voltage amplified by $A/(1+A\beta)$ becomes a constant offset of the output voltage. The output of the second stage output is given by

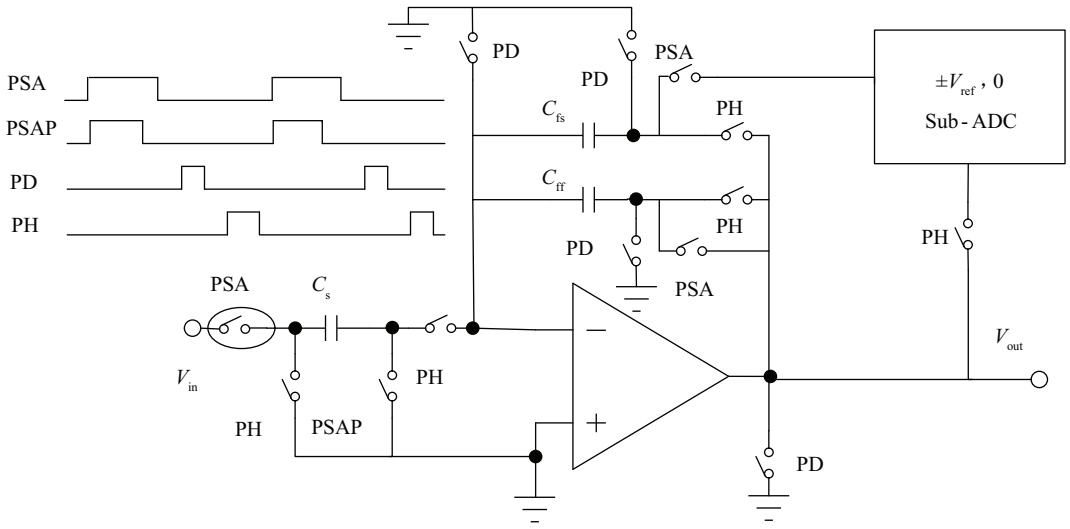

Fig. 3. Schematic of the SMDAC.s

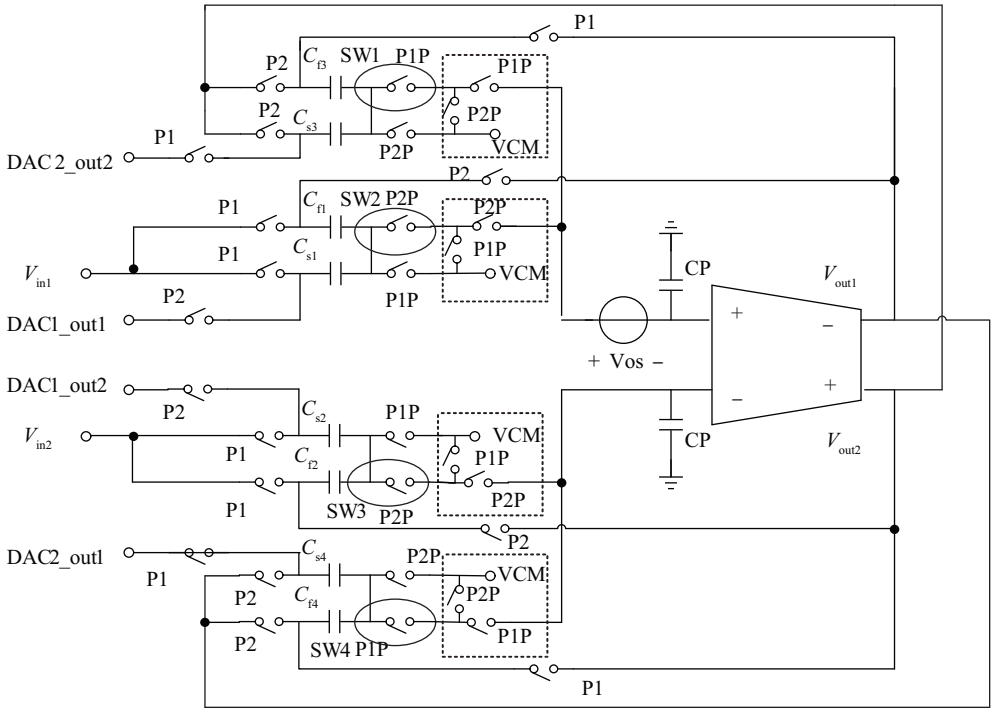

Fig. 4. Schematic of opamp sharing.

$$V_{out} = 2\left(2V_{in} \pm DV_{ref} + \frac{A}{1+A\beta}V_{os}\right) \pm DV_{ref} + \frac{A}{1+A\beta}V_{os} = 2\left(2V_{in} \pm DV_{ref}\right) \pm DV_{ref} + 3\frac{A}{1+A\beta}V_{os}. \quad (3)$$

The effect of offset is $3\dfrac{A}{1+A\beta}V_{os}$, which can be alleviated by the following method. The output of the first stage is connected to the input of the second stage with reverse polarity, as shown in Fig. 4. Thus, the output of the second stage output can be expressed as

$$V_{out} = -2\left(2V_{in} \pm DV_{ref} + \frac{A}{1+A\beta}V_{os}\right) \pm DV_{ref} + \frac{A}{1+A\beta}V_{os} = -2\left(2V_{in} \pm DV_{ref}\right) \pm DV_{ref} - \frac{A}{1+A\beta}V_{os}. \quad (4)$$

So the effect of the offset is decreased to one third. The second drawback can be solved by introducing additional switches, shown in the dashed boxes of Fig. 4. The two successive stages are isolated further by the additional switches, so the crosstalk is mitigated[4]. The controlling signals of additional switches are P1P and P2P, which already exist in the

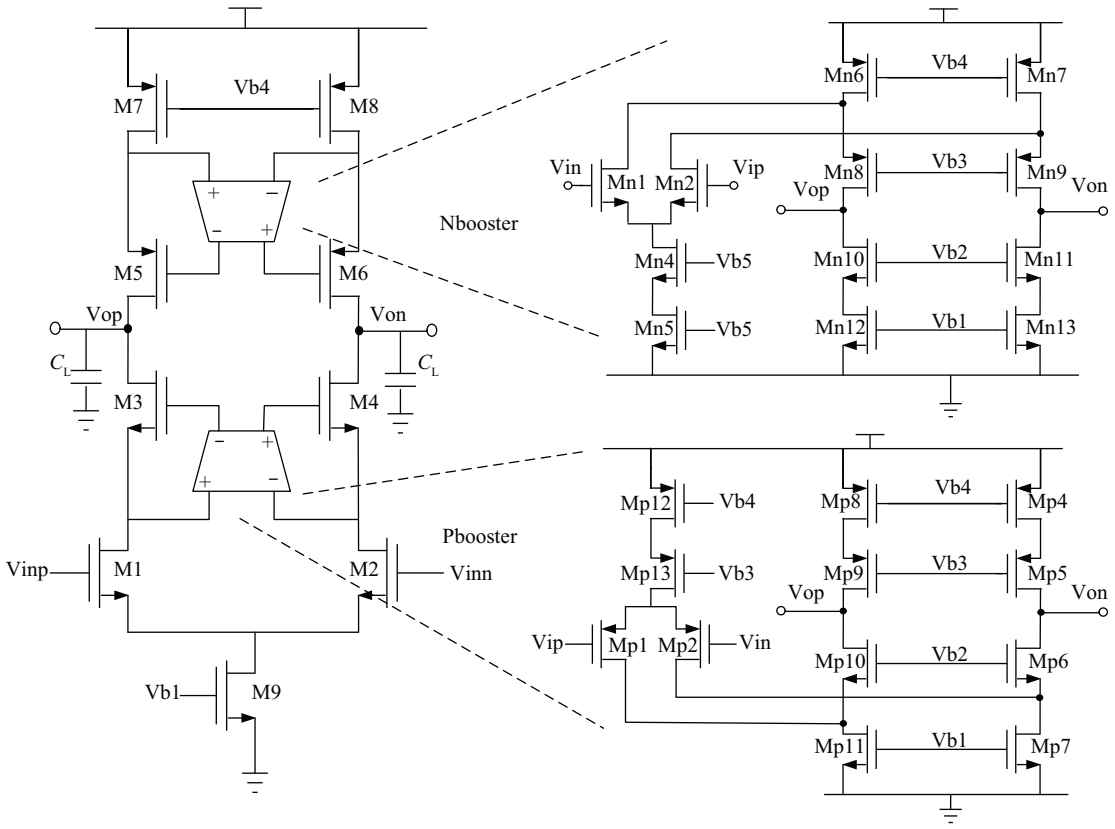

Fig. 5. Schematic of the opamp.

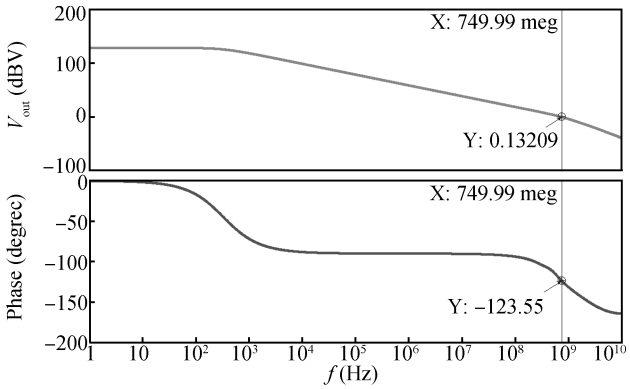

Fig. 6. Simulated frequency response of the amplifier.

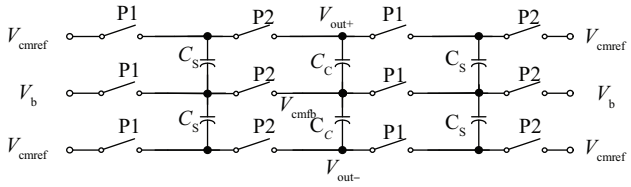

Fig. 7. Common-mode feedback circuit.

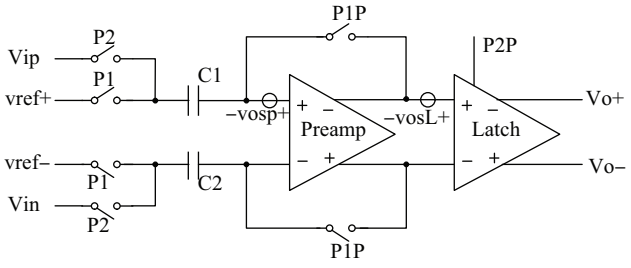

Fig. 8. Schematic of the comparator.

ADC and don't increase the implementation complexity.

3.3. Opamp

A telescopic opamp offers excellent bandwidth with less power consumption at the cost of reduced signal swing range compared with other types of opamps[6]. In order to acquire a high gain with high bandwidth, the gain-boosted telescopic opamp is used in this design, as shown in Fig. 5. The poles and zeros in the transfer function are optimized, so the opamp achieves fast settling in the transient response[8, 9]. The 2 Vp-p differential dynamic range is required under a 3.3-V power supply. Simulations show that the opamp in the SM-DAC achieves about a 60 phase margin, greater than 130-dB DC gain and more than 750-MHz gain bandwidth while maintaining a 2 Vp-p output signal swing, as illustrated in Fig. 6.

The opamp uses a switch circuit (SC) common-mode feedback circuit, as shown in Fig. 7, which is implemented with one set of output holding capacitors and two sets of resetting capacitors. These resetting capacitors operate on both non-overlap clock phases, enabling the opamp to maintain the output common-mode level during the whole clock cycle. In order to reduce the power dissipation of the opamps, the sampling capacitance and current of the opamps in the ADC are scaled

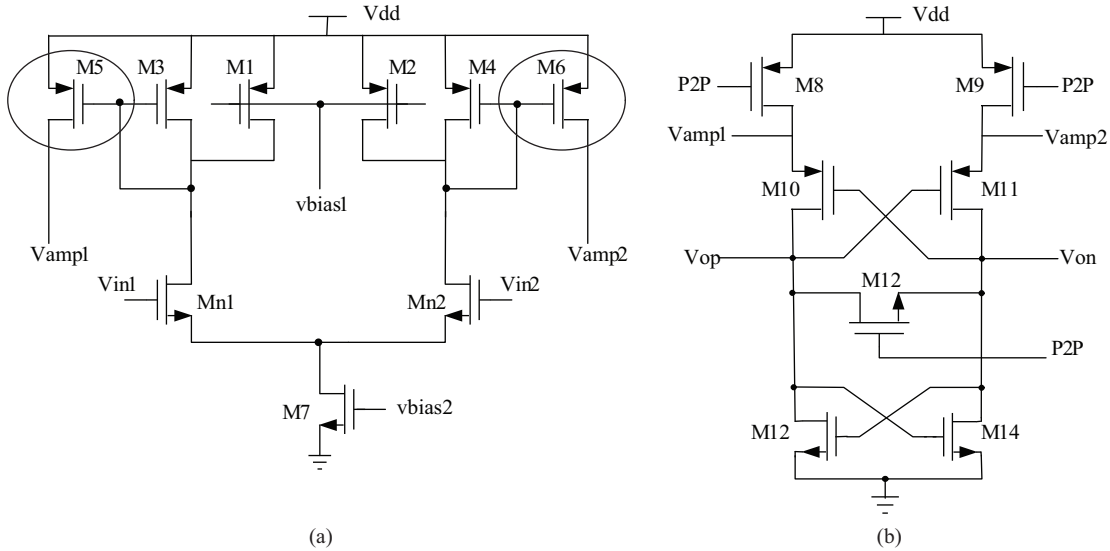

Fig. 9. Comparator. (a) Preamplifier. (b) Latch.

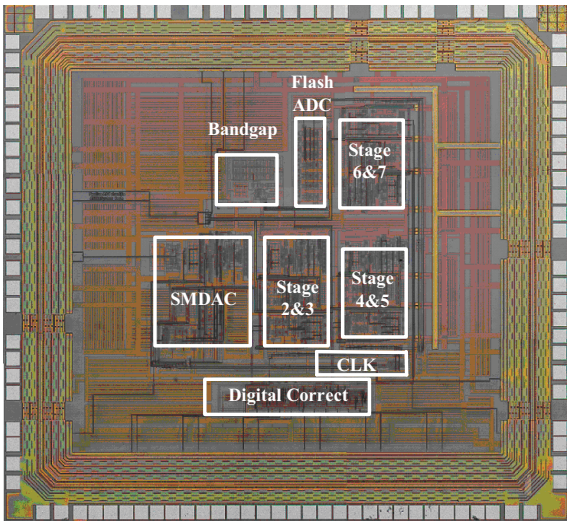

Fig. 10. Die micrograph.

down along the pipelined stages. Three different opamps are designed in this ADC. The SMDAC, stages 2 & 3 and stages 4 & 5 use different opamps (the opamp in stages 6 & 7 is same as that in stages 4 & 5).

4. Comparator

A total of 21 comparators are used in the sub-ADC of the stages and the 3-bit flash ADC. To reduce the effect of input referred offset and kick-back noise of the latch, a preamplifier is placed at the input of the latch[10], as shown in Fig. 8.

During the P1P clock phase, the preamplifier is in a unity-gain feedback loop around, and the sampling capacitor C_1 will be charged with the offset voltage V_{osp} of the preamplifier. During the P2 clock phase, the feedback loop opens and the input-referred offset of the preamplifier will be subtracted from the offset voltage that had been previously stored in the capacitors C_1. The offset voltage V_{OSL} of the latch is scaled to V_{OSL}/A when referred to the input of the preamplifier, A is the gain of

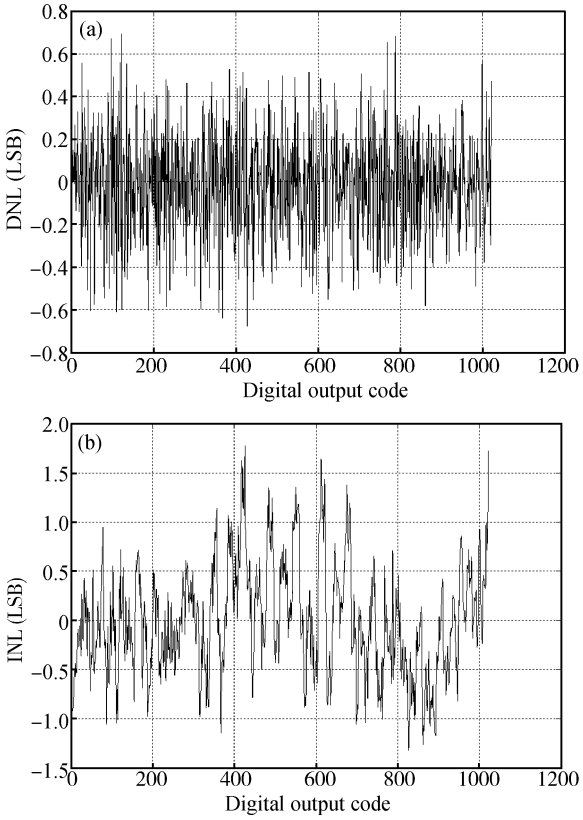

Fig. 11. Measured static performance. (a) DNL. (b) INL.

the preamplifier. A schematic of the preamplifier and latch are shown in Fig. 9. When P2P is low, the latch regenerates the difference voltages and the regeneration time is 0.4 μs.

5. Implementation and measured results

The prototype ADC is fabricated in a 0.35 μm 3.3 V CMOS process and occupies an active area of 1.81 mm^2 only. Figure 10 shows the die micrograph. A typical measured static performance is shown in Fig. 11. The measured differential nonlin-

Table 1. Performance summary.

Parameter	Value	Value
Resolution (bit)	10	10
Process	0.35 μm CMOS	0.35 μm CMOS
Power supply (V)	3.3	3.3
Active area (mm^2)	1.81	1.81
f_s (MHz)	20	50
SFDR (dB)	74.71 (f_{in} = 9.9 MHz), 73.95 (f_{in} = 22.1 MHz)	59.44 (f_{in} = 21.7 MHz), 56.85 (f_{in} = 49.7 MHz)
THD (dB)	72.70 (f_{in} = 9.9 MHz), 70.80 (f_{in} = 22.1 MHz)	56.82 (f_{in} = 21.7 MHz), 56.14 (f_{in} = 49.7 MHz)
SNR (dB)	59.71 (f_{in} = 9.9 MHz), 57.97 (f_{in} = 22.1 MHz)	54.67 (f_{in} = 21.7 MHz), 50.84 (f_{in} = 49.7 MHz)
SNDR (dB)	59.50 (f_{in} = 9.9 MHz), 57.75 (f_{in} = 22.1 MHz)	52.67 (f_{in} = 21.7 MHz), 49.72 (f_{in} = 49.7 MHz)
ERBW (MHz)	22.1	49.7
ENOB	9.6 (f_{in} = 9.9 MHz), 9.3 (f_{in} = 22.1 MHz)	8.5 (f_{in} = 21.7 MHz), 8.0 (f_{in} = 49.7 MHz)
DNL/INL (LSB)	0.22/0.43	0.7/1.75
Power (mW)	113	133

Table 2. Comparison of performance on several ADCs with similar resolution.

Parameter	Ref. [11]	ADS5102[12]	MAX1446[13]	This work	
Process (μm)	0.25	–	–	0.35	0.35
Power supply (V)	3.0	3.3	3.0	3.3	3.3
Active area (mm^2)	1.4	–	–	1.81	1.81
Resolution (bit)	10	10	10	10	10
f_s (MHz)	80	65	60	20	50
SFDR (dB)	72.2	71	73	74.71	59.44
SNDR (dB)	57.8	57	59	59.50	52.67
ENOB (bit)	9.3	9.0	9.51	9.6	8.5
DNL/INL (LSB)	0.21/0.56	0.5/1	0.4/0.6	0.22/0.43	0.7/1.75
Power (mW)	95	160	111	113	133

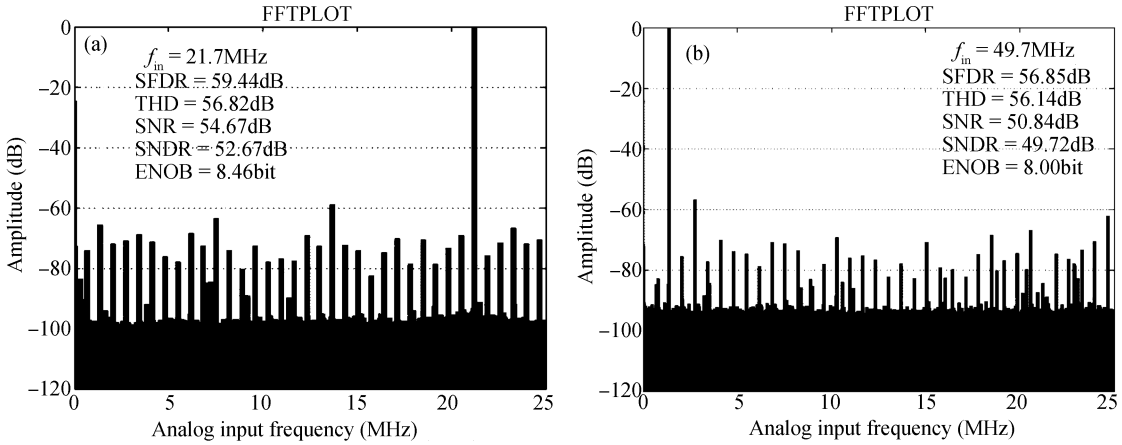

Fig. 12. Measured FFT plots @ f_s = 50 MS/s. (a) 21.7-MHz input. (b) 49.7-MHz input.

earity (DNL) and integral nonlinearity (INL) are less than 0.7 and 1.75 LSB, respectively.

The measured fast Fourier transform (FFT) spectra for input frequencies of 21.7 MHz and 49.7 MHz are plotted in Fig. 12. The ADC achieves more than 52.67-dB SNDR and above 59.44-dB SFDR performance with Nyquist input at full sampling rate. Figure 13 shows the measured dynamic performance versus the input frequency. This exhibits constant dynamic performance for input frequencies of up to twice the Nyquist rate (49.7 MHz) .The total power consumption of the ADC is approximately 133 mW at 50 MS/s with a 3.3-V supply. The performance of the ADC is summarized in Table 1. (The effective resolution bandwidth (ERBW) is the input frequency where the SNDR has dropped by 3 dB.) In Table 2, this work and some pipelined ADCs with similar resolutions are compared. This design shows the best dynamic and static performance at 20 MS/s and lesser area in this category. If power is pro proportional to V^2, this design dissipates 97 mW and 109 mW at 20 MS/s and 50 MS/s, respectively, when the power supply is 3 V. The tradeoff between SFDR, SNDR, power and area is well balanced in this work.

6. Conclusion

This paper describes a 3.3-V 10-bit 50-MS/s CMOS ADC, which occupies only a 1.81 mm^2 active area. The ADC achieves 52.67-dB SNDR and 59.44-dB SFDR performance with Nyquist input at a full sampling rate. The ADC exhibits

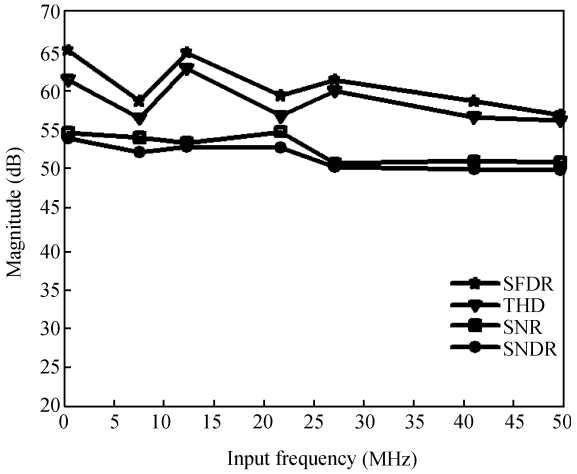

Fig. 13. Measured dynamic performance versus input frequency.

constant dynamic performance for input frequencies up to twice the Nyquist rate. The performance is obtained by employing the opamp-sharing architecture and by using SMDAC architecture, where the matching requirement along with the potential problems in the traditional SHA-less architecture are eliminated. The 10-bit pipelined ADC is completed by using just four opamps.

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