A continuous-time/discrete-time mixed audio-band sigma delta ADC

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Abstract: This paper introduces a mixed continuous-time/discrete-time, single-loop, fourth-order, 4-bit audio-band sigma delta ADC that combines the benefits of continuous-time and discrete-time circuits, while mitigating the challenges associated with continuous-time design. Measurement results show that the peak SNR of this ADC reaches 100 dB and the total power consumption is less than 30 mW.

Key words: continuous-time; discrete-time; sigma delta modulator; ADC

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1. Introduction

Although sigma delta ADC has largely been implemented as discrete-time (DT) circuits, continuous-time (CT) sigma delta ADC has received much attention in the last couple of years for high-speed and high-accuracy applications. A CT design allows for relaxed amplifier unity-gain bandwidth and power requirements. It also provides better noise immunity due to their inherent anti-aliasing properties[1].

Despite the advantages mentioned above for CT sigma delta ADC, audio-band sigma delta ADC implementations have remained in the DT domain, because they achieve relatively high linearity, and are very tolerant of clock jitter. Chopper stabilization can be readily employed in discrete time to remove the flicker noise, and the filter coefficients are very stable.

While all DT circuits need a driver in front of the integrator to load the sampling capacitors which perform the voltage-to-charge conversion, CT sigma delta ADC avoids having to buffer the input. The DT circuits require high-bandwidth amplifiers in order to transfer the charge from sampling to integrating capacitors at required settling accuracy during one clock cycle, and the CT circuits require less unity-gain bandwidth in the amplifiers for the same operating speed. On the sigma delta feedback side, the DT digital-to-analog (DACs) are also made of switched capacitors so the reference voltage has to be buffered to attain the required sampling speed, and the DACs for CT sigma delta ADC can be implemented with current sources which do not load the voltage reference[2].

This paper introduces a mixed CT/DT audio-band sigma delta ADC that combines the benefits of CT and DT circuits, while mitigating the challenges associated with CT design.

2. Mixed CT/DT audio-band sigma delta ADC

A sigma delta ADC requires a set of two transfer functions. In the audio-band low-pass ADCs, the two functions are a high-pass noise transfer function (NTF) and a low-pass signal transfer function (STF)[3]. The architecture of the mixed CT/DT, single-loop, fourth-order, 4-bit, audio-band sigma delta ADC is shown in Fig. 1.

This architecture allows for good control of the NTF as well as for a good control of STF by using both feedback coefficient c_1 and the feed-forward coefficients b_1, b_2, b_3, b_4. No feed-forward coefficient is connected at the input of the modulator, leaving only the first CT integrator to load the audio input. The integrator coefficients a_1, a_2, a_3, a_4 can be chosen as freedom degrees so the designer can control these integrator's outputs within 20% to 80% of the voltage between ground and the supply voltage when the ADC is not overloaded. This architecture has four feed-forward channels. When the input is larger than the overload level, the last integrators are into saturation, but the first integrator is still working normally. The fourth-order ADC becomes first-order ADC which is stable in any case. When the input comes back into the under-overload level, the first-order ADC is restored as fourth-order ADC automatically. Only one feedback path connected to CT integrator is used in this architecture. The feedback path for CT integrator can be implemented with current sources, which do not need reference voltages and voltage buffers.

The NTF is the filter defining the resolution and other properties of a sigma delta ADC; hence the design process always starts by defining this transfer function. Different filter families (Butterworth, ChebyshevI, ChebyshevII or elliptic) can be used. The delta–sigma toolbox[4] uses ChebyshevII high-pass filter for designing NTF. This paper calculates the ADC coefficients based on this toolbox. The input signal bandwidth is 20 kHz, and the over-sampling ratio (OSR) is 256. The design results are shown as

$$\mathrm{NTF}(z) = \frac{(z-1)^4}{(z^2-1.57z+0.622)\,(z^2-1.76z+0.802)}, \tag{1}$$

$$\mathrm{STF}(z) = \frac{0.66986\,(z-0.8518)\left(z^2-1.827z+0.8584\right)}{(z^2-1.57z+0.622)\,(z^2-1.76z+0.8202)}. \tag{2}$$

Normalized magnitude characteristic of NTF is shown in Fig. 2. The quantization noise can be transferred to high-frequency by NTF. The peak signal-noise-ratio (SNR) of this ADC can reach 117 dB.

The coefficients of sigma delta modulator are summarized in Table 1.

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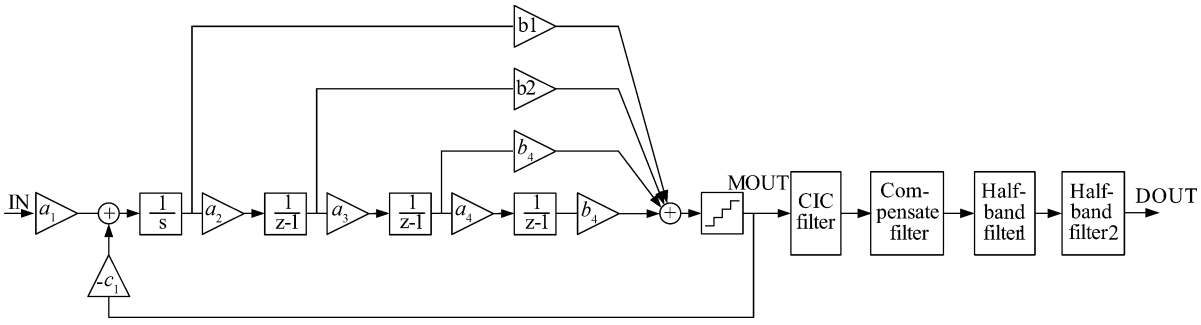

Fig. 1. Mixed CT/DT audio-band sigma delta ADC architecture.

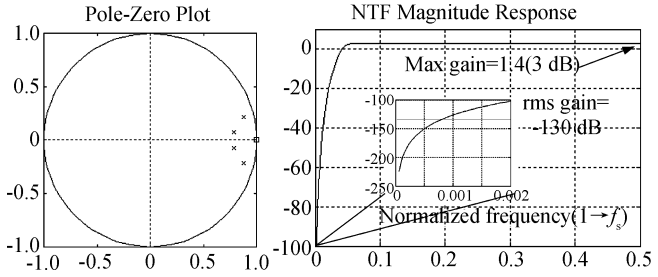

Fig. 2. NTF magnitude characteristic.

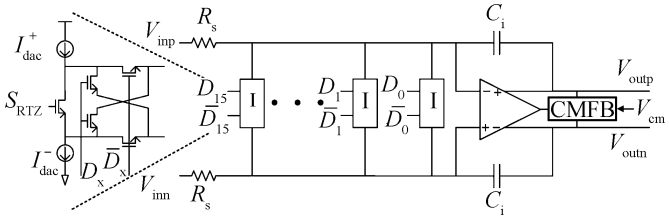

Fig. 3. First order CT integrator.

Table 1. Modulator coefficients.

Parameter	Value	Parameter	Value
a_1	0.2	b_1	1.4
a_2	0.3	b_2	2
a_3	0.2	b_3	1.6
a_4	0.1	b_4	1.2
c_1	0.2		

Digital decimation filter decimates and filters the high-speed data stream of the modulator's output, attenuates the noise outside of the input signal bandwidth, such as quantization noise, the noise generated by the modulator and pre-filter, and changes the modulator output sampling frequency down to the signal Nyquist frequency. The circuit complexity of the digital decimation filter is decided by its pass-band ripple coefficients, stop-band attenuation coefficients and transition zone width. Digital decimation filter can be achieved by single-stage or multi-stage. In a single-stage implementation, we have to use high-order filter, in order to save hardware, digital decimation filter usually is achieved by multi-stage. In this paper, we design digital decimation filter using cascaded integrator comb (CIC) filter, compensation filter and two half-band filters which are cascaded together[5].

3. Circuit design

3.1. CT integrator

An active-RC circuit is used for the first CT integrator, which is shown in Fig. 3. This should be preferred for high-linearity applications since the operational amplifier holds the voltage between its inputs ideally equal, turning the Rs resistors into linear voltage-to-current converters. The DAC of this CT integrator is implemented as a set of 16 current sources controlled by a thermometer-coded, 16-bit word supplied by the quantizer[6].

A differential current source consists of two current sources, I_{dac+} and I_{dac-}, which are connected to one or the other of the operational amplifier inputs, according to the quantizer decision Dx. On Dx logic-high, I_{dac+} is sourced into the non-inverting operational amplifier input node and I_{dac-} is sunk from the inverting input node. On Dx logic-low, the connections are reversed, therefore the common-mode feedback current is ideally zero. The feedback current is integrated by the operational amplifier on the two capacitors C_i in the same manner as the signal current. The return-to-zero clock S_{RTZ} is used to reduce in-band quantization noise due to inter-symbol modulation.

The R_s, C_i, and I_{dac+} of the first CT integrator can be calculated according to the integrator coefficients a_1, c_1 and the conversion from DT to CT. The conversion formula from DT to CT is shown as[7]

$$H(z) = \frac{1}{z-1} \Rightarrow H(s) = \frac{f_{clk}}{s}, \tag{3}$$

where f_{clk} denotes the DT integrator sampling frequency. The transfer function of the DT integrator and the conversion from DT integrator to CT integrator is calculated as

$$\begin{aligned} Y(z) &= \frac{a_1}{z-1}X(z) \pm \frac{c_1}{z-1}E(z) \\ &\Rightarrow \begin{cases} H_X(z) = \dfrac{a_1}{z-1} \Rightarrow H_X(s) = \dfrac{a_1 f_{clk}}{s}, \\ H_E(z) = \dfrac{c_1}{z-1} \Rightarrow H_E(s) = \dfrac{c_1 f_{clk}}{s}. \end{cases} \end{aligned} \tag{4}$$

With an ideal operational amplifier, the transfer function

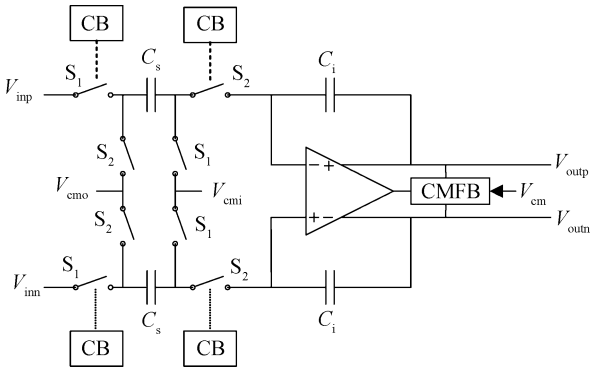

Fig. 4. Higher order SC integrators.

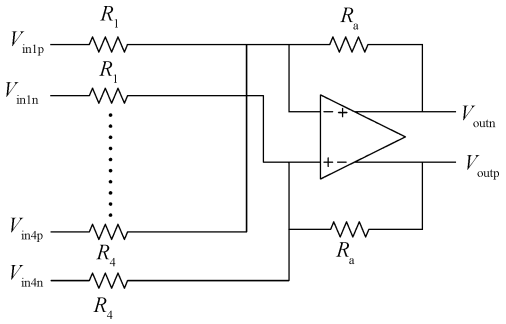

Fig. 5. Feed-forward adder.

of the first CT integrator is

$$\frac{V_{\text{in}}}{R_{\text{s}}} \pm 16I_{\text{dac}} = C_{\text{i}}\frac{\text{d}V_{\text{out}}}{\text{d}t} \Rightarrow \begin{cases} H_{\text{X}}(s) = \dfrac{1}{sR_{\text{s}}C_{\text{i}}}, \\ H_{\text{E}}(s) = \dfrac{16I_{\text{dac}}}{sC_{\text{i}}}. \end{cases} \tag{5}$$

According to Eqs. (4) and (5), the R_{s}, C_{i}, and I_{dac} can be calculated as

$$R_{\text{s}}C_{\text{i}} = \frac{1}{a_1 f_{\text{clk}}}, \tag{6}$$

$$I_{\text{dac}} = \frac{c_1}{16}C_{\text{i}}f_{\text{clk}}. \tag{7}$$

3.2. SC integrator

The higher-order integrators are fully differential switched-capacitor (SC) circuits, which are shown in Fig. 4. They consist of sampling capacitors C_{s}, integrating capacitors C_{i} and operational amplifier[8].

One advantage of SC integrator is the decoupling of the input signal common-mode V_{cmi} and the operational amplifier common-mode input V_{cmo}. The two values, V_{cmi} and V_{cmo}, are independently set with V_{cmi} tied to the middle of the supply voltage to take advantage of the rail-to-rail output capability of the previous integrator while V_{cmo} has a low value falling inside the common-mode input range of the PMOS-input amplifier. Another advantage of SC integrator is the good control of capacitor ratios. In a sigma delta modulator, the better control of each path gain means that the decrease of the modulator performance can be minimized due to the impact of coefficient deviation.

The sampling switches have to offer a low on-resistance during the sampling phase. In order to guarantee an adequately low resistance, the clock voltage used to drive sampling switches can be bootstrapped beyond the supply voltage range.

Because the modulator has only one feedback path connected to CT integrator, the higher-order SC integrators are designed simply, which do not need feedback sampling capacitors or reference voltage.

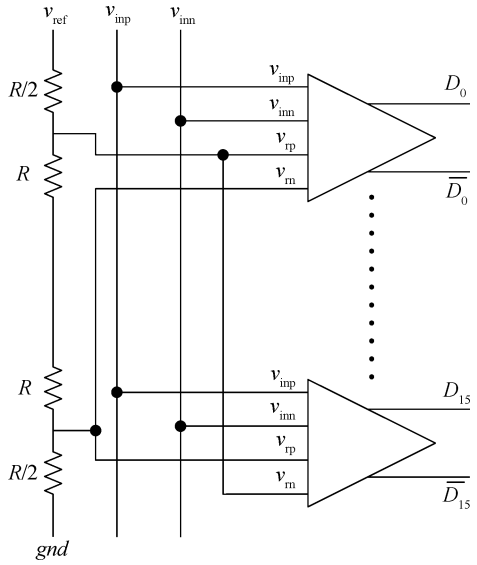

Fig. 6. A 4-bit quantizer.

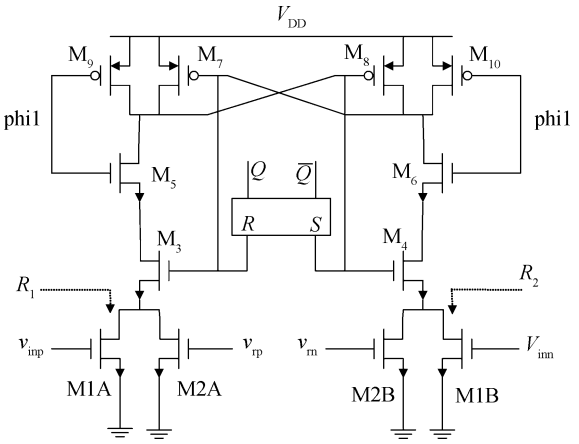

Fig. 7. Latch comparator.

3.3. Feed-forward adder

An adder, as shown in Fig. 5, is used in front of the quantizer to sum the feed-forward coefficients.

The resistors are noise-limited, yet have values large enough so they do not load the integrators significantly. The voltage-to-current converters R_1 to R_4 are scaled according to the feed-forward coefficients b_1, b_2, b_3, b_4. The summation resistor R_{a} is further scaled to bring the output signal of the adder in the input range of the quantizer.

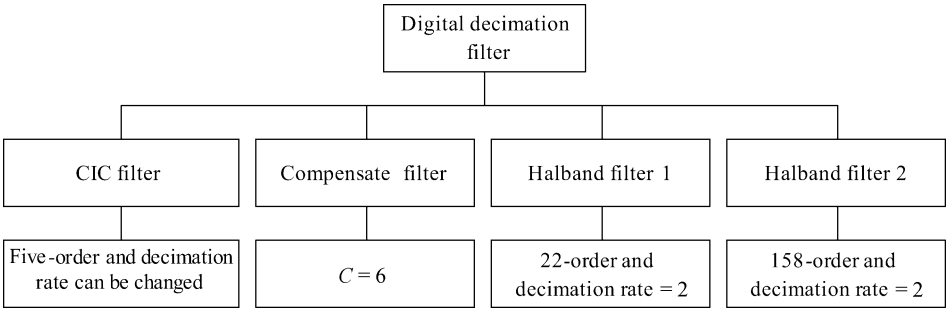

Fig. 8. Digital decimation filter.

3.4. Quantizer

Sixteen comparators connected to a resistive ladder are used to build the 4-bit quantizer, as shown in Fig. 6.

The resistive ladder supplies the reference levels by dividing the reference supply vref into 16 steps. The differential input voltage vinp and vinn is supplied to all comparators. A practical latch comparator is shown in Fig. 7.

The values of the inputs will cause the resistances R_1, R_2 to vary. When the latch is enabled, the drains of M3 and M4 are connected to the comparator output. M3 and M4 form a parallel positive-feedback path and the gain of the feedback path depends on the value of the resistors $R_1$and R_2. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the R_1 and R_2 resistances.

3.5. Digital decimation filter

Digital decimation filter uses cascade structure including CIC filter, compensation filter and two half-band filters. Single-stage integrator comb filter's side lobe level is only lower than the main lobe of 13.46 dB, which means that stop-band attenuation is poor, generally very difficult to directly meet the practical requirement. In order to reduce the side lobe level, we use multi-stage cascaded integrator comb filter, namely, CIC filter. The CIC filter's form is determined by the filter's decimation rate and filter's order. In this paper, the OSR of the sigma delta ADC is 256, so the CIC filter's decimation rate is 64. Choose the order of the CIC filter higher one order than the modulator' order to ensure that through the CIC filter the noise spectrum's shape does not change, so that the last filters extraction to get the most resolution. The transfer function of compensation filter is shown as

$$H(z) = \frac{1}{|C+2|}(1 + Cz^{-I} + z^{-2I}). \tag{8}$$

Take different C value, compensation filter gets different compensation results. Through the analysis of the filter's pass-band ripple and stop-band attenuation by MATLAB FVTool, when taking $C = 6$, the cascade filter's pass-band ripple is 0.08 dB, which meets the design requirements.

In order to guarantee that decimation filter with a decimation rate of 2 does not produce aliasing distortion, the filter must filter the quarter of Nyquist frequency (F_s) or more frequency components out before decimating. Half-band filter can achieve this function. Its pass-band ripple and stop-band attenuation are the same, and its pass-band edge frequency and stop-band edge frequency are relative to the F_s/4 symmetry.

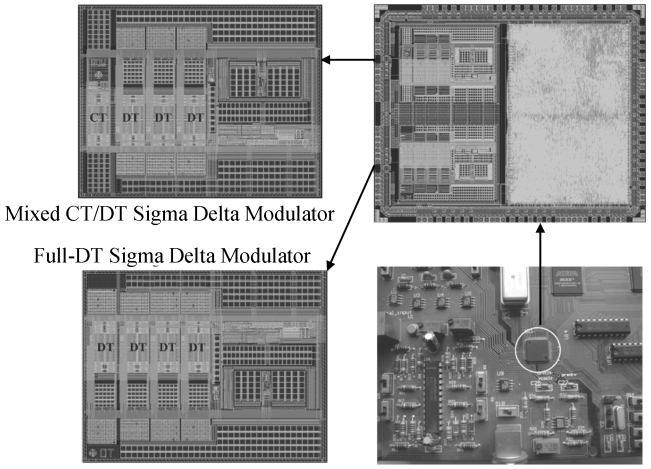

Fig. 9. Micrograph of the test chip.

The whole structure of digital decimation filter is shown in Fig. 8.

4. Layout and results

An audio-band sigma delta ADC test chip is designed and fabricated in SMIC 0.18 μm one-poly four-metal CMOS process. The tapeouted chip can easily be configured as either the mixed CT/DT ADC or the full-DT ADC, which includes a mixed CT/DT modulator, a full-DT modulator and a shared digital decimation filter. Modulator choice signal can control the mixed CT/DT modulator working on with the full-DT modulator shutdowning to configure as the mixed CT/DT ADC and vice versa. The only difference between full-DT sigma delta modulator and mixed CT/DT sigma delta modulator is that the first integrator of full-DT sigma delta modulator is fully differential switched capacitor circuit. The whole chip area including I/O pads is approximately 2×1.5 mm^2 and the area of both modulators is 0.8×0.6 mm^2. The test chip is shown in Fig. 9, which can be configured as either the mixed CT/DT or the full-DT audio-band sigma delta ADC.

Measurement results of the mixed CT/DT sigma delta ADC are illustrated as follows. Figure 10(a) shows a fast Fourier transform (FFT) plot with a –3 dBFS 3.35 kHz input. SNR is measured to be around 98 dB. Figure 10(b) shows the FFT plot with noise. Figure 11 shows the measured SNR and signal noise distortion ratio (SNDR) for a 3.35 kHz input signal. The peak SNR of 100 dB is achieved in a 20 kHz signal bandwidth.

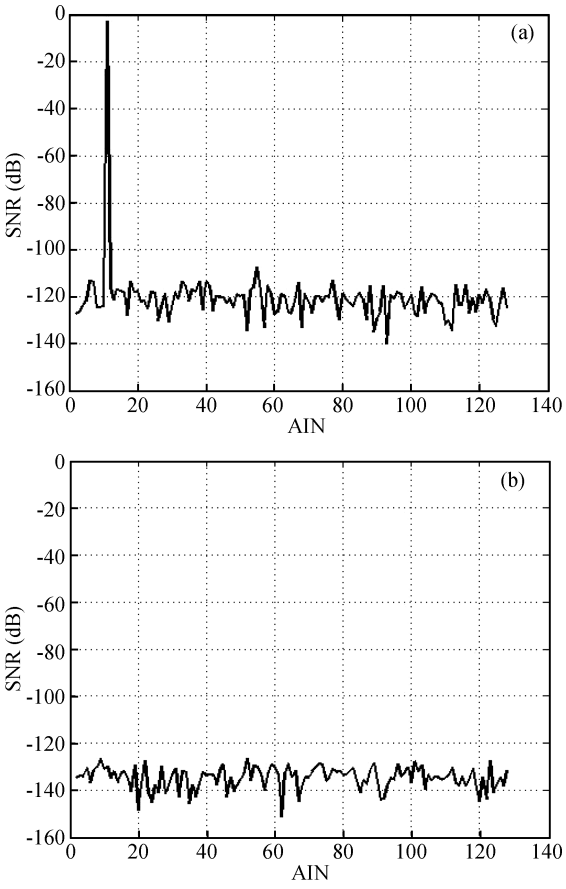

Fig. 10. (a) FFT spectrum with –3 dBFS 3.35 kHz input. (b) FFT spectrum with noise.

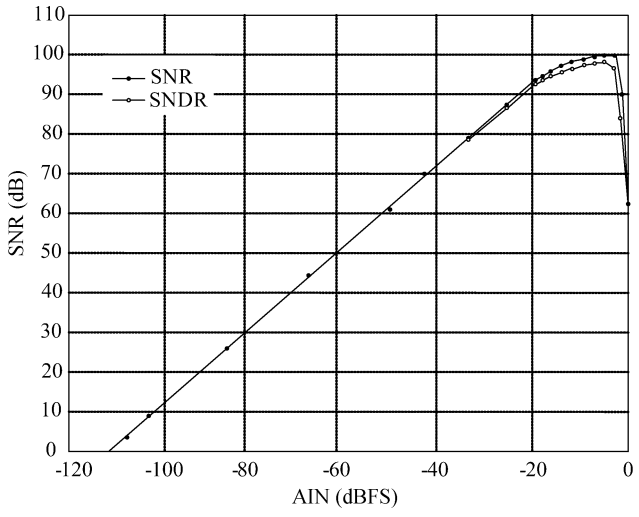

Fig. 11. Measured SNR and SNDR.

Figure 12 shows the performance comparison between mixed CT/DT sigma delta ADC and full-DT sigma delta ADC. The tapeout chip includes the two structure ADCs. Modulator choice signal can control which ADC is working on and shutdown another ADC. Test the two structure ADCs in turn, we can see when the input signal of mixed CT/DT sigma delta ADC reaches –3 dBFS, the peak SNR is 100 dB and the DR is 110 dB. When the input signal of full-DT sigma delta ADC

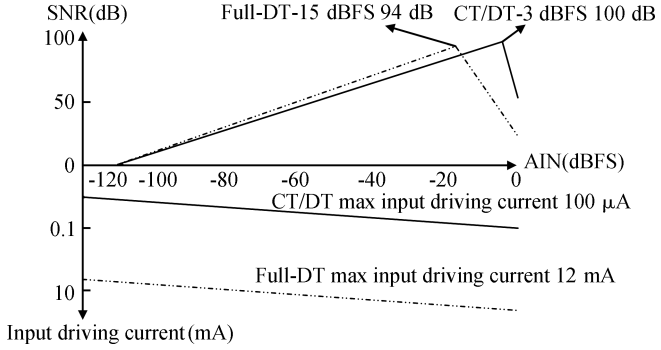

Fig. 12. compare between mixed CT/DT sigma delta ADC and full -DT sigma delta ADC.

Table 2. Performance summary.

Parameter	Value
Resolution	24 bit
OSR	256
DR	110 dB
Peak SNR	100 dB
SNDR	98 dB
PSRR	–92 dB
Input signal bandwidth	20 kHz
Supply voltage	1.8 V/3.3 V
Sigma Delta modulator supply current	10 mA
Digital decimation filter supply current	3 mA
IO pad supply current	2 mA
Total power consumption	30 mW
Technology	SMIC 0.18 μm CMOS 1P4M
Chip area	2×1.5 mm^2

reaches –15 dBFS, the peak SNR is only 94 dB and the DR is 98 dB. So mixed CT/DT sigma delta ADC has better SNR, higher dynamic range which means ADC can offer high resolution and wide input range. The max input driving current of mixed CT/DT sigma delta ADC is 100 μA and the max input driving current of full-DT sigma delta ADC is 12 mA, the lower input driving current of mixed CT/DT sigma delta ADC means that the complex driving circuits is not needed.

The most important specifications are summarized in Table 2. The figure of merit (FOM) of the converter is determined as

$$\mathrm{FOM_{SNR}} = \frac{P}{2 \times f_{\mathrm{B}} \times 2^{(\mathrm{peakSNR}-1.76)/6.02}}, \tag{9}$$

$$\mathrm{FOM_{DR}} = \frac{P}{2 \times f_{\mathrm{B}} \times 2^{(\mathrm{DR}-1.76)/6.02}}, \tag{10}$$

where P, f_{B}, DR, and peakSNR, denote the power consumption, signal bandwidth, dynamic range (DR) and peak SNR.

Table 3 shows a performance comparison between different designs and this work. The mixed CT/DT audio-band sigma delta ADC of this work operates at 20 kHz signal bandwidth with 30 mW power dissipation, and achieves $\mathrm{FOM_{SNR}}$ = 9.18 pJ and $\mathrm{FOM_{DR}}$ = 2.9 pJ, which are smallest compared with other designs in Table 3.

Table 3. Performance comparison.

Parameter	Ref. [9]	Ref. [10]	Ref. [11]	This work	
Structure	Full-DT	Full-DT	Full-DT	Full-DT	Mixed CT/DT
Tech. (μm)	0.35	0.35	0.65	0.18	0.18
Resolution (bit)	24	24	24	24	24
V_{DD} (V)	5	3.3/5	5	1.8/3.3	1.8/3.3
f_B (kHz)	20	20	100	20	20
Power (mW)	300	68	295	33	30
Peak SNR (dB)	110	105	95	94	100
DR (dB)	120	114	97	98	110
FOM_{SNR} (pJ)	29	11.69	32	20.13	9.18
FOM_{DR} (pJ)	9.17	4.15	25	12.7	2.9

5. Conclusion

Measurement results show the mixed CT/DT audio-band sigma delta ADC offers better SNR, lower power consumption and the FOM is very small than full-DT sigma delta ADC. With such competitive advantages, mixed CT/DT audio-band sigma delta ADC will become a preference in the new audio-band ADC implementations.

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