A novel complementary N^+-charge island SOI high voltage device*

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Abstract: A new complementary interface charge island structure of SOI high voltage device (CNI SOI) and its model are presented. CNI SOI is characterized by equidistant high concentration n^+-regions on the top and bottom interfaces of dielectric buried layers. When a high voltage is applied to the device, complementary hole and electron islands are formed on the two n^+-regions on the top and bottom interfaces. The introduced interface charges effectively increase the electric field of the dielectric buried layer (E_I) and reduce the electric field of the silicon layer (E_S), which result in a high breakdown voltage (BV). The influence of structure parameters and its physical mechanism on breakdown voltage are investigated for CNI SOI. E_I = 731 V/μm and BV = 750 V are obtained by 2D simulation on a 1-μm-thick dielectric layer and 5-μm-thick top silicon layer. Moreover, enhanced field E_I and reduced field E_S by the accumulated interface charges reach 641.3 V/μm and 23.73 V/μm, respectively.

Key words: complement; charge islands; interface charges; dielectric buried layer; breakdown voltage
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1. Introduction

The breakdown voltage (BV) of a SOI (silicon on insulator) high voltage device is limited by the low vertical breakdown voltage ($V_{B,V}$), and some work has been carried out[1−8]. Enhancing the electric field of the buried dielectric is a feasible way to increase the $V_{B,V}$, so BV by ENDIF (enhanced dielectric layer field) and several new structures have been proposed[9−14], in which introducing interface charges is effective and attractive.

Based on the theoretical investigation of complementary interface charge islands (CNI SOI) with a buried oxide layer, further research on SOI with complementary interface charge islands (CNI SOI) is proposed in this paper, which provides a higher BV than conventional SOI. The influences of structure parameters on the BV are analyzed and compared with conventional SOI.

2. Structure and mechanism

CNI SOI LDMOS and its mechanism are shown in Figs. 1(a) and 1(b). Equidistant high concentration n^+-regions are implanted on the top and bottom interfaces of a dielectric buried layer. When a high voltage is applied to the device, complementary holes and electron islands are formed on the two n^+-regions on the top and bottom interfaces. t_s, t_I, t_{sub} and H represent the thickness of the top Si layer, buried layer, substrate and CNI layer, respectively. L_d, D and W are the lengths of the drift region, n^+-regions and spacing of two neighboring n^+-regions, respectively.

For an optimized device in the lateral direction, BV lies on the vertical BV ($V_{B,V}$), and then, BV is nearly interrelated with the electric field distribution under the drain (along MN in Fig. 1(a)), especially the electric fields E_S and E_I on the interface, where E_S and E_I are the electric fields in the silicon and dielectric buried layer at A point under the drain, respectively. To clarify, suppose that the charge density $\sigma = \sigma_t + \sigma_b$ (σ_t: charge density of inversion hole on the top interface, σ_b: charge density of inductive electrons on the bottom interface) in each CNI cell is equal, which divides the device into n regions, as shown in Fig. 1(a): the first CNI cell with interface charge density σ_1 ($\sigma_1 = \sigma_{1,t} + \sigma_{1,b}$) is region 1, while the last CNI cell (under the drain) with interface charge density $\sigma_n = \sigma_{Ld+LS}$ is region n. When a high positive voltage V_d is applied to the drain while the source, gate and substrate are grounded, the 2-D potential $\phi(x, y)$ in the drift region can be written as $\phi(x, y) = \omega(x, y) + \varphi(x, y)$, where $\omega(x, y)$ and $\varphi(x, y)$ are the contributions of V_d and depleted impurities in the drift region, respectively, in which, $\varphi(x, y)$satisfies the 2-D Poisson equation:

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_S}, \quad 0 \leqslant x \leqslant L_d + L_s, \quad 0 \leqslant y \leqslant t_S, \quad (1)$$

where ε_S is the permittivity of silicon and q is the electron charge. For a fully-depleted drift region, the vertical electric field in the top silicon layer satisfies

$$E_y(x,y) = -\frac{\partial\varphi(x,y)}{\partial y} = \psi_1(x) + \psi_2(x)y, \quad 0 \leqslant x \leqslant L_d + L_s, \quad 0 \leqslant y \leqslant t_S. \quad (2)$$

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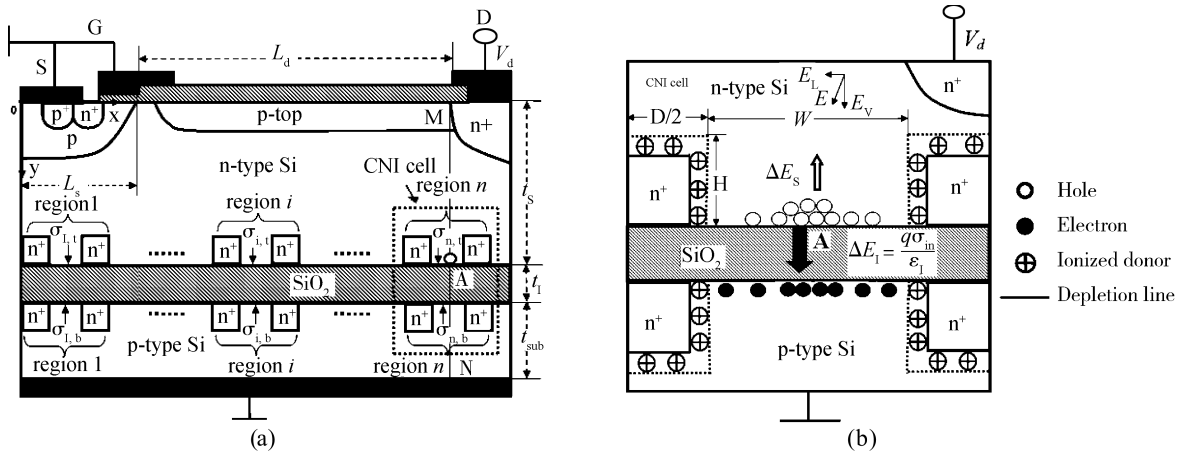

Fig. 1. (a) Device structure and (b) a CNI cell of CNI SOI LDMOS.

The boundary conditions for Eq. (2) are given by

$$\left.\frac{\partial\varphi(x,y)}{\partial y}\right|_{y=0}=0, \tag{3}$$

$$\varphi(0,0)=0,\quad \varphi(L_{\rm d}+L_{\rm s},0)=V_{\rm d}, \tag{4}$$

$$\frac{\varepsilon_{\rm I}[\varphi(x,t_{\rm S})-\varphi(x,t_{\rm S}+t_{\rm I})]}{t_{\rm I}}=-\left.\frac{\partial\varphi(x,y)}{\partial y}\varepsilon_{\rm S}\right|_{y=t_{\rm S}}+q\sigma_{\rm i}(x), \tag{5}$$

where $\varepsilon_{\rm I}$ is the permittivity of the dielectric buried layer (SiO_2), and Equation (5) is based on the continuity of electric displacement on the interface ($y=t_{\rm S}$). Solving Eq. (2) with the boundary conditions yields

$$\varphi(x,y)=-\frac{1}{2}\psi_2(x)y^2+\psi_2(x)t^2+\frac{q\sigma_{\rm i}(x)t_{\rm I}}{\varepsilon_{\rm I}}+\varphi(x,t_{\rm S}+t_{\rm I}), \tag{6}$$

where $t=t_{\rm s}\sqrt{0.5+t_{\rm I}\varepsilon_{\rm S}/t_{\rm s}\varepsilon_{\rm I}}$ is the characteristic thickness of SOI/PSOI devices. From Eq. (6), the surface potential distribution ($y=0$) is obtained as

$$\varphi(x,0)=-\psi_2(x)t^2+\frac{q\sigma_{\rm i}(x)t_{\rm I}}{\varepsilon_{\rm I}}+\varphi(x,t_{\rm S}+t_{\rm I}). \tag{7}$$

With Eq. (6), Equation (7) yields

$$\varphi(x,y)=\frac{q\sigma_{\rm i}(x)t_{\rm I}+\varepsilon_{\rm I}\varphi(x,t_{\rm S}+t_{\rm I})-\varepsilon_{\rm I}\varphi(x,0)}{2\varepsilon_{\rm I}t^2}y^2+\varphi(x,0). \tag{8}$$

From Eq. (9), the electric potential distribution under the drain (along MN) can be obtained as

$$\varphi(L_{\rm d}+L_{\rm s},y)=\frac{q\sigma_{\rm i}(L_{\rm d}+L_{\rm s})t_{\rm I}+\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},t_{\rm S}+t_{\rm I})-\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},0)}{2\varepsilon_{\rm I}t^2}y^2+\varphi(L_{\rm d}+L_{\rm s},0). \tag{9}$$

From Eq. (9), the vertical electric field under the drain (along MN) is derived as

$$E_y(L_{\rm d}+L_{\rm s},y)=\frac{\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},0)-q\sigma_{\rm i}(L_{\rm d}+L_{\rm s})t_{\rm I}-\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},t_{\rm S}+t_{\rm I})}{\varepsilon_{\rm I}t^2}y. \tag{10}$$

With Eq. (10) and Gauss-theory on the interface, the electric fields in the silicon and dielectric buried layers $E_{\rm S}$ and $E_{\rm I}$ of A point are obtained as

$$E_{\rm S}=\frac{V_{\rm d}-\varphi(L_{\rm d}+L_{\rm s},t_{\rm S}+t_{\rm I})}{t^2}t_{\rm S}-\frac{t_{\rm I}t_{\rm S}q\sigma_{L_{\rm d}+L_{\rm s}}}{\varepsilon_{\rm I}t^2}, \tag{11}$$

$$E_{\rm I}=\frac{\varepsilon_{\rm S}t_{\rm S}}{\varepsilon_{\rm I}t^2}[V_{\rm d}-\varphi(L_{\rm d}+L_{\rm s},t_{\rm S}+t_{\rm I})]+\frac{t_{\rm S}^2q\sigma_{L_{\rm d}+L_{\rm s}}}{2\varepsilon_{\rm I}t^2}. \tag{12}$$

From Eqs. (11) and (12), the interface charge $\sigma_{L_{\rm d}+L_{\rm S}}$ in the proposed CNI SOI can enhance $E_{\rm I}$ in comparison with the conventional SOI ($\sigma_{L_{\rm d}+L_{\rm S}}=0$), while shielding the silicon layer electric field $E_{\rm S}$ avoiding silicon layer premature breakdown (shown as $\Delta E_{\rm I}$ and $\Delta E_{\rm S}$ in Fig. 1(b), respectively). These all contribute to a high BV. Moreover, with $\sigma_{L_{\rm d}+L_{\rm S}}=0$, Equations (11) and (12) can be used for the conventional SOI.

3. Results and discussion

Two-dimensional device simulations[15] for the proposed CNI SOI LDMOS specified in Table 1 were performed to verify the device operation.

Figure 2 is the hole and electron concentrations on both the top ($y=4.999$ μm) and bottom ($y=6.001$ μm) interfaces of the buried dielectric layer for the CNI SOI LDMOS at breakdown. Plentiful holes are located on the top interface whose concentration increases from the source to the drain with potential 3.32×10^{18} cm^{-3} of hole concentration under the drain. Moreover, there are 10^{17} cm^{-3}-class electrons existing on the bottom interface.

From Fig. 3(a), the inversion layer is about 90 nm. Based on Eqs. (11) and (12), the interface inversion holes should effectively enhance $E_{\rm I}$ and improve BV. Figure 3(b) gives the

Table 1. Device parameters used in the simulation.

Device parameter	Value	Unit
Drift length, L_d	30–90	μm
Thickness of SOI layer, t_S	5	μm
Thickness of Buied layer, t_I	1	μm
Thickness of p-top layer, t_p	0.5, 0.8,1	μm
Thickness of p-substrate layer	2	μm
p-substrate concentration	3×10^{14}	cm^{-3}
Thickness of CNI layer, H	0–1.2	μm
n^+-region length in CNI layer, D	0–2	μm
n^+-region concentration in CNI layer	1×10^{19}	cm^{-3}
Spacing of two neighboring n^+-region in CNI layer, W	1–3.5	μm

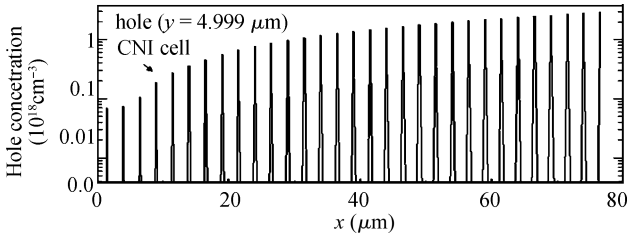

Fig. 2. Hole concentrations on both the top ($y = 4.999\ \mu$m) interfaces of the buried dielectric layer for CNI SOI at breakdown ($D = H = 0.5\ \mu$m, $W = 2\ \mu$m, $L_d = 70\ \mu$m).

three-dimensional hole distribution in the last CNI cell under the drain, in which, the highest hole concentration is at the Cell A point because of the maximal Coulomb force at this point.

Figure 4 is the vertical electric field and potential distribution at breakdown under the drain. E_I increases from 89.7 V/μm of the conventional SOI to 731 V/μm of CNI SOI, which results in a BV of 750 V for CNI SOI compared with 204 V for the conventional SOI. The voltage shared by the buried dielectric layer ($V_I = t_I E_I$ = 731 V) is above 90% of the BV. Inversion charges reduce the Si layer electric field E_S to 5.87 V/μm and avoid Si layer premature breakdown.

Figure 5 gives a comparison of surface electric field and the equipotential contour distribution at breakdown for the proposed CNI SOI and conventional SOI LDMOS. It is clear that the equipotential contour distribution of CNI SOI is more uniform than that of conventional SOI. Moreover, interface holes of CNI SOI effectively modulate the surface electric field, which means that a more uniform surface electric field is achieved for the proposed CNI SOI than that of conventional SOI, as shown in Fig. 5.

Figure 6 gives the dependences of hole concentrations at middle points of n^+-regions on applied voltages. With adding V_d from 100 V to BV (750 V), the hole concentrations at each middle point of the n^+-regions increase, and for each V_d, the hole concentration is enhanced from source to drain with potential. This shows that interface holes have the self-adaptive characteristic and ability, which automatically varied with the applied voltage and effective enhancement on E_I to make the device endure the applied voltages.

Figures 7(a), 7(b) and 7(c) give the influences of D, H, W and L_d on BV. It can be seen that BV is improved with increasing L_d which breaks through the BV limitation of conventional

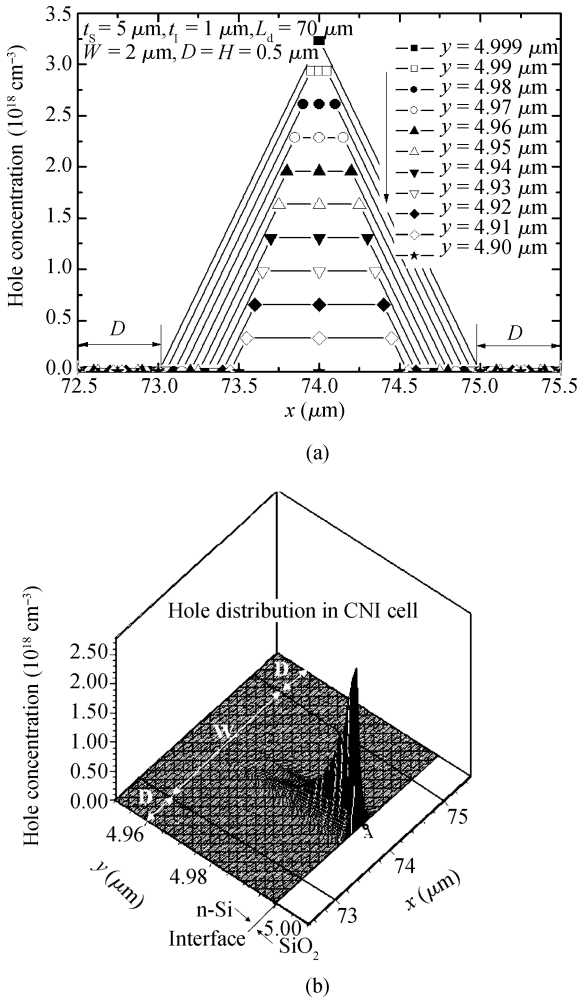

Fig. 3. Charge distribution for the CNI SOI LDMOS at breakdown. (a) Hole distribution in a CNI cell with different vertical distances. (b) Three-dimensional hole distribution in a CNI cell.

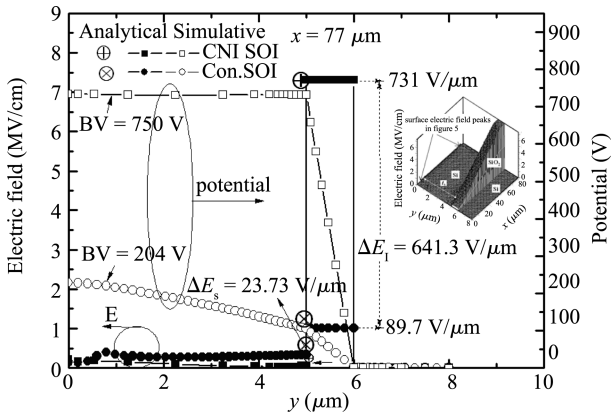

Fig. 4. Vertical electric fields and potential distribution under the drain ($x = 77\ \mu$m) for the CNI SOI ($N_d = 1.2\times10^{15}$cm^{-3}) and the conventional SOI ($N_d = 2.4\times10^{15}$cm^{-3}).

SOI. BV > 450 V can be obtained with W from 1.5–2.5 μm. H and W obviously affect BV and there is a maximum BV of 750 V when $W = 2\ \mu$m and $D = H = 0.5\ \mu$m with L_d = 70 μm.

Figure 8 shows the influences of N_{n+} on BV, E_I and the

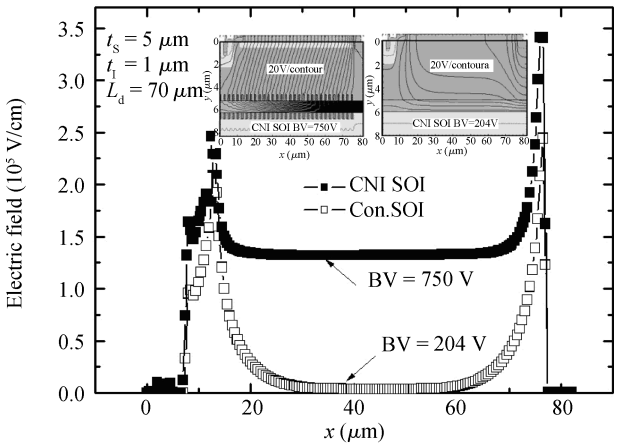

Fig. 5. Surface electric field (y = 0.001 μm) distributions for CNI SOI and conventional SOI. The inset is the equipotential contour distribution for the two devices.

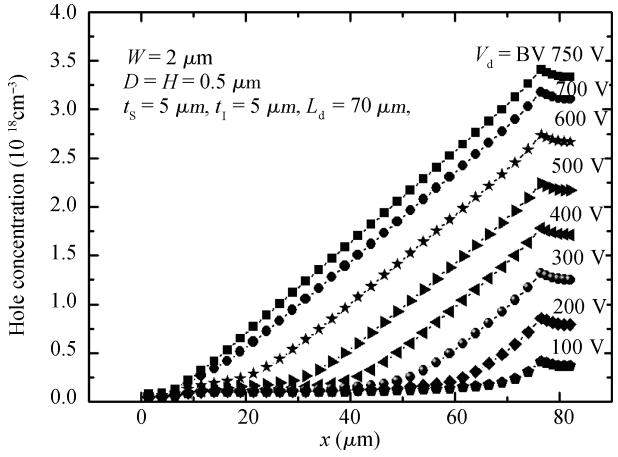

Fig. 6. Hole concentrations at every cell middle point with different applied voltages.

maximal hole concentration $N_{h,m}$. It can be seen that when N_{n+} is larger than 1.7×10^{18} cm^{-3}, BV is invariable as well as E_I and $N_{h,m}$. When N_{n+} is less than 1.7×10^{18} cm^{-3}, BV decreases with the decreasing N_{n+}, the reason for which can be explained as follows. When N_{n+} is larger than 1.7×10^{18} cm^{-3}, the n$^+$-regions under the drain are undepleted and the ionized donors are invariable, which is independent of N_{n+}, and therefore, inversion holes are fixed by the force from the ionized donors.

Figure 9 shows the dependence of thickness t_p and concentration N_p of the p-top layer on BV. BV is almost invariable with t_p from 0.5, 0.8 to 1 μm, and for each t_p, The maximal BV appears when t_pN_p is about 1.5×10^{12} cm^{-2}, which satisfies the RESURF (reduced surface field) condition and, after that, BV sharply decreases because of premature breakdown at the n$^+$–p junction of the drain side.

4. Conclusion

A new high-voltage device structure of the CNI SOI LDMOS is proposed. CNI SOI effectively utilizes the enhancement effect of the interface charges on the electric field of the dielectric buried layer to increase the breakdown voltage. BV increases by 267.6% in comparison with the conventional SOI with the same t_S, t_I and L_d. The fabrication processes of CNI SOI are fully compatible with conventional CMOS/SOI technology. This offers potential for applications in high voltage and power integrated circuits.

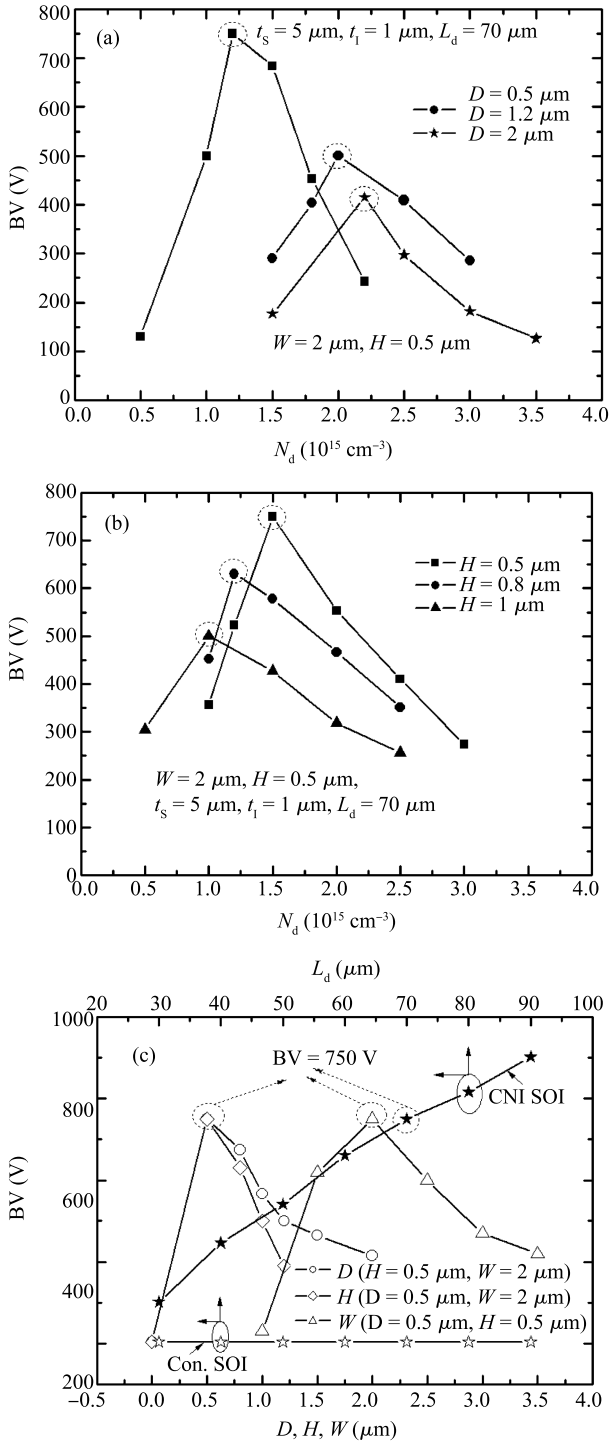

Fig. 7. (a), (b) Influences of D and H on breakdown voltage. (c) Influences of structure parameters D, H, W and L_d on breakdown voltage.

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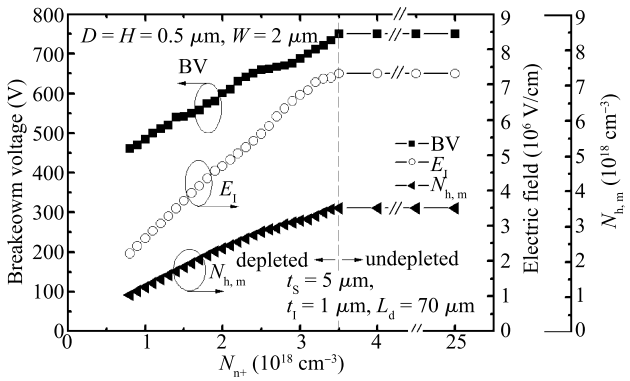

Fig. 8. Influences of N_{n+} on BV, E_I and the maximal hole concentration $N_{h,m}$.

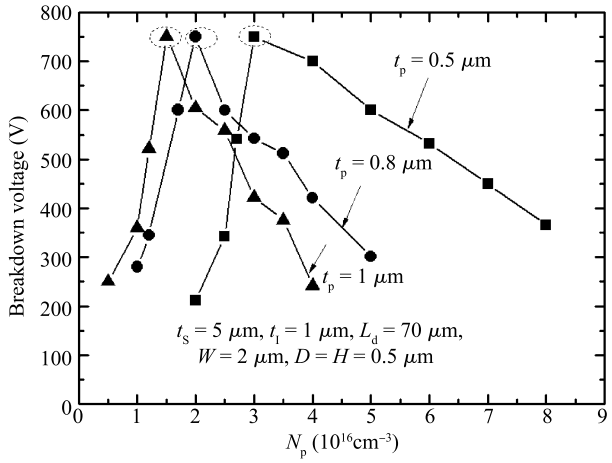

Fig. 9. Dependence of p-top layer thickness t_p and concentration N_p on BV.

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