Design and implementation of adaptive slope compensation in current mode DC–DC converter*

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Abstract: To improve the compensation for the inherent instability in a current mode converter, the adaptive slope compensation, giving attention to the problems of the traditional compensation on compensation accuracy, loading capability and turning jitter, is presented. Based on the analysis of current loop, by detecting the input and output voltage, converting the adaptive slope compensation current, the compensation of the current loop is optimized successfully. It can not only improve the compensation accuracy but also eliminate the over compensation, the turning jitter and the poor loading capability in the reported slope compensation. A power supply chip with adaptive slope compensation has been fabricated in a 0.35 μm CMOS process. The measurement results show that the chip starts up and operates steadily with the constant current limit under conditions of 5 V input voltage, from 10% to 100% duty cycle.

Key words: current mode; slope compensation; current limit; loading capability
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1. Introduction

With the fast development of process technology, the internal power of an SOC is gradually becoming lower and lower nowadays. The direct advantage of the low power is low dissipation, but the noise tolerance is also decreasing. The characteristics of the system can be affected by a small voltage fluctuation evidently. Therefore, the design and implementation of a power supply for an SOC including excellent loop stability are becoming difficult and challenging.

The current mode DC–DC converter is widely applied due to its advantages of better dynamic performance, high precision, large gain-bandwidth and limited current protection instantaneously, but there is an inherent instability when the duty cycle exceeds 50%. So, stability is often maintained in such current mode switching converters by adjusting the current derived signal used to control the converter with a slope compensation signal, which should ensure the loop stability and exert no influence on the other characteristics. The reported compensation circuit provides solutions to the inherent instability problem in Refs. [1–8]. The traditional slope compensation circuit is designed by the linear slope compensation, which will lead to two problems: one is over compensation; the other is poor loading capability without the especial self-calibration. Then the improved method is introduced by piecewise linear slope compensation[1−3]. But there are still some problems: (1) the fatal one is the jitter at the turning point of the piecewise; (2) in the fixed slope range, the slope compensation is still beyond the target value. So, in this paper, we deduce the principle of the slope compensation in the current mode DC–DC converter newly, and propose a kind of adaptive slope compensation avoiding the above problems.

Finally, through theory calculation, the simulation with HSPICE, and the layout with Virtuoso software, a monolithic current mode DC–DC buck converter with proposed adaptive slope compensation has been fabricated with a 0.35 μm CMOS process for validation. Measurement results show that the design and implementation of the loop compensation has good performance, and then it can be widely used in the current mode converter with preferable characteristics.

2. System design

The diagram of the power system with the peak current mode DC–DC converter is shown in Fig. 1. In the DC–DC converter, M1 is the main switch and M2 is the synchronous switch; the loop filter is composed of L_0, C_0 and $R_{\rm ERS}$; the feedback and error amplifier consists of $R_{\rm FB1}$, $R_{\rm FB2}$ and an error amp; the modulator is formed by PWM and logic. The voltage loop stability is designed by the cancellation of pole-zero in the output of the error amp, which is described in Section 3 in detail. Through the DAC control, the system soft start is obtained[9]. Also, the proposed slope compensation is achieved by the adaptive slope compensation by the slope block. Since the same gate voltage of M1 and M3, the system can sample the inductor ramp current in the power switch M1 on state from the voltage across the $R_{\rm SENSE}$, and the peak current can be controlled too. To improve the system efficiency in light load, the Zero comparator samples the inductor current in the synchronous state from the voltage across the $R_{\rm CROSS}$, the inductor current can be shut off when the current equals to zero, preventing the inductor current to ground. This mode is usually called power save mode[10], then the power dissipation is decreased rapidly, the converter efficiency is improved directly. The fault control unit, including over-temperature protection, over-voltage protection, and under-voltage protection, protects the system beyond the recommended operating conditions.

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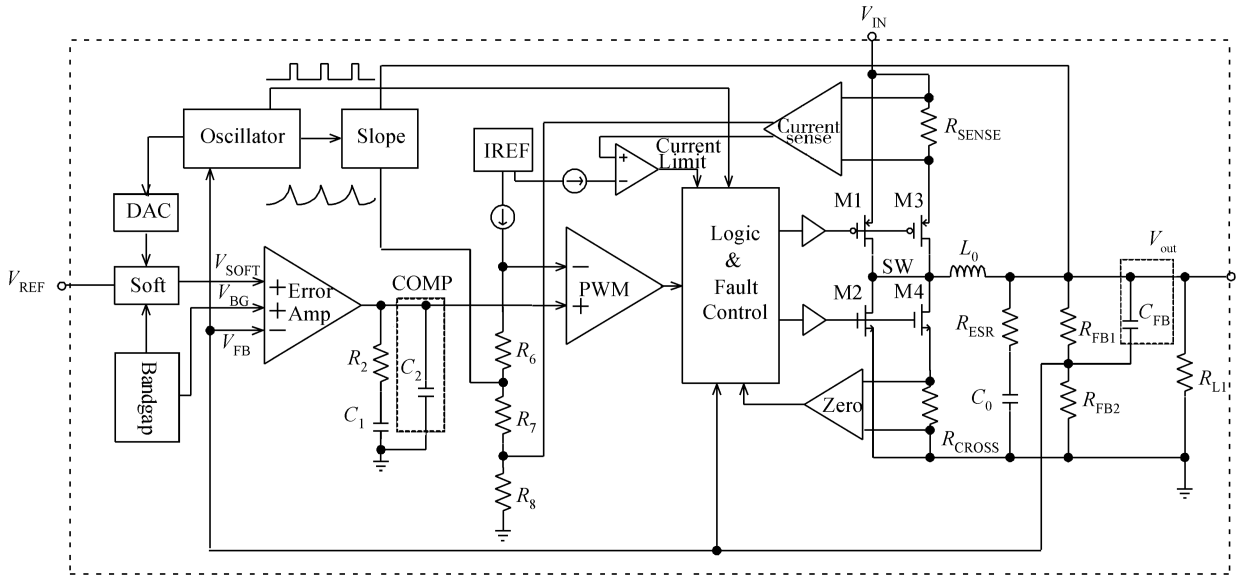


Fig. 1. Diagram of the power system.

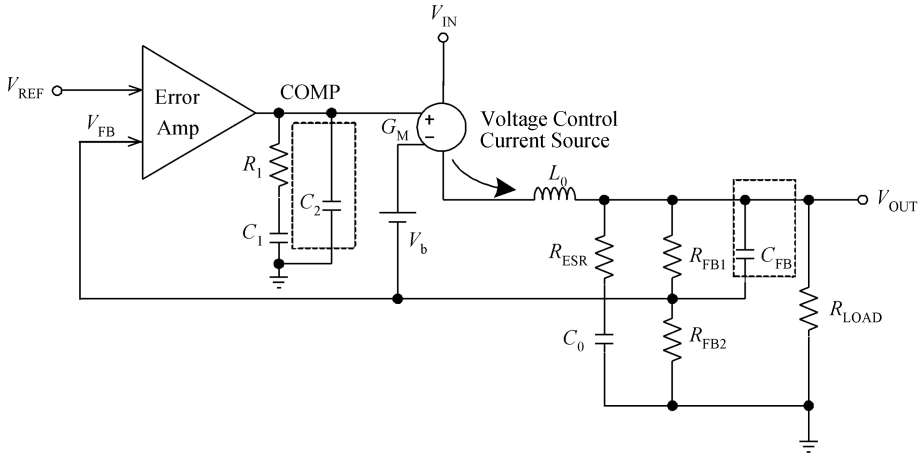


Fig. 2. Diagram of the loop.

3. Proposed slope compensation design

3.1. Loop stability

The dual loop control in switching power supply has the better system stability and fast transient response, which has become the mainstream in recent years. And the voltage loop is controlled through the COMP node, as the output of the internal transconductance error amplifier is shown in Fig. 2 simply. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system. The DC gain of the voltage feedback loop A_{VLOOP} is given by

$$A_{VLOOP} = \frac{V_{FB}}{V_{OUT}} A_{EA} G_M R_{LOAD}, \tag{1}$$

where V_{FB} is the feedback voltage, A_{EA} is the error amplifier voltage gain, G_M is the current sense transconductance and R_{LOAD} is the load resistor value. The system has two poles of importance. One is due to the compensation capacitor (C_1) and the output resistor of the error amplifier, and the other is due to the output capacitor (C_0) and the load resistor. These poles are located at

$$f_{P1} = \frac{1}{2\pi \dfrac{V_{EA}}{G_{EA}} C_1}, \tag{2}$$

$$f_{P2} = \frac{1}{2\pi R_{LOAD} C_0}, \tag{3}$$

where G_{EA} is the error amplifier transconductance. Besides these two poles, the voltage loop also has one zero of importance due to the compensation capacitor (C_1) and the compensation resistor (R_1), which is located at

$$f_{Z1} = \frac{1}{2\pi R_1 C_1}. \tag{4}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and a high ESR value. The zero is due to the ESR and capacitance of the output capacitor. In this case, a third pole set by the compensation capacitor (C_6) and the compensation resistor (R_3) is used to compensate

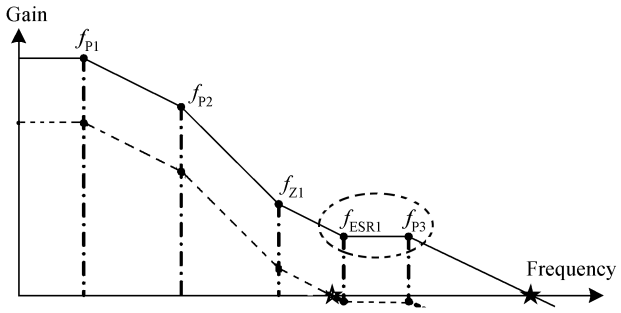


Fig. 3. Pole and zero location of the loop.

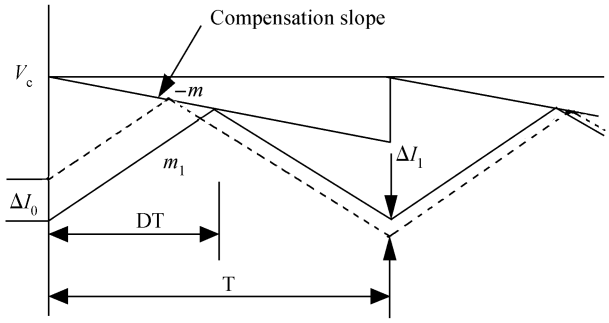


Fig. 4. Loop curve with slope compensation.

the effect of the ESR zero on the loop gain. These two ESR zero and compensation pole are located at

$$f_{\mathrm{ESR}} = \frac{1}{2\pi R_{\mathrm{ESR}} C_0}, \tag{5}$$

$$f_{\mathrm{P3}} = \frac{1}{2\pi R_1 C_2}. \tag{6}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency, as shown in Fig. 3.

3.2. Slope compensation principle

The PWM (pulse width modulation) function occurs for current-mode control, except that the ramp is created by monitoring the inductor current. This signal is comprised of two parts: the ac ripple current, and the dc or average value of the inductor current. The output of the current-sense amplifier is summed with a voltage ramp through the resistor at the inverting input of the PWM comparator. For current-mode control, the ideal steady-state modulator gain may be modified depending upon whether the voltage ramp is fixed, or proportional to some combination of inductor and bias current. Further modification of the gain is realized when the input and output voltages are perturbed to derive the effective small-signal terms. However, the concepts remain valid, despite small-signal modification of the ideal steady-state value. The difference between the average inductor current and the dc value of the sampled inductor current can cause instability for certain operating conditions. This instability is known as sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of the next switching cycle. Subharmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding an extra ramp (slope compensation) to the current-sense signal prevents this oscillation. It can be understood from the following detailed description.

For PWM duty cycles greater than 50%, the fixed frequency current mode converters require a slope compensation to avoid sub-harmonic oscillation. The higher the duty cycle is, the greater the slope compensation required[8−10]. The principle of operation is described in Fig. 4. V_{C} is the output signal of the error amplifier, the solid line is the inductor current curve with no distortion, the dotted line is the inductor current curve with ΔI_0 distortion, D is the duty cycle, T is the switching cycle, m_1 is the slope of rise inductor current, and m_2 is the slope of fall inductor current. If there is no slope compensation, it can be given by

$$m_1 = \frac{V_{\mathrm{IN}} - V_{\mathrm{OUT}}}{L}, \tag{7}$$

$$m_2 = \frac{V_{\mathrm{OUT}}}{L}. \tag{8}$$

In the CCM (continue conduction mode), then

$$\frac{m_2}{m_1} = -\frac{D}{1-D}, \tag{9}$$

$$\Delta I_1 = \Delta I_0 \frac{m_2}{m_1}. \tag{10}$$

From Eq. (10), we can see that if the duty is less than 50%, ΔI_1 is attenuated periodically and the system loop is conclusive, but if the duty is larger than 50%, ΔI_1 increases periodically, the system loop is aborted and the loop is unstable. So the slope compensation is introduced to stabilize the loop. Once the voltage V_{C} adds the slope compensation as m, shown in Fig. 4, then

$$\Delta I_1 = \Delta I_0 \frac{m_2 + m}{m_1 + m}. \tag{11}$$

By the slope compensation, Equation (11) can be designed as

$$\left|\frac{\Delta I_1}{\Delta I_0}\right| = \left|\frac{m_2 + m}{m_1 + m}\right| < 1. \tag{12}$$

From Eq. (12), it is observed that the slope compensation makes that ΔI_1 is attenuated periodically in the duty cycle above 50%. So the system loop becomes conclusive and stable. The compensation curve is shown in Fig. 4 with the slope m. But the slope has a certain relationship with the slope m_1 and m_2, as expressed by Eq. (13), which is determined by the duty cycle.

$$m > \frac{1}{2}(m_2 - m_1). \tag{13}$$

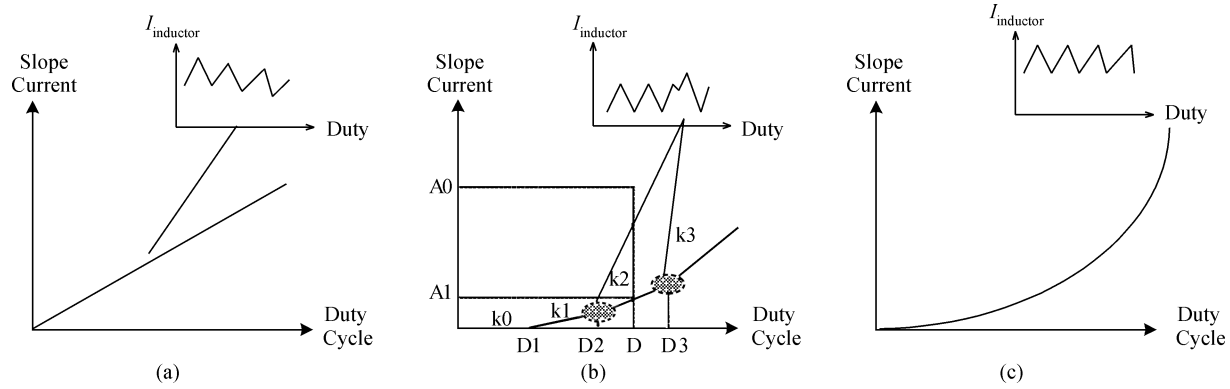


Fig. 5. (a) Linear slope compensation. (b) Piecewise linear slope compensation. (c) Adaptive slope compensation.

4. Proposed slope compensation and current limit implementation

The traditional slope compensation has been reported in Refs. [1, 2], as summarized in Figs. 5 (a) and 5(b). Figure 5(a) is the most common and simplest slope compensation, which utilizes the linear slope compensation in every duty cycle. It will result in more slope surplus, especially in low duty cycle, and affect the peak current limit of the DC–DC converter. Then the piecewise linear slope compensation is widely used in a certain application field in Fig. 5(b). But because of the serious jitter in the turning of the piecewise linear slope compensation, this method is difficult to operate at a continuous duty cycle range. In order to improve the above considerations, the proposed adaptive slope compensation can be designed in Fig. 5(c). Then there is no slope compensation surplus, and the current limit can be independent of the slope compensation. So, It can not only improve the compensation accuracy but also eliminate the over compensation, the turning jitter and poor loading capability in the proposed dynamic slope compensation.

Generally, in the linear and piecewise linear slope compensation, taking $m_1 = 0$ as the worst case, then the maximum slope compensation is added in the entire duty cycle range, which is the fundamental reason for the discussion problems. But in this paper, the accurate slope compensation can be calculated by substituting Eqs. (7) and (8) in Eq. (13),

$$\begin{aligned} m > \frac{1}{2}(m_2 - m_1) &= \frac{1}{2}\left(\frac{V_{\rm OUT}}{L} - \frac{V_{\rm IN} - V_{\rm OUT}}{L}\right) \\ &= \frac{1}{2}\left(\frac{2V_{\rm OUT} - V_{\rm IN}}{L}\right) \\ &= \frac{V_{\rm OUT} - \frac{1}{2}V_{\rm IN}}{L}. \end{aligned} \tag{14}$$

Now consider Eq. (14). The deduced slope compensation contains three parameters: input voltage $V_{\rm IN}$, output voltage $V_{\rm OUT}$ and inductor L. When we have selected the certain inductor, only two parameters are left. Assuming the inductor is 1 μH, the deduced slope compensation is simplified by

$$m > V_{\rm OUT} - \frac{1}{2}V_{\rm IN}. \tag{15}$$

Therefore, the implementation circuit of the proposed slope compensation is shown in Fig. 6. The right part of the bottom block is the current sense circuit, and the left part is the proposed slope compensation circuit. OP1, R_2, M15 and M16 make up the V–I converter from the output voltage $V_{\rm OUT}$. OP2, R_3–R_5, M10 and M11 make up the V–I converter from the input voltage $V_{\rm IN}$. The results can be expressed by

$$I_1 = \frac{V_{\rm OUT}}{R_2}, \tag{16}$$

$$I_5 = \frac{V_{\rm IN}\dfrac{R_5}{R_4 + R_5}}{R_3}, \tag{17}$$

where $R_4 = R_5$, $R_2 = R_3 = R$, then

$$I_1 = \frac{V_{\rm OUT}}{R}, \tag{18}$$

$$I_5 = \frac{\frac{1}{2}V_{\rm IN}}{R}. \tag{19}$$

Through the current mirror setting, the current I_1 equals I_4, and the current I_5 equals I_3. It is inevitable that the current I_2 flowing through M13 is the difference between I_3 and I_4,

$$I_2 = I_4 - I_3 = I_1 - I_5 = \frac{V_{\rm OUT} - \frac{1}{2}V_{\rm IN}}{R}. \tag{20}$$

It can be seen that Equations (20) and (15) are the same except for the coefficient of R. So the adaptive slope compensation can be achieved by the left part of Fig. 6, and the waveform is shown in Fig. 7. At the T_1 range, the adaptive slope compensation will be added at the input of the PWM comparator. T_2 is the minimum duty cycle, there isn't need the slope compensation. With the duty cycle increasing, the slope compensation current I_2 is too large. So, the resistor R_7 is used to trade off the large slope compensation current.

From the right part of bottom block in Fig. 6, we can see that the voltage $V_{\rm RSENSE}$ across the resistor $R_{\rm SENSE}$is a function of inductor current, so this voltage can be selected to control the peak current. Because the $R_{\rm DSON}$ of M3 is much less than $R_{\rm SENSE}$ by design, $V_{\rm RSENSE}$ can be expressed by

$$V_{\rm SENSE} = V_{\rm IN} - V_{\rm SW} = I_L R_{\rm M1\_DSON}, \tag{21}$$

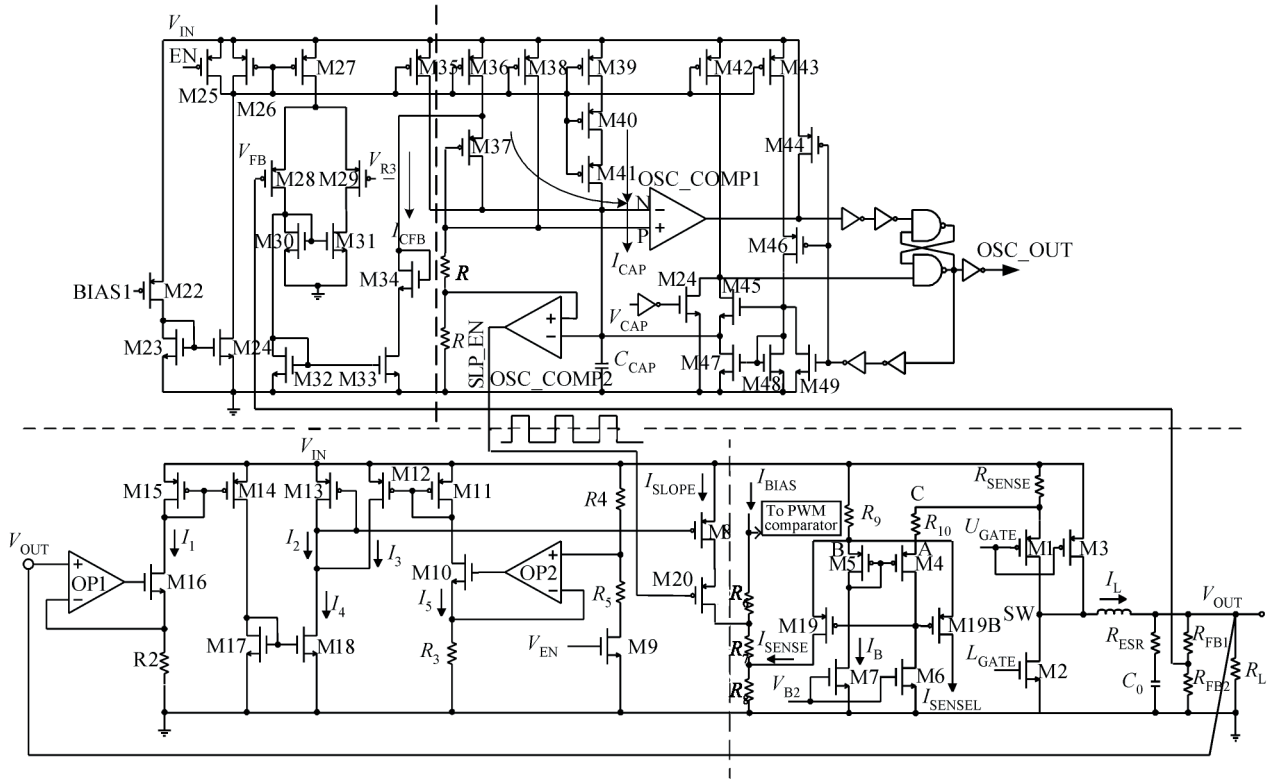


Fig. 6. Circuit of the proposed slope compensation.

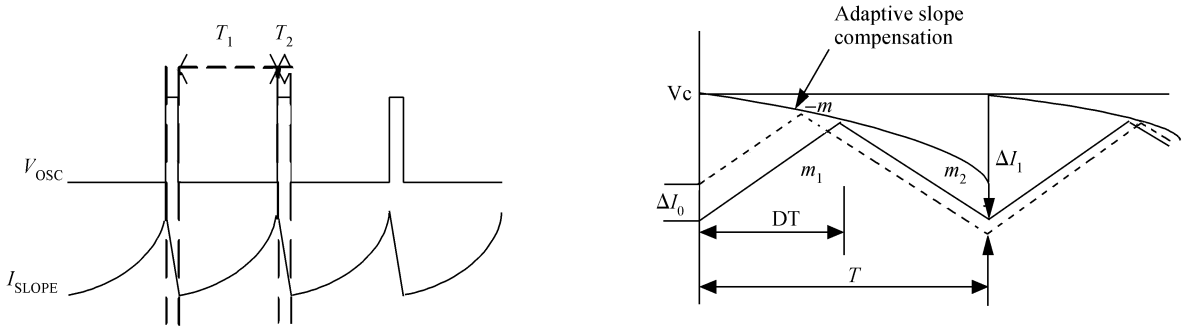


Fig. 7. Waveform of the slope compensation.

$$V_C = V_{IN} - (V_{IN} - V_{SW})\frac{R_{SENSE}}{R_{SENSE} + R_{M3\_RDSON}} \approx V_{SW}, \quad (22)$$

$$V_C - R_{10}I_B = V_{IN} - R_9(I_B + 2I_{SENSE}), \quad (23)$$

$$I_{SENSE} = I_{SENSEL} = \frac{1}{4}\left(\frac{V_{IN} - V_C + R_{10}I_B}{R_9} - I_B\right). \quad (24)$$

When the inductor current reaches the peak current limit threshold, we can control the state of the main switch M1 by the current limit comparator with the current $I_{SENSENL}$, which makes the peak current limit unrestricted by the slope compensation added at the inverting input of the PWM comparator with the current I_{SENSEN}. This is mainly because the current I_{SENSEN} and $I_{SENSENL}$ control the current loop operation and the current limit, respectively.

In Fig. 6, the top block is the oscillator providing the trigger pulse to conduct the power device and the control pulse to enable the adaptive slope compensation block by OSC_OUT and SLP_EN signals, respectively. During the start-up of the switching power supply, the inductor current will increase very fast due to the low output, and there will be the large peak inductor current and the output voltage ripple at the output of the converter. Here, it can be avoided by the decreased switch frequency, which is achieved by the transistor M28–M34. When the feedback voltage V_{FB} is below the 0.3 V reference voltage, the current of M30 and M32 is increased too, which will result in an increase in I_{CFB} through M34. Then the charging current of the oscillator cap is decreased accordingly to reduce the switching frequency.

5. Experimental results and discussion

The current mode DC–DC converter with the proposed adaptive slope compensation has been fabricated in a 0.35 μm CMOS process. The micrograph of the IC is shown in Fig. 8, and the total layout area is only 0.8 mm^2. The converter has

Table 1. Comparison with some reference.

Parameter	Ref. [1]	Ref. [3]	Ref. [5]	This work
Process	0.5 μm CMOS	0.6 μm BCD	–	0.35 μm CMOS
Input voltage (V)	2–5.5	2.5–5.5	4.75–23	2.5–5.5
Duty cycle test (%)	11–100	—	D_{MAX} = 90%	10–100
Supply current (μA)	—	—	1300	200, 28 (No switching)
Current limit (A)	0.9–1.2 @ D = 20%–90%	1.5 @ V_{IN} = 2.5 V 3 @ V_{IN} = 5.5 V	Typical = 5.8, Minimum = 4	4 @ D = 10%–100%
Loading capability improved (%)	30	20	—	> 60
Efficiency (%)	94	93	95	96
Load transient (V/A)		1.3	0.12	0.08
Output voltage accuracy (%)	±2	—	±3	±1.3

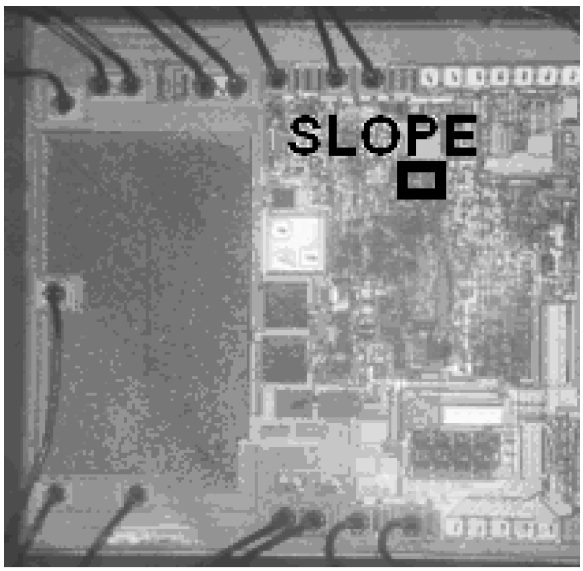


Fig. 8. Micrograph of the proposed power system.

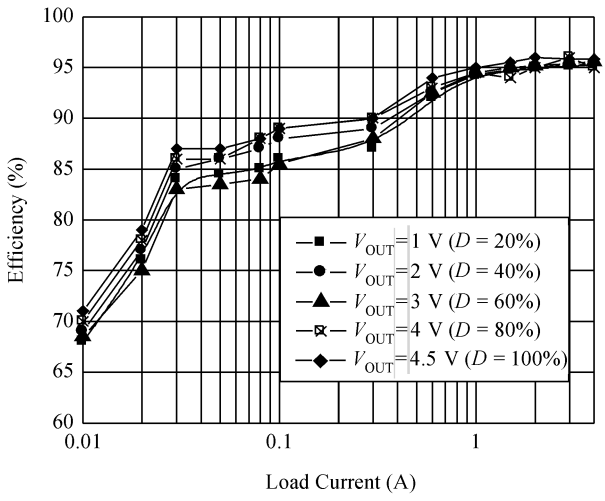
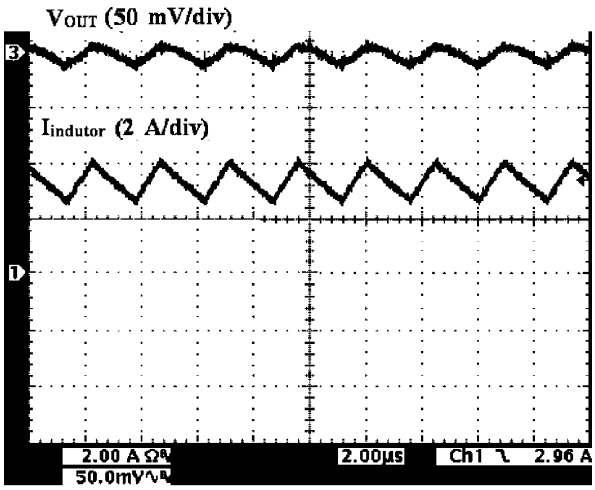
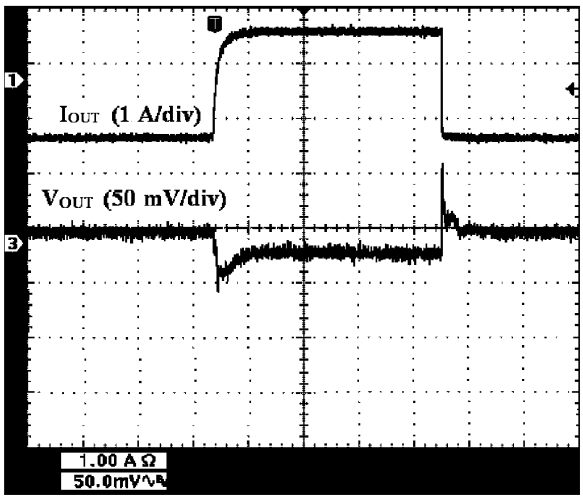


Fig. 9. Efficiency versus load and duty cycle.



(a)



(b)

Fig. 10. Test operation waveform. (a) Nominal operation. (b) Load transient (test condition: V_{OUT} = 2.5 V, C_{in} = 10 μF, C_{out1} = 4.7 μF, L = 1 μH).

only a 200 μA quiescent current, including the current consumption of all other protection blocks. Figure 9 shows the conversion efficiency versus the duty cycle. The test operation waveform of the proposed converter is shown in Fig. 10.

Figure 9 shows the converter efficiency curves versus the duty cycle, respectively, in the case of 20%, 40%, 60%, 80% and 100% duty cycle, which shows that the efficiency is up to 96% in the load range from 10 mA to 4 A, and the lowest efficiency is also about 70% at 10 mA load, indicating that power save mode made and adaptive slope compensation are important contributions to the increase of light load efficiency. Also, the efficiency under different duty cycle results shows that the loop stability and the anti-overcompensation are guaranteed by the novel adaptive slope compensation design. At the same time, Figure 11 shows the current limit versus the duty cycle aiming at the loading capability. It can be seen that the

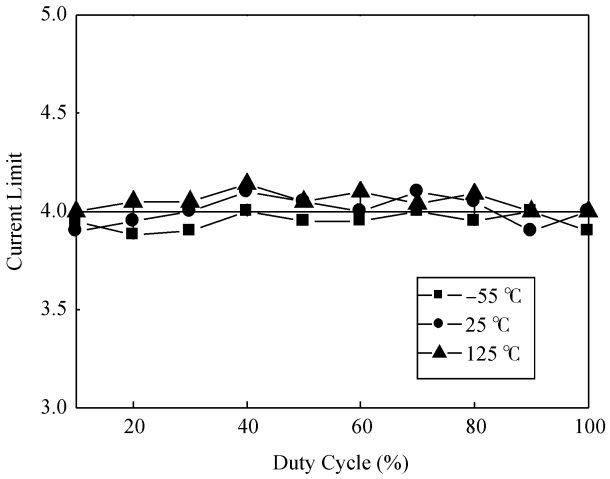


Fig. 11. Measurement current limit versus duty cycle.

current limit is independent of the duty cycle, and then poor loading capability in the traditional method is improved.

So, from the experimental measurement results, the proposed adaptive slope compensation circuit is verified in a practical application. Meanwhile, compare to the methods proposed in Refs. [1, 3], the newly designed current loop compensation is given more attention to the accuracy of the compensation value, the over-compensation, the loading capability and the implementation, as summarized in Table 1. The great improvements of proposed slope compensation can be summarized as (1) the accuracy of the slope compensation is achieved by the adaptive detecting of the output and input; (2) the over-compensation in the linear and piecewise linear slope compensation is eliminated; (3) the turning jitter in the piecewise slope compensation is avoided by the continuous slope gradual change; and (4) the loading capability is also guaranteed by the slope compensation and the current loop control separately.

6. Conclusion

An adaptive slope compensation design of current mode switching power supply is presented in this paper based on analyzing the voltage loop and current loop stability in detail. The design and measured results are reported on the prototype DC–DC converter, which successfully demonstrates the design techniques of this paper and the better voltage and current loop stability of DC–DC converters in portable applications. The measurement results show that the chip starts up and operates steadily under conditions of 5 V input voltage, constant current limit, from 10% to 100% duty cycle. Compared with the previous work summarized in discussions, it provides dynamic slope compensation, high efficiency, improved loading capability and loop stability.

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