# A low voltage and small hysteresis $C_{60}$ thin film transistor*

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**Abstract:** Organic thin film transistors with $C_{60}$ as an n-type semiconductor have been fabricated. A tantalum pentoxide ($Ta_2O_5$)/poly-methylmethacrylate (PMMA) double-layer structured gate dielectric was used. The $Ta_2O_5$ layer was prepared by using a simple solution-based and economical anodization technique. Our results demonstrate that double gate insulators can combine the advantage of $Ta_2O_5$ with high dielectric constant and polymer insulator for a better interface with the organic semiconductor. The performance of the device can be improved obviously with double gate insulators, compared to that obtained by using a single $Ta_2O_5$ or PMMA insulator. Then, a good performance n-type OTFT, which can work at 10 V with mobility, threshold voltage and on/off current ratio of, respectively, 0.26 $cm^2/(V{\cdot}s)$, 3.2 V and $8.31 \times 10^4$, was obtained. Moreover, such an OTFT shows a negligible "hysteresis effect" contributing to the hydroxyl-free insulator surface.

**Key words:** organic thin film transistors; $C_{60}$; double gate dielectrics
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## 1. Introduction

The potential applications of organic thin film transistors (OTFTs) have been realized as a result of their attractive features, such as low-temperature processing and mechanical flexibility compared with inorganic transistors[1−3]. And the performance of OTFTs has been improved rapidly in the last decade. However, the operation mode of OTFTs still cannot meet all of the requirements of applications due to the low carrier mobility and high work voltage. The utilization of high dielectric constant (high-$k$) inorganic dielectrics should be considered reasonably as a way to lower the work voltage, because such dielectrics can enhance the accumulation of carriers under a low gate voltage[4, 5]. On the other hand, since OTFTs work in the accumulation regime and most of the modulated charge lies within the first 10 nm in the semiconductor near the interface, the quality of insulator, especially the semiconductor/insulator interface, can strongly influence the performance of OTFTs. Unfortunately, the high-$k$ inorganic oxides usually have hydrophilic and rough surfaces, which can decrease the performance of OTFTs[6, 7]. In contrast, polymer dielectrics have the advantage in easily making film by solution-processing to form a layer with a smooth surface. We note that, up to now, the higher mobility both in p-type and n-type OTFTs has often been obtained based on a polymer dielectric, which indicates that the high quality interface can form easily between the polymer dielectric and the semiconductor[8, 9]. However, the low dielectric constant of the polymer dielectrics may make their use limited in further applications. Although the work voltage can also be lowered by using ultra-thin polymer insulators[10], it is still very difficult to fabricate ultra-thin pinhole-free films with good insulator characteristics.

To date, most reports focus on the p-type (hole transport) OTFTs and have achieved good performances[11]. In order to realize applications, both p-type and n-type transistors are needed and should have a comparable performance. Thus, to fabricate high performance n-type (electron transport) OTFTs are demanded recently[12, 13]. Previously, there have been several studies on the double-layer gate dielectrics for the fabrication of n-type inorganic transistors based on ZnO[14, 15]. In this paper, a good performance n-type OTFT, which also includes double insulator layers of a spin-coated PMMA film covering anodized $Ta_2O_5$, was demonstrated. This kind of OTFT has a low voltage, high mobility and a negligible "hysteresis effect".

## 2. Experiment

Devices with three different structures were fabricated. Figure 1(a) shows the structure of Ta/$Ta_2O_5$/$C_{60}$/Al, referred to as Device A. Figures 1(b) and 1(c) show the structures of Ta/PMMA/$C_{60}$/Al and Ta/$Ta_2O_5$/PMMA/$C_{60}$/Al, referred to as Devices B and C. The fabrication of the films in the devices was as follows. 600 nm tantalum (Ta) films were sputtered on cleaned glasses. The $Ta_2O_5$ film was formed on the Ta film by anodic oxidation (anodization). A Keithley 2400 source unit was used to control the current–voltage. Anodization was carried out with a constant current density of 0.2 $mA/cm^2$ in 2.1 g/L citric acid solution, and the constant current across the growing $Ta_2O_5$ layer was maintained by ramping the voltage up to an anodization voltage of 100 V[16]. Then, the voltage was maintained constant. According to the anodization ratio of 2 nm/V[17], the corresponding thickness of the $Ta_2O_5$ layer was 200 nm. After anodization, the $Ta_2O_5$ films were then ultrasonically cleaned and dried in a vacuum oven. To form double insulators, a 50 nm thick PMMA polymer dielectric layer was prepared by spin-coating from a chlorobenzene solution (2 wt.%) on top of $Ta_2O_5$. In addition, a 430 nm thick PMMA layer was prepared from a chlorobenzene solution (5.5 wt.%)

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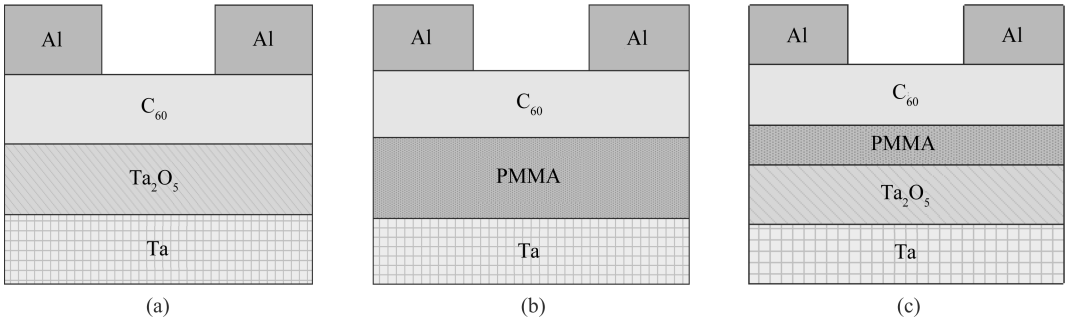


Fig. 1. Schematic cross-sectional structures of OTFTs with (a) $Ta_2O_5$ insulator, (b) PMMA insulator, and (c) $Ta_2O_5$/PMMA insulators.

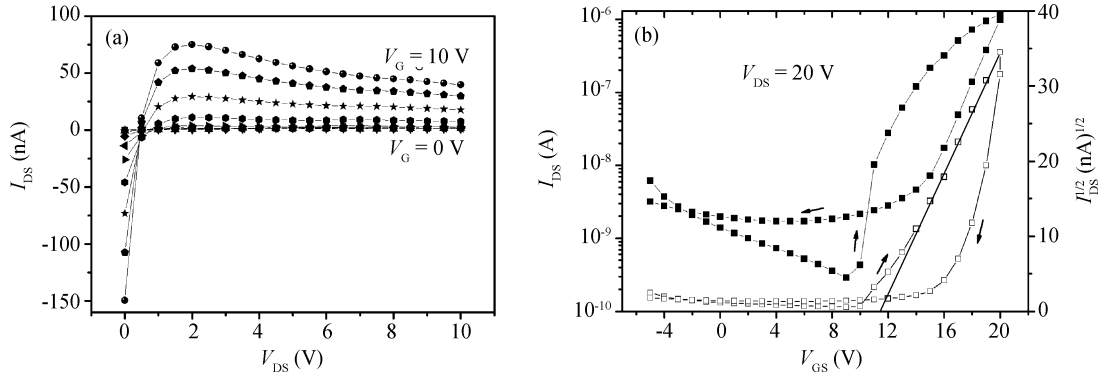


Fig. 2. Electrical characteristics of the OTFT with a $Ta_2O_5$ single insulator. (a) $I_{DS}$ versus $V_{DS}$ output curve. (b) $I_{DS}^{1/2}$ and lg $I_{DS}$ versus $V_{GS}$ transfer curve.The voltage is applied in Al electrode.

on top of Ta to fabricate OTFTs with a single polymer insulator. Then, 80 nm thick $C_{60}$ film was thermally deposited at a rate of 1 Å/s in a vacuum under of $3 \times 10^{-4}$ Pa pressure as the semiconducting layer. The substrates were maintained at room temperature during deposition. Finally, aluminum was evaporated through a shadow mask as the top contact source (S) and drain (D) electrodes. The length ($L$) and width ($W$) of the channel were 100 $\mu$m and 10 mm, respectively.

The electric characteristics of the OTFTs were measured at room temperature in a nitrogen atmosphere with an Agilent 4155C semiconductor parameter analyzer. The surface morphology of the films was examined by atomic force microscopy (AFM, DI MultiMode Nanoscope IIIa, Veeco).

## 3. Results and discussion

Figure 2(a) shows the output characteristics ($I_{DS}$–$V_{DS}$) of Device A (single $Ta_2O_5$ insulator). A very poor performance was obtained. When $V_{GS} = 10$ V, the output current was only 39.7 nA. Moreover, as a drawback existed in most high-$k$ inorganic dielectrics, a large leakage current was observed in this device too. It should be mentioned that a decrease in $I_{DS}$ when the $V_{DS}$ voltage increases above pinch-off in the saturated region could be observed from the output characteristics. This effect has been reported in fullerene n-type OTFTs and may be related to trapping in the semiconductor[18]. After the first scan of electric characteristics to measure the output curve, another scan was carried out in order to obtain the transfer curve. We note that there are some obvious differences in the current data between the output curve and the transfer curve. Figure 2(b) shows the transfer characteristics of Device A. The carrier mobility ($\mu$) can be calculated at the saturation regions from a plot of the square root of the drain current ($I_{DS}^{1/2}$) versus $V_{GS}$ by the following equation,

$$I_{DS} = \frac{WC_i}{2L}\mu(V_G - V_T)^2, \quad (1)$$

where $W$ is the channel width, $L$ is the channel length, $C_i$ is the capacitance per unit area of the insulator and $V_T$ is the threshold voltage. The $C_i$ of the gate insulators was measured to be about 84 nF/cm$^2$ by using a Ta/$Ta_2O_5$/Al (MIM) structure. For a single $Ta_2O_5$ layer, a low threshold voltage $V_T$ was expected because more charges can be induced easily under a low $V_{GS}$ and a conducting channel may form in the early stage exclude other reasons. However, since $V_T$ is closely related to the charge state at the semiconductor and insulator interface, here the large $V_T$($\approx$ 11.5 V) indicates that the anodized $Ta_2O_5$ films have too many charge traps at the interface with the $Ta_2O_5$/$C_{60}$. Besides the large $V_T$, the quite large "hysteresis effect", which could lead the threshold voltage shift, was observed in the current–voltage characteristics during the sweep direction of the gate voltage from –5 to 20 V (off to on state) and 20 to –5 V (on to off state). The hysteresis effect may also be attributed to the electron traps at the interface with the $Ta_2O_5$/$C_{60}$. Indeed, by modifying the deposition method and annealing of the $Ta_2O_5$ film to attain a better interface, Pereira *et al*. have shown that the interface oxide charge density and interface trapped charges can be decreased. Thus the hysteresis can be reduced[19]. Consequently, the $\mu$ of Device A was only 0.004 cm$^2$/(V· s) and the on/off current ratio was less than $10^3$. The advantage of the

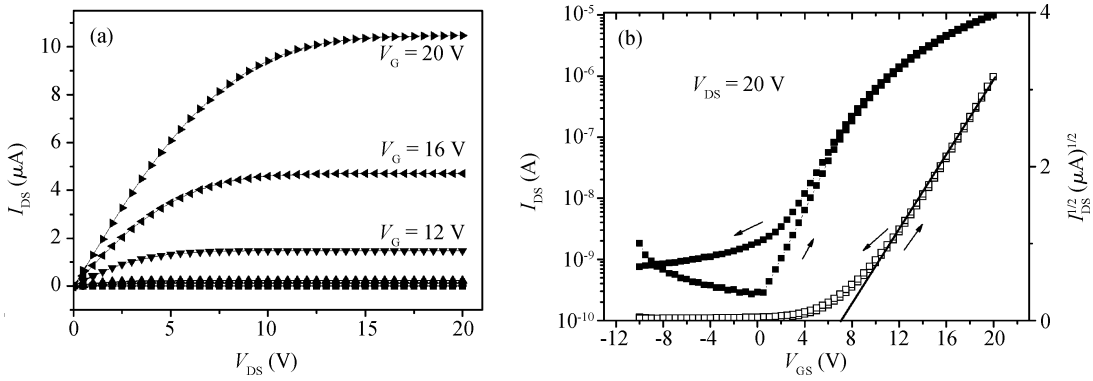


Fig. 3. Electrical characteristics of the OTFT with a PMMA single insulator. (a) $I_{DS}$ versus $V_{DS}$ output curve. (b) $I_{DS}^{1/2}$ and lg $I_{DS}$ versus $V_{GS}$ transfer curve.

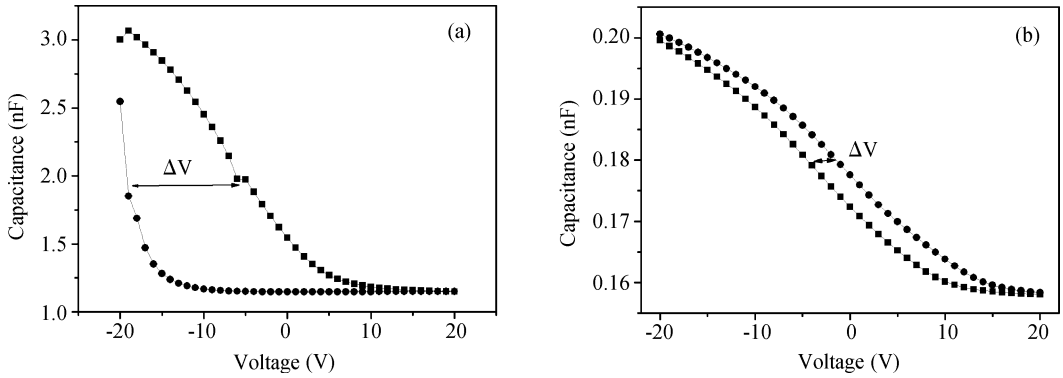


Fig. 4. $C$–$V$ characteristic curve of the (a) Ta/$Ta_2O_5$/$C_{60}$/Al and (b) Ta/PMMA/$C_{60}$/Al MIS structures. The voltage is applied in Al electrode.

high-$k$ insulator was not exhibited at all.

Figure 3(a) shows the output characteristics of Device B (single PMMA insulator). The performance shows good and clear saturation behavior. When $V_{GS}$ = 20 V, the output current was 10.46 $\mu$A. This performance is obviously higher than that of Device A. Figure 3(b) shows the following transfer characteristics. A negligible "hysteresis effect" was observed, which indicates fewer electron traps in the PMMA/$C_{60}$ interface than in the $Ta_2O_5$/$C_{60}$ interface. However, the work voltage and the threshold voltage $V_T$ ($\approx$ 7 V) were still a bit large due to the low dielectric constant of the polymer dielectric. The extracted $\mu$ and on/off ratio are 0.194 cm$^2$/(V·s) and $3.46\times10^4$ in Device B.

It is confirmed that the interface quality of the PMMA/$C_{60}$ is better than that of the $Ta_2O_5$/$C_{60}$ from analyzing the electric characteristics. In order to further understand more details, we then measured the morphology of the insulator's surface. Indeed, we measured the morphology of the insulator surface by AFM (not shown here)[16]. The surface roughness of the $Ta_2O_5$ was 2.11 nm. In contrast, the $Ta_2O_5$/PMMA film showed a very smooth surface. When 50 nm PMMA film coats upon the $Ta_2O_5$ film, the surface roughness was 0.3 nm, which could compare to that of single PMMA surface. PMMA solutions must have filled up the valley regions on the $Ta_2O_5$ surface[16]. Apparently, the smooth insulator surface is very helpful in improving the performance since it has been reported that a rough dielectric surface not only adds the surface traps but also causes the scattering and restricts the flow of charges[20]. On the other hand, it has pointed out that, in n-type OTFTs, OH-groups (silanol groups) appearing at the dielectric surface can trap electron easily, which could reduce the mobility and make a large hysteresis. Due to the report that $Ta_2O_5$ film has the property of trapping electrons because of oxygen vacancies in the film, the hydroxyl-free property of PMMA as another reason is also considered to contribute the excellent contact between PMMA film and $C_{60}$ film.

To investigate the trap densities at the interfaces of $Ta_2O_5$/$C_{60}$ and PMMA/$C_{60}$, capacitance–voltage ($C$–$V$) measurement of Ta/$Ta_2O_5$/$C_{60}$/Al and Ta/PMMA/$C_{60}$/Al structures was carried out. The frequency of measurement was 10 kHz. The applied voltage of Al electrode is changed between –20 and +20 V. The hysteresis swept forward and backward reflects the trap density at the insulator/$C_{60}$ interface or in the bulk of insulators, as shown in Figs. 4(a) and 4(b). The shifts of the flat-band voltages ($\Delta V$) are about 15 V and 3 V for the $Ta_2O_5$/$C_{60}$ and PMMA/$C_{60}$ structures. Assuming that $\Delta V$ originated from trapped electrons at the insulator/$C_{60}$ interface, then the density of the interface-traps ($N_t$) can be estimated by the following equation[21],

$$N_t \approx C_i \frac{\Delta V}{q}, \tag{2}$$

where $C_i$ is the capacitance per area of the insulator and $q$ is the elementary charge. Using this formula, we are able to estimate the trap density to be $7.87\times10^{12}$ cm$^{-2}$ for the $Ta_2O_5$/$C_{60}$ interface and $1.1\times10^{11}$ cm$^{-2}$ for the PMMA/$C_{60}$ interface. As

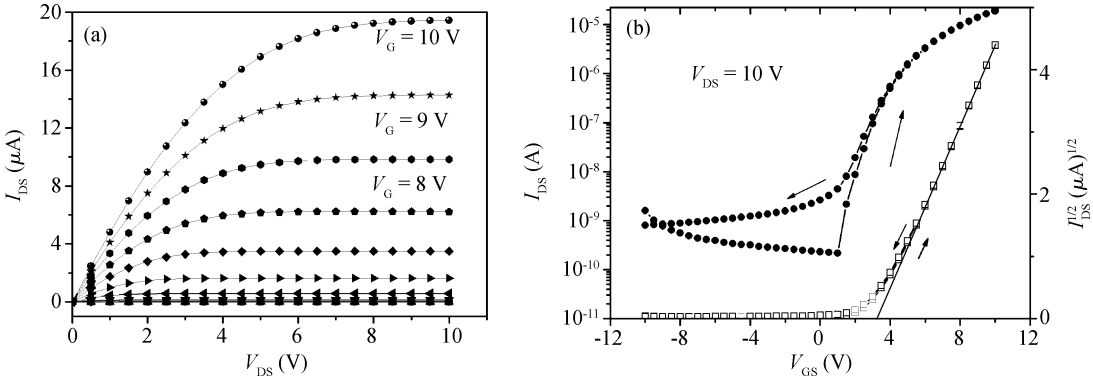


Fig. 5. Electrical characteristics of the OTFT with $Ta_2O_5$/PMMA double insulators. (a) $I_{DS}$ versus $V_{DS}$ output curve. (b) $I_{DS}{}^{1/2}$ and lg $I_{DS}$ versus $V_{GS}$ transfer curve.

Table 1. Parameters of the transistors.

| Insulator | $\mu$ (cm$^2$/(V·s)) | $V_T$ (V) | On/off ratio |
|---|---|---|---|
| $Ta_2O_5$ | 0.004 | 11.5 | $8.51 \times 10^2$ |
| PMMA | 0.194 | 7 | $3.46 \times 10^4$ |
| $Ta_2O_5$/PMMA | 0.26 | 3.2 | $8.31 \times 10^4$ |

seen, the trap density of the PMMA/$C_{60}$ interface is more less than $Ta_2O_5$/$C_{60}$ interface.

The best performance of the OTFT can be obtained with the double gate insulators. Figure 5(a) shows the output characteristics of Device C ($Ta_2O_5$/PMMA double insulators). The result also displays clear saturation behavior. A large output drain current of 19.4 $\mu$A can be achieved easily under a gate bias ($V_{GS}$) as low as 10 V. The following transfer characteristics of Device C are shown in Fig. 5(b). Besides the negligible "hysteresis effect", the best performance with mobility, threshold voltage and on/off current ratio of, respectively, 0.26 cm$^2$/(V·s), 3.2 V and $8.31 \times 10^4$ was obtained. Thus, we conclude that the double gate insulators can combine the advantage of $Ta_2O_5$ with high dielectric constant and polymer insulator for a better interface with an organic semiconductor. We must point out that by simply spincoating a PMMA layer on top of the $Ta_2O_5$, the total capacitance value will be reduced compared with that of a single $Ta_2O_5$. A 50 nm thickness of PMMA is reasonable here since it can smooth the $Ta_2O_5$ surface completely and avoid reducing the capacitance largely. Too thick PMMA film coverage upon $Ta_2O_5$ should not be carried out.

The properties of the OTFT with three different configurations are summarized in Table 1.

## 4. Conclusion

We have succeeded in obtaining an n-type OTFT based on $C_{60}$ with $Ta_2O_5$/PMMA double gate dielectrics. Compared to the $Ta_2O_5$ single dielectric, the $Ta_2O_5$/PMMA dielectrics have a much better insulating property and a much smoother surface. And compared to a single PMMA layer, the $Ta_2O_5$/PMMA dielectrics have obviously high capacitance. This kind of OTFT has the best performance, including low voltage, high mobility and negligible hysteresis effect. The performance of other n-type OTFTs may also be improved in the same way.

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