Nonlinear characterization of GaN HEMT*

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Abstract: DC I–V output, small signal and an extensive large signal characterization (load-pull measurements) of a GaN HEMT on a SiC substrate with different gate widths of 100 μm and 1 mm have been carried out. From the small signal data, it has been found that the cutoff frequencies increase with gate width varying from 100 μm to 1 mm, owing to the reduced contribution of the parasitic effect. The devices investigated with different gate widths are enough to work in the C band and X band. The large signal measurements include the load-pull measurements and power sweep measurements at the C band (5.5 GHz) and X band (8 GHz). When biasing the gate voltage in class AB and selecting the source impedance, the optimum load impedances seen from the device for output power and PAE were localized in the load-pull map. The results of a power sweep at an 8 GHz biased various drain voltage demonstrate that a GaN HEMT on a SiC substrate has good thermal conductivity and a high breakdown voltage, and the CW power density of 10.16 W/mm was obtained. From the results of the power sweep measurement at 5.5 GHz with different gate widths, the actual scaling rules and heat effect on the large periphery device were analyzed, although the effects are not serious. The measurement results and analyses prove that a GaN HEMT on a SiC substrate is an ideal candidate for high-power amplifier design.

Key words: GaN HEMT; load-pull measurements; optimum load impedance; power sweep measurement
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1. Introduction

Solid-state amplifiers are replacing traveling-wave-tube amplifiers in microwave power applications. However, the low operation voltages of solid-state devices lead to a large device periphery, resulting in high device and circuit complexity, and reducing production yield and reliability. Wide-band gap technologies, like GaN, can achieve a power density ten times higher than both silicon and GaAs, and higher voltage operation. Furthermore, the AlGaN/GaN heterostructure induces a very high electron density in the HEMT channel compared with standard AlGaAs/GaAs HEMT devices, which, in combination with the high saturated electron drift velocity, leads to an output power density that is higher than that reached in conventional high frequency semiconductor technologies[1−3]. These advantages will ultimately result in reduced circuit complexity, and improved gain, efficiency and reliability.

However, although GaN HEMTs offer important advantages for high power applications, GaN-based transistors are limited by some issues. Defects play a major role in limiting the state-of-the-art device's output power. The extremely high power density reached in the large periphery devices poses thermal degradation and reliability problems because AlGaN/GaN HEMTs suffer from self-heating and trapping effects[4]. In order to provide the mature technology based on GaN, it is fully understanding of the device technology, its reliability, and the development of circuit and system application, which needs an accurate power characterization system. Load-pull measurement is a straightforward to measure the transistor parameters such as the output-power, gain and efficiency under large-signal conditions[5]. When performing a load-pull measurement, using the tuner to determine the optimum load and source match, the reflection coefficient and optimum load impedance seen by the transistor can be known. Following that, the power sweep measurements are performed. The data of output power, PAE and gain as a function of the input power are investigated.

In this paper, the self-developed AlGaN/GaN HEMTs grown on a SiC substrate with a gate length of 100 μm and 1 mm are reported[6]. The nonlinear setup, complex calibration process and measurement of the load-pull characterization system are presented. The different nonlinear measurements in a large signal were performed, including the output power, transducer gain, power added efficiency as function of the load reflection coefficient and impedance at the C band (5.5 GHz) and X band (8 GHz). The data demonstrate the correct choice and compromise between the output power and the PAE as a function of the loading condition. The scaling properties of different gate width devices were investigated at a frequency of 5.5 GHz. Finally, at 8 GHz, operating in class AB, the output power and gain were measured with different drain voltages. The CW output power density of 10.16 W/mm can be reached. The results show that a GaN HEMT on a SiC substrate has a good thermal conductivity, high voltage breakdown and high load impedance.

2. Device technology

The devices were grown by a metal organic chemical vapour deposition (MOCVD) system on a 4H-SiC substrate.

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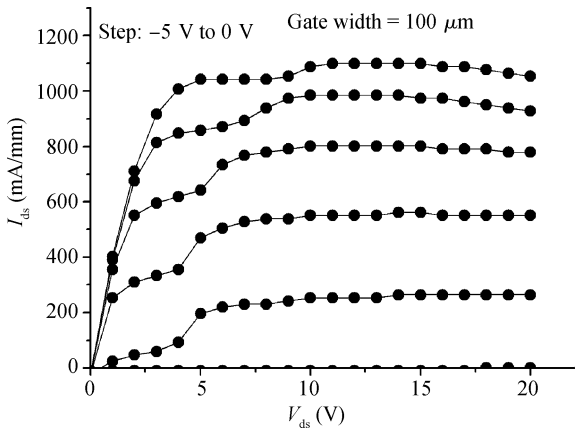

Fig. 1. DC drain current normalized to 1 mm for 100-μm-wide device.

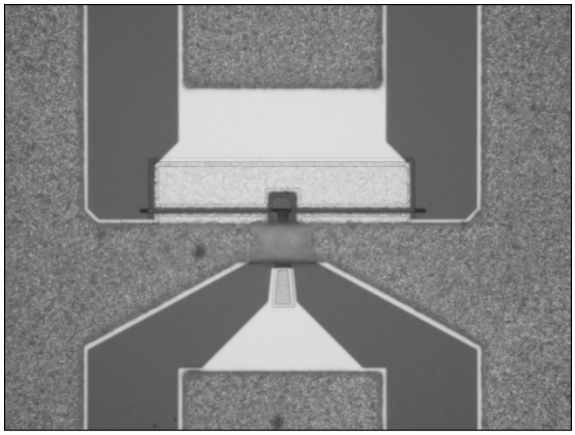

Fig. 2. Photograph of GaN HEMT with gate wide of 100-μm device.

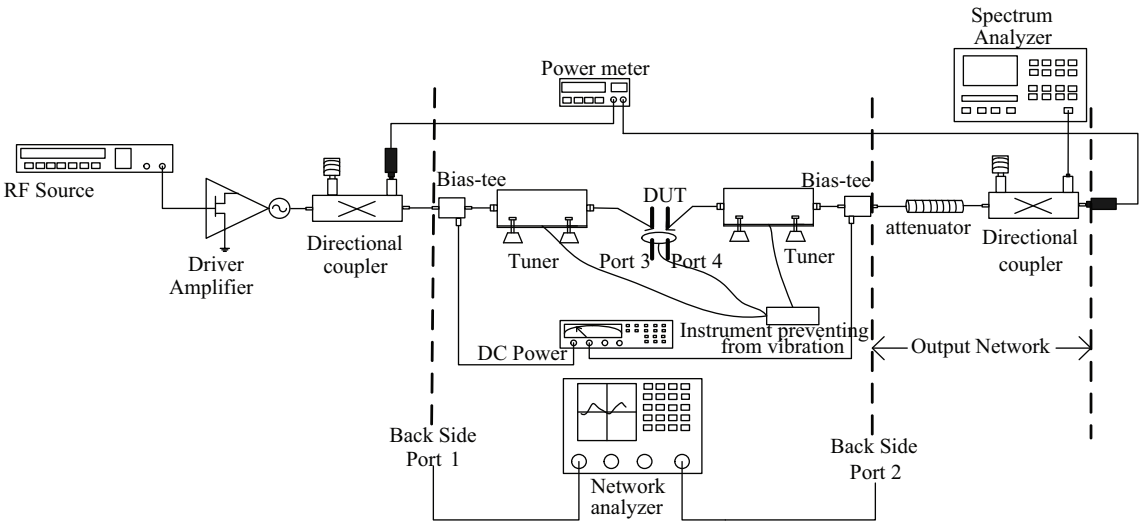

Fig. 3. Scheme of the automatic load/source-pull system.

The layered structure consists of a 100 nm-thick high temperature AlN nucleation layer, a 2 μm-thick GaN buffer layer and a 24 nm-thick un-doped AlGaN barrier layer with the Al component 30%. The measured Hall mobility, sheet electron density and sheet resistance are 1570 $cm^2/(V{\cdot}s)$, 1.29×10^{13} cm^{-2} and 308 $\Omega/\square$ at room temperature[7].

The devices were fabricated on the AlGaN/GaN epilayer described above. Mesa isolation was formed by Cl_2-based dry etching with an etching depth of about 150 nm. Ti/Al/Ni/Au (20 nm /120 nm / 55 nm / 45 nm) ohmic contact deposition is formed by using electron-beam evaporation and annealing at 850 ℃. A passivation film of Si_3N_4 was deposited by employing PECVD. The gate windows were opened by photolithography, followed by CF_4 plasma treatment in a reactive ion etching system. Finally, the Ni/Au Schottky gate was deposited by electron-beam evaporation[8].

The device on wafer measurements is a gate length of 0.5 μm with a gate width of 100 μm and 1 mm (100 μm × 10 fingers). Figure 1 shows that the I–V characteristics of the GaN HEMT with a gate length of 0.5 μm and a gate width of 100 μm are behaved over a drain bias V_{ds} of 0–20 V and a gate bias V_{gs} of –5 to 0 V. The data are obtained by DC characterization of the load-pull system. Figure 2 shows the layout of the 100 μm device. The pinch-off voltage of the transistor is –5 V. The I_{dss} of the GaN HEMT is approximately 1200 mA. However, the I_{ds} of the 1 mm-wide gate device is 520 mA biasing V_{gs} = –3 V, which is slightly lower than the I_{ds} for the 100 μm-wide gate device scaling behaviour (about 540 mA). That is due to the heating effect and degradation of thermal for the large periphery device in comparison to the small one.

3. Nonlinear measurement setups

The Maury real-time electromechanical load-pull system[9] that was developed by Xidian University, operating in the 1.8–18 GHz frequency range and handling an average power rating of 50 W, is shown in Fig. 3. The system consists of a CW signal source, a pre-amplifier, an isolator, two directional couplers at the input and output, a bias-tee at the input, a high power bias-tee at the output, the automatic tuner at the input and output, an attenuator, a dual-channel power meter, a spectrum analyzer and a vector network analyzer. The pre-amplifier is to boost input available power P_{in} (at port 3, as shown in Fig. 3.) high enough to drive the transistor in compression. Two high power bias-tees and directional couplers are taken up. The coupler at the input port couples to the power meter to moni-

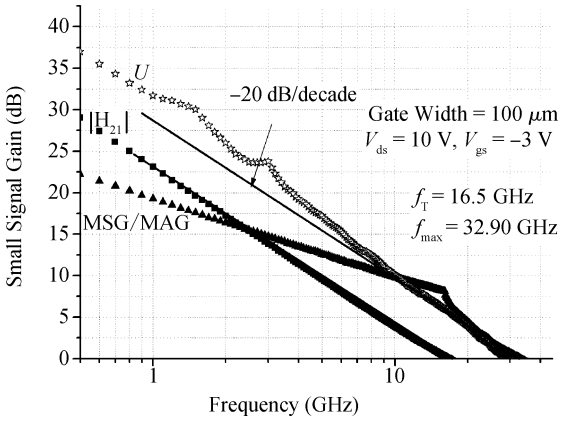

Fig. 4. Small signal performance for a gate width of 100 μm GaN HEMT on SiC substrate.

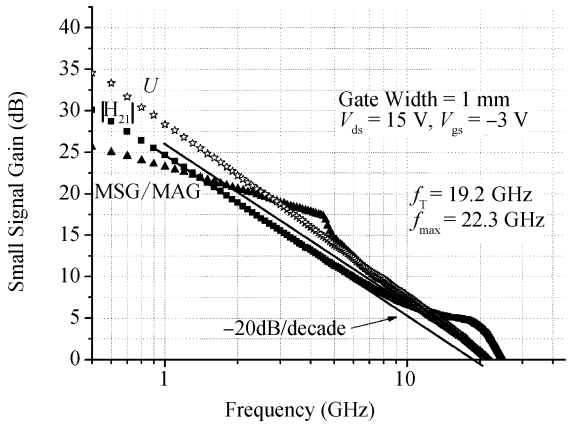

Fig. 5. Small signal performance for a gate width of 1 mm GaN HEMT on SiC substrate.

tor the input reflection power, while the one at the output port couples the output power to the spectrum analyzer to monitor transistor oscillation. The power generated at the output of the DUT is obtained by the output power meter by correcting the S parameter of the tuner and the S parameter of the output network. The DUT is connected to the tuner by the low-loss RF probe and cable. The Maury electromechanical tuners at the input and output are adjusted to provide the optimum source and load reflection coefficients. The purpose of the VNA calibration is to implement the correcting algorithms to compensate for systematical errors and set the non-linear characterization reference plane at the probe tips (from port 1 and port 2 to port 3 and port 4). The *in situ* calibration technology was used. In the calibration procedure, the ports' error terms were obtained and recorded by VNA with TRL and SOLT calibration methods. The S-parameters of the input tuner and output tuner for each tuner's position with other S parameters of the individual system blocks were measured. After that, the power calibration was followed with every part of the S parameters in order to measure the reflection coefficients, impedance, gain, PAE and output power at the DUT reference accurately[10].

4. Results and discussion

4.1. Small-signal characterization

The RF small signal performance was measured from 10 MHz to 40 GHz using an Agilent E8363B network analyzer. Before measuring, the system was calibrated with TRL cascade impedance standards and set the measuring reference plane at the DUT reference[11]. The extrinsic cutoff gain frequency f_T and the maximum frequency of oscillation f_{max} were determined as zero gain values of the current gain H_{21} and unilateral power gain, respectively. The small signal performance of the GaN HEMT with a gate width of 100 μm biasing at V_{ds} = 10 V, V_{gs} = –3 V was plotted in Fig. 4. The f_T of 16.53 GHz and f_{max} of 32.9 GHz were calculated with a slope of –20 dB/decade. With respect to the scaling effect, the f_T of 19.2 GHz and f_{max} of 22.3 GHz for the 1 mm-wide GaN HEMT on the same wafer was characterized, too. From the data in Figs. 4 and 5, the current gain f_T increases for large devices up to 1 mm. The parasitic effect of the pad capacitance decreases by enlarging the number of gate fingers[12]. For high power amplifier design, the maximum frequencies of oscillation of small devices and large periphery devices are enough for the 8 GHz[13].

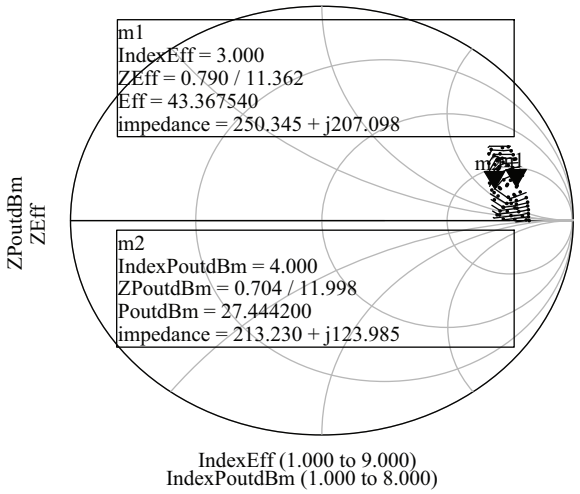

Fig. 6. Fundamental load pull measurement results of 100-μm-wide device at 5.5 GHz biased in class AB.

4.2. Load-pull and power sweep measurements

The load-pull measurement is based on the fundamental tuner load-pull characterization after selecting the fundamental source tuner. The *in situ* calibration method described above was performed to provide the constant and accurate reference planes before measurement. The output power and PAE versus the load reflection coefficient and load impedance are clearly demonstrated in the Smith chart, which is only valid in the calibration area, not whole Smith chart. Therefore, systems have to be elaborated minimizing losses to reach the maximum values of reflection coefficients.

Figure 6 shows the load-pull map of a 0.5 × 100 μm GaN HEMT on a SiC substrate at 5.5 GHz and in class AB operation. The figure illustrates the comprise between the maximum output power and the maximum PAE, and it shows the high magnitude of external load reflection coefficient $\Gamma_L = 0.79\angle 11.362$ and Z_L = 250.345 + j207.098 for the best PAE (43.36%), and $\Gamma_L = 0.704\angle 11.998$ and Z_L = 213.230 + j123.985 for the maximum output power (27.44 dBm). Because of the inherent losses

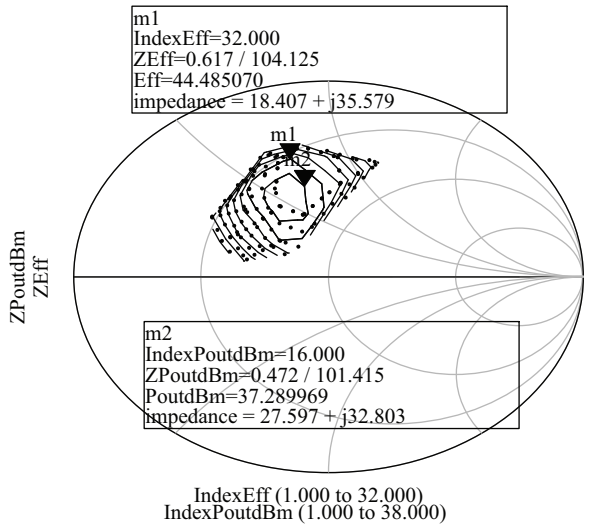

Fig. 7. Fundamental load pull measurement results of 1-mm-wide device at 5.5 GHz biased in class AB.

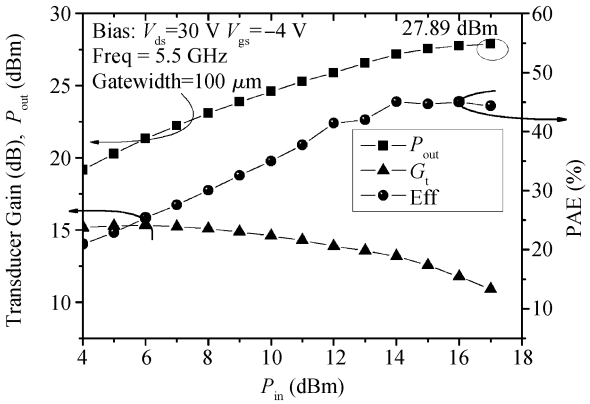

Fig. 8. P_{out}, gain and PAE measurements for a 100-μm-wide device when the load impedance is for maximum output power.

of the tuner and the probe, the characterization cannot cover enough area in the Smith chart, so the maximum PAE and output power should be a little less than the optimum values.

Figure 7 shows the load-pull map of a 10 × 0.5 × 100 μm GaN HEMT on a SiC substrate at 5.5 GHz and in class AB operation. A maximum power added efficiency of 44.48% can be reached when the fundamental load impedance and load reflection coefficient are 18.41 + j35.58 and 0.617∠104.125. When the fundamental load impedance and load reflection coefficient are 27.597 + j32.803 and 0.472∠101.415, the output power reaches the maximum power of 37.289 dBm, but the PAE is 44%. The dates illustrate that the impedance of the maximum output power is not the same as the optimum PAE. The load impedance of the large periphery device is comparatively high for the design of matching networks, which is characteristic of a GaN based device.

In Figs. 8 and 9, the results of the power measurement of a GaN HEMT on a SiC substrate with a gate width of 100 μm and a gate width of 1 mm are shown. The data are obtained when selecting the tuner position to achieve the maximum output power.

The output power, gain and PAE as a function of the input power are evaluated under the same conditions: frequency of 5.5 GHz, drain bias voltage of 30 V and gate bias voltage of –4 V. The bias condition was class AB operation. For the gate width of 100 μm, the linear gain was 15 dB. The output power at the 1 dB gain compression point was 25.3 dBm (3.38 W/mm). The maximum output power at 5 dB compression was capable of 27.89 dBm (6.15 W/mm). The PAE in this case was 45%. In the similar characterization, the results of a 1 mm device were demonstrated. The linear gain was 15.8 dB. The output power at the 1 dB gain compression point was 35.02 dBm (3.18 W/mm). The maximum output power at 7 dB compression was capable of 37.79 dBm (6.02 W/mm). The PAE in the case was 38.7%.

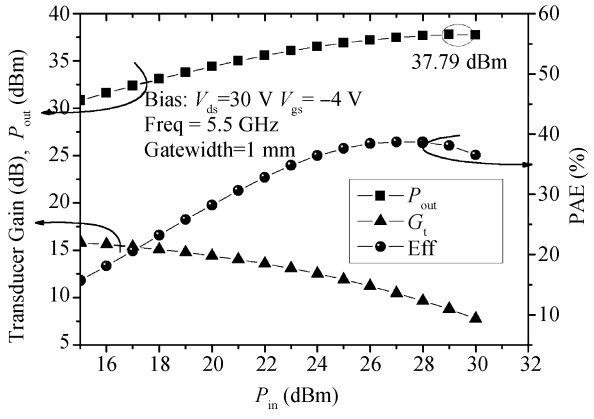

Fig. 9. P_{out}, gain and PAE measurements for a 1-mm-wide device when the load impedance is for maximum output power.

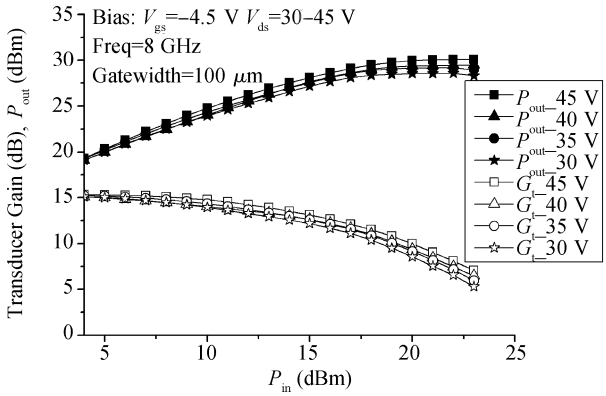

Fig. 10. Output power and gain behaviour of a 100-μm-wide GaN device at 8 GHz, operating in class AB and various drain bias conditions from 30 to 45 V.

The advantage of a GaN HEMT is the high breakdown voltage, which is critical for high power amplifier operation. For this reason, a simple experimental procedure was investigated, based on the typical behavior shown in Fig. 10. Figure 10 reports the output power and gain as a function of the input power, for a 0.5 × 100 μm device with four different drain voltages from 30 to 45 V. However, the device is biased at a gate voltage of –4.5 V at a frequency of 8 GHz, which decreases the self-heating effect of the DC current. The maximum output power increases from 28.3 dBm (6.76 W/mm) to 30.07 dBm (10.16 W/mm), and the output power at the 1 dB gain compression point increases from 25.27 to 26.25 dBm. The PAE

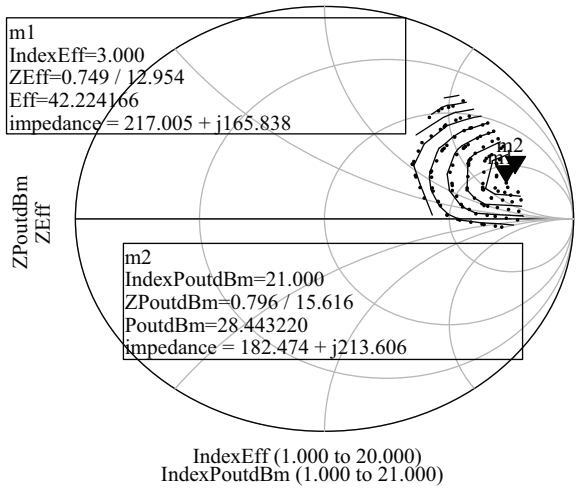

Fig. 11. Fundamental load pull measurement results of a 100-μm-wide device at 8 GHz biased in class AB.

was 40% when the maximum output power was reached. Correspondingly, the transducer gain increases from 15 to 15.3 dB. From the output power curves, the output power could be increased by adding the drain voltage. However, owing to the risk of probe damage in high voltage and high current, the measurement related to a higher drain voltage could not perform. In Fig. 11, when the maximum output power reaches 28.3 dBm (6.76 W/mm), the load reflection coefficient is 0.796∠15.62, which means that the edge of calibration in the Smith chart covers larger at 8 GHz than that at 5.5 GHz (0.704∠11.998). So the optimum load reflection coefficient can be measured. The data in Figs 10 and 11 demonstrate that the drain voltage biased in the GaN HEMT has a large swing. These performances guarantee that the GaN-based device can provide the higher power density and impedance, which make it much easier to match them to the system.

4.3. Self-heating effect on the scaling property of the large periphery device

When the gate widths of the transistor alter from 100 μm to 1 mm, the scaling rule should be considered. The ideal scaling rule[14] is

$$\mathrm{Sf} = \frac{U_{\mathrm{gw}}^{\mathrm{new}} N_{\mathrm{gf}}^{\mathrm{new}}}{U_{\mathrm{gw}}^{\mathrm{Orig}} N_{\mathrm{gf}}^{\mathrm{Orig}}}, \tag{1}$$

where Sf is the scaling factor. U_{gw} and N_{gf} represent the unit gate width and the number of gate fingers. However, the ideal scaling rule is seldom true, which is attributable to factors such as thermal environment, actual geometry and layout of the transistor die.

When the dimensions of the transistor increase, the thermal is the important factor. Heating in the active area of the large periphery transistor is the principal cause of device performance degradation. Self-heating effects at a high drain bias will increase the device lattice temperature and so does the carrier phonon scattering rate, which leads to reduced carrier mobility and carrier saturation velocity. The results have a great influence on the threshold voltage and will reduce the I_{dss} and peak transconductance. The decrease in peak transconductance with self-heating will result in a decrease in the circuit cut-off frequency. The decrease in I_{dss} will reduce the RF swing under large-signal operation, participating in the reduction of the RF output power. The increase in the number of fingers will also have an impact on the horizontal heat flow in the buffer layer[15] and the channel temperature of center fingers increases also.

However, as shown in Figs 4 and 5, the current gain f_{T} increases rather decreases with increasing size, which probably means that the parasitic effect of the pad capacitances exceeds the effect of self-heating.

By comparing the power sweep results in Figs 8 and 9, we can finally comment on the scaling properties of different gate width devices in large signal operation. From Eq. (1), the ratios of output power at 1 dB compression point to maximum output power at 10 dB. However, in our measurements, from the small device (gate width = 100 μm) to the large device (gate width = 1 mm), the output power at the 1 dB gain compression point changes from 25.3 to 35.02 dBm, corresponding to the gate width. The improvement is 9.72 dB. The maximum output power rises from 27.89 dBm in the 100 μm device to 37.8 dBm in the 1 mm device, with approximately 9.91 dB of improvement. The power improvements are slightly less than the ideal 10 dB increase. The scaling results are due to imperfect scaling of the DC current in the large periphery, which leads to thermal degradation and the reduction of the RF output power. The effect is related to the DC behaviour that was measured above. The drain current at a gate bias of –3 V changes from 54 mA (gate width of 100 μm) to 520 mA (gate width of 1 mm). The increase is 9.8 dB, which demonstrates the effect of self-heating[16].

5. Conclusion

The small signal performance and an extensive power characterization of GaN-based HEMT devices have been presented. The gate width of the 100 μm device and large periphery were studied. From the small signal data, the cutoff frequencies increase with the gate width, varying from 100 μm to 1 mm. The power characterization includes the load-pull and power sweep at frequencies of 5.5 GHz and 8 GHz. At 5.5 GHz, from the power sweep results, the maximum output power is 27.89 dBm (6.15 W/mm) with a gate width of 100 μm, and 37.8 dBm (6.02 W/mm) with a gate width of 1 mm when the load reflection coefficients are 0.704∠11.998 and 0.472∠101.415, respectively. A GaN HEMT on a SiC substrate has been measured by changing the drain voltage from 30 to 45 V with a biasing gate voltage in class AB operation. The results show that the GaN HEMT on a SiC substrate has a thermal conductivity, and it can exhibit maximum output power of 10.16 W/mm and a PAE of 40%. A high gate–drain breakdown voltage ensures the large swing in RF power. From the results, the improvement in output power verifies the scaling performance and thermal degradation for the large periphery device. The small signal performance and load-pull results demonstrate that the GaN HEMT is a promising candidate for high power amplifiers.

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