A 264 MHz CMOS G_m–C LPF for ultra-wideband standard*

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Abstract: A 264 MHz CMOS 4th G_m–C LPF target for the UWB standard is presented. The filter is designed by cascading two biquad cells. Compared with the previously published biquad cells, the biquad proposed here saves 1 transconductor, 3 CMFB networks and 2 capacitors. Benefiting from these merits, the power consumption and chip area of the 4th order UWB LPF are reduced dramatically without other characteristics being affected. The LPF is designed and fabricated with TSMC 0.18 μm 1P6M CMOS technology. The implemented LPF achieves a power gain of –0.5 dB. The measured frequency response matches well with that of the simulating results. The core chip area is only 0.06 mm^2, which has a wonderful advantage over those from similar work. The LPF excluding test-buffers dissipates a total current of 3 mA from the 1.8 V power supply.

Key words: low pass filter; CMOS; G_m–C; ultra-wideband
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1. Introduction

An ultra wideband (UWB) system has recently emerged and attracted great attention from both the market and researchers. In the frequency range from 3.1 to 10.6 GHz, the UWB system can be categorized into two approaches: single band (impulse radio) and multiple bands. For the multi-band approach, multi-band orthogonal frequency division multiplex (MB-OFDM) UWB, the spectrum is divided into several subbands of 528 MHz. Thus, MB-OFDM UWB can be implemented with a very high data rate of up to 480 Mb/s to meet the increasing demands of consumers for fast data transmission.

The low-pass filter (LPF) is a key building block in the transceiver system, mostly designed for channel selection and anti-alias. There are mainly three kinds of wideband filters: the switched-capacitor filter, the G_m–C filter and the active-RC filter. The switched-capacitor filter needs a higher sampling frequency than a pass band cutoff frequency.

An active RC filter needs a high speed operational amplifier. Compared with an active-RC filter, the G_m–C analog filter generates good frequency responses due to the absence of local feedback. The performance of the transconductor largely affects the capability of the G_m–C analog filters. Many of the previously published papers made efforts to improve the speed, linearity or dynamic range of the transconductor circuits[1−4]. In this study, a novel biquad LPF topology is proposed. Compared with the conventional biquad cells[5−7], this methodology saves 1 transconductor, 3 CMFB networks and 2 capacitors. Benefiting from these merits, the power consumption and chip area of the 4th order LPF are reduced dramatically.

2. Circuit design

2.1. Biquad LPF structure

A simplified diagram of the biquad[8] is shown in Fig. 1.

The transfer function of the LPF can be expressed as:

$$\frac{V_{LP}}{V_{IN}} = \frac{G_{m1}G_{m3}}{C_1C_2} \times \left[S^2 + \left(\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + \frac{G_{m2}}{C_2}\right)S + \frac{1 + G_{m2}R_2 + G_{m3}G_{m4}R_1R_2}{R_1R_2C_1C_2}\right]^{-1}, \quad (1)$$

where G_m is the transconductance of the G_m cells. The resistor R_1 stands for the output resistance of the G_{m2} cell and R_2 represents the output resistance of the G_{m4} cell in parallel with the output resistance of the G_{m2} and G_{m1} cells. The cutoff frequency (ω_0) and the quality factor of the LPF are revealed as follows,

$$\omega_0^2 = \frac{1 + G_{m2}R_2 + G_{m3}G_{m4}R_1R_2}{R_1R_2C_1C_2} \approx \frac{G_{m3}G_{m4}}{C_1C_2},$$
$$Q \approx \frac{\omega_0}{\dfrac{1}{R_1C_1} + \dfrac{1}{R_2C_2} + \dfrac{G_{m2}}{C_2}}. \quad (2)$$

The resistance seen from the BP node is equal to the output resistance of G_{m1}, G_{m2} and G_{m4} in parallel with $1/G_{m2}$. The

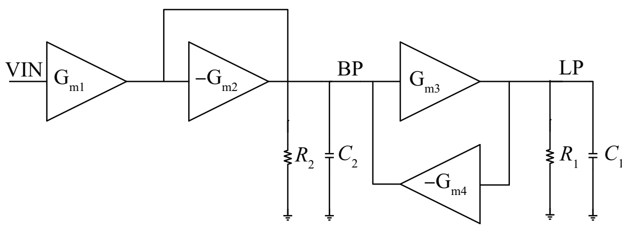

Fig. 1. Architecture of biquad LPF.

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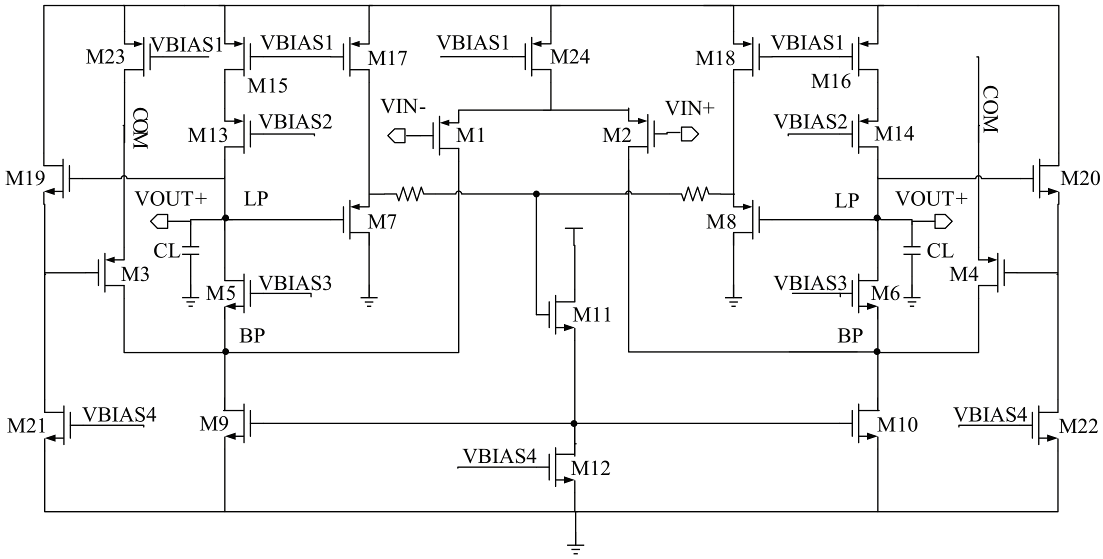

Fig. 2. Schematic of the proposed biquad LPF

output resistances, R_1 and R_2 , are larger than the small resistor of $1/G_{\rm m2}$. In such a case, the small resistor of $1/G_{\rm m2}$ plays the dominant role in the quality factor, as demonstrated in Eq. (2). In the 264 MHz UWB low pass filters, a very high quality factor is not required. Therefore, conventional techniques employed to enhance R_1 and R_2 not only increase the quality factor negligibly but also have the negative consequence of decreasing the cutoff frequency owing to the parasitic pole introduced by the internal node. From the architecture of Fig. 1, there are at least two poles. The first pole is located at a low frequency and is equal to $1/R_1C_1$, while the second one is equal to $G_{\rm m2}/C_2$ and is located at a very high frequency. The second pole restricts the maximum achievable bandwidth of a process. As mentioned before, to reach a higher cutoff frequency, the $\rm G_m$ -cell must have a very simple design without any poles.

2.2. Biquad LPF realization

Figure 2 shows the proposed Biquad LPF core. $G_{\rm m1}$ and $G_{\rm m4}$ are realized by the input differential pair (M1–M2) and feedback differential pair (M3–M4), respectively. The negative sign of $G_{\rm m4}$ in Fig. 1 is implemented by utilizing negative feedback. Assuming that the voltage of VIN+ decreases, the current of M2 increases and injects into the BP node, which enhances the voltage of VOUT+ node. Subsequently, the gate voltage of M4 increases and the current of M4 decreases (drains current from BP node). This process is analogous to the functions of the $G_{\rm m1}$ and – $G_{\rm m4}$ cells in Fig. 1, where $G_{\rm m1}$ injects current into the BP node and – $G_{\rm m4}$ drains current from it. The art of the technique lies in how $G_{\rm m2}$ and $G_{\rm m3}$ are addressed. As can be seen from Fig. 1, $G_{\rm m2}$ provides the low resistance of $1/G_{\rm m2}$ for the BP node to push the second pole of the loop to higher frequencies. Meanwhile, the input resistance of $G_{\rm m4}$ is infinite and its output current is equal to $G_{\rm m4}V_{\rm BP}$. In the circuit of Fig. 2, M5–M6 play the role of both $G_{\rm m2}$ and $G_{\rm m3}$. The transistors M5 and M6 are in common-gate configuration and provide the low resistance of $1/g_{\rm m56}$ for the BP nodes, analogous to $G_{\rm m2}$ in Fig. 1. Also, M5 and M6 drain the current of $G_{\rm m56}V_{\rm BP}$ from the BP nodes and buffer it to the output nodes. Therefore, by adopting this topology, the KCL relation and equivalent resistance do not change in the BP node meantime one transconductor is economized. The transfer function of the LPF is given by

$$\begin{aligned}\frac{V_{\rm OUT}}{V_{\rm IN}} =& \frac{g_{\rm m2}}{C_{\rm L}}\frac{g_{\rm m20}}{C_{\rm gs4}+C_{\rm gs20}} \\ &\times\left[S^2+\left(\frac{1}{R_1C_{\rm L}}+\frac{g_{\rm m20}}{C_{\rm gs4}+C_{gs20}}\right)S\right.\\ &\left.+\frac{1+g_{\rm m4}R_1}{R_1(g_{\rm m20})^{-1}C_{\rm L}(C_{\rm gs4}+C_{\rm gs20})}\right]^{-1},\\ R_1 \approx& [(g_{\rm m6}r_{\rm 06})(r_{\rm 02}\parallel r_{\rm 04}\parallel r_{\rm 06}\parallel r_{\rm 010})]\parallel(g_{\rm m14}r_{\rm 014}r_{\rm 016}),\\ R_2 \approx& \frac{1}{g_{\rm m6}}\parallel(r_{\rm 02}\parallel r_{\rm 04}\parallel r_{\rm 06}\parallel r_{\rm 010})\approx\frac{1}{g_{\rm m6}},\end{aligned} \tag{3}$$

The cutoff frequency and quality factor are equal to

$$\omega_0^2 \approx \frac{g_{\rm m4}g_{\rm m20}}{C_{\rm L}(C_{\rm gs4}+C_{\rm gs20})}, \tag{4}$$

$$Q \approx \frac{\omega_0}{\dfrac{g_{\rm m20}}{(C_{\rm gs4}+C_{\rm gs20})}}. \tag{5}$$

The DC gain of the biquad is given by

$$A_{\rm dc} \approx \frac{g_{\rm m2}}{g_{\rm m4}}. \tag{6}$$

2.3. Common-mode feedback

The common-mode feedback (CMFB) network consists of M7, M17, M9, M19, $R_{\rm CM1}$, $R_{\rm CM2}$, M11, M12, M9, M10,M5,M6,M7, and M17. M8, M18 are source followers between the output node and its corresponding CM voltage extracting resistor. The CM voltage detected by $R_{\rm CM1}$ and $R_{\rm CM2}$ is shifted by $V_{\rm GS78}$ compared with the output node CM level[9].

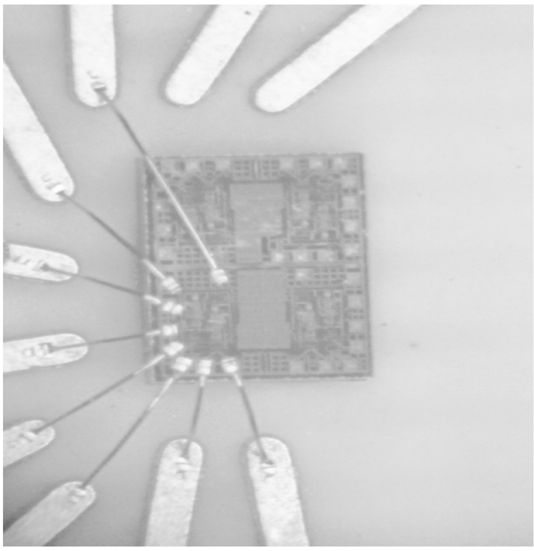

Fig. 3. Microphotograph of the LPF.

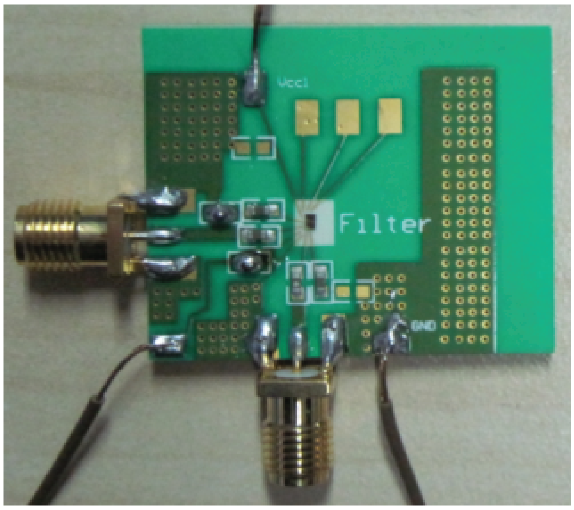

Fig. 4. Die on PCB test.

Following this voltage is transferred by V_{GS11} due to M11–M12 source follower, and then the currents of M9 and M10 are adjusted to match the current mirrors of M15 and M16. The output node CM voltage is given by

$$\begin{aligned}V_{\text{OUT\_CM}} &= |V_{GS9}| + |V_{GS11}| - |V_{GS7}| \\ &= \sqrt{\frac{2I_9}{\mu_n C_{ox}\frac{W}{L}}} + |V_{th9}| + \sqrt{\frac{2I_{11}}{\mu_n C_{ox}\frac{W}{L}}} + |V_{th11}| \\ &\quad - \sqrt{\frac{2I_7}{\mu_p C_{ox}\frac{W}{L}}} - |V_{th7}| \\ &= \sqrt{\frac{2\left(I_{15} - \frac{I_{23}}{2} - \frac{I_{24}}{2}\right)}{\mu_n C_{ox}\frac{W}{L}}} + |V_{th9}| + \sqrt{\frac{2I_{11}}{\mu_n C_{ox}\frac{W}{L}}} \\ &\quad + |V_{th11}| - \sqrt{\frac{2I_7}{\mu_p C_{ox}\frac{W}{L}}} - |V_{th7}|. \end{aligned} \tag{7}$$

The stability of the common-mode loop can be ensured by the condition that the non-dominant pole of the loop is located at a higher frequency than the 3 GBW of the loop. This condition can be expressed as

$$\omega_{\text{non-dom}} \geqslant 3\text{GBW}_{\text{CM}}. \tag{8}$$

For the common mode loop,

$$\begin{aligned}\text{GBW}_{\text{CM}} &= A_{\text{CM}}\omega_{\text{dom}} = \frac{g_{m9}}{C_L}, \\ \omega_{\text{non-dom}} &= \frac{g_{m11}}{C_{gs9} + C_{gs11}}, \\ \omega_{\text{dom}} &= \frac{1}{R_1 C_L}. \end{aligned} \tag{9}$$

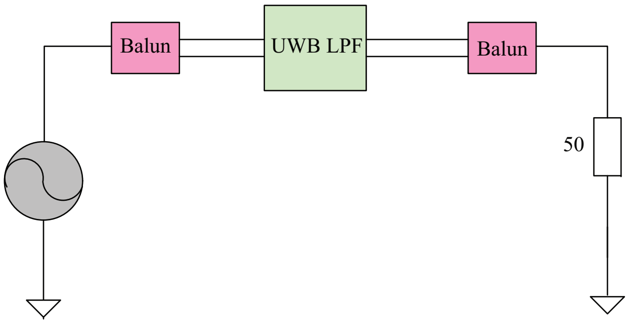

Fig. 5. Test mode.

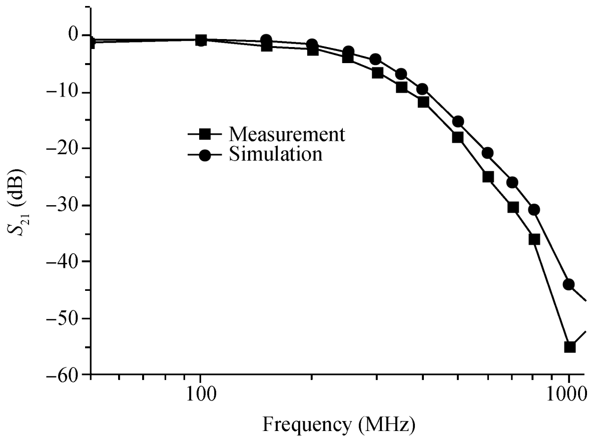

Fig. 6. Measured and simulated S_{21}.

3. Measurement results and analysis

The LPF in this work is designed in TSMC 0.18 μm 1P6M RF CMOS technology. Two stages of biquads are cascaded to obtain a fourth-order LPF. The chip photograph of the circuit, with a core chip area of 0.2×0.3 mm^2, is shown in Fig. 3. The LPF die is tested on a PCB, as shown in Fig. 4. As the LPF has differential input and differential output, a couple of baluns are employed to convert the single end signal to differential signals, and vice versa (Fig. 5). The Agilent E8363B is used to

Table 1. Performance comparison with published UWB LPFs.

Parameter	Technology	Cutoff freq (MHz)	Gain (dB)	Chip area (mm^2)	Current (mA)
This work	0.18 μm CMOS	264	–0.5	0.06	3
Ref. [10]	65 nm CMOS	240	9–43	0.21	30
Ref. [11]	0.25 μm CMOS	200	0	—	70
Ref. [12]	0.35 μm CMOS	200	0	0.18	20
Ref. [13]	0.15 μm CMOS	264	0	0.28	9.7

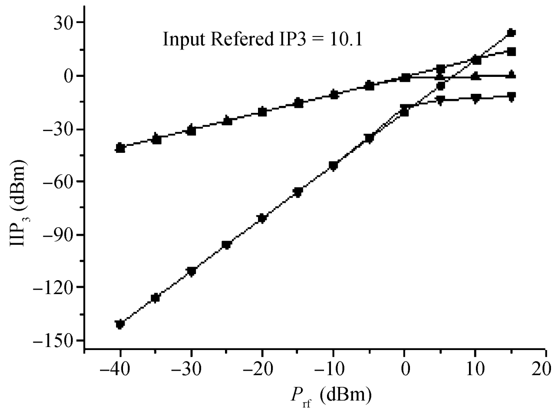

Fig. 7. Measured IIP3.

measure the S_{21} parameter. The simulated and measured S_{21} parameters are compared in Fig. 6. The measured S_{21} agrees quite well with that of the simulation. With two tones of frequencies of 100 and 101 MHz and equal amplitudes applied, the measured input-referred third-order intercept point (IIP3) is equal to 10.1 dBm, as shown in Fig. 7. The total current in this circuit is 3 mA under a 1.8 V supply voltage.

4. Conclusion

This paper describes the design of a 264 MHz CMOS 4th G_m–C LPF fabricated by TSMC 0.18 μm 1P6M CMOS technology. A novel biquad is proposed, which saves 1 transconductor, 3 CMFB networks and 2 capacitors. Benefiting from these merits, the power consumption and chip area of the 4th order UWB LPF are reduced dramatically without other characteristics being negatively affected. The measured results validate the feasibility of these techniques.

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