A 0.18 μm CMOS inductorless complementary-noise-canceling-LNA for TV tuner applications*

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Abstract: This paper presents an inductorless complementary-noise-canceling LNA (CNCLNA) for TV tuners. The CNCLNA exploits single-to-differential topology, which consists of a common gate stage and a common source stage. The complementary topology can save power and improve the noise figure. Linearity is also enhanced by employing a multiple gated transistors technique. The chip is implemented in SMIC 0.18 μm CMOS technology. Measurement shows that the proposed CNCLNA achieves 13.5–16 dB voltage gain from 50 to 860 MHz, the noise figure is below 4.5 dB and has a minimum value of 2.9 dB, and the best P_{1dB} is –7.5 dBm at 860 MHz. The core consumes 6 mA current with a supply voltage of 1.8 V, while the core area is only 0.2 × 0.2 mm^2.

Key words: noise cancellation; LNA; low-power; multiple gated transistors; complementary
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1. Introduction

The fast growing market of wireless communications has driven much effort toward the development of high-performance low-cost, low-noise and low-power CMOS RF blocks. LNA is one of the most important RF blocks. In general, the first stage of a receiver RF front-end is an LNA. According to the Friis equation, it is clear that the system noise figure is dominated by the LNA noise performance, so noise optimization is one of the most critical steps in LNA design. Traditional LNA design involves tradeoffs between impedance matching and the noise figure (NF). Many possible solutions for getting good noise performance have been presented and noise cancellation is a good candidate for wideband LNAs, which are used in UWBs, TV tuners, etc[1−6]. In Ref. [1], the concept of noise canceling is shown. It consists of an amplifier stage that provides source impedance, an auxiliary amplifier sensing the voltage across the real input source and a circuit combining the output of the two stages. But the auxiliary amplifier consumes more power to reduce the impact of the NF.

Linearity is one of the most critical features of LNA and impacts the dynamic range of the whole receiver chain. An LNA with good linearity can significantly minimize the RF circuit issues, such as harmonics, intermodulation, blocking and cross modulation[7]. For this reason, the LNA must have good linearity, i.e. high second and third order distortion intercept points (IIP2 and IIP3). The even-order nonlinearity can easily be reduced by designing a differential topology. However, it is difficult to reduce the odd-order distortion. There are several methods presented in the literature to improve the LNA linearity. Source degeneration is an effective method. But there is a trade-off between the linearity and the gain of LNA. Negative feedback is another useful method. The feedback can degrade the noise performance and also increase the power consumption. The multiple gated transistor (MGTR) topology is another effective way to linearize the circuit[8, 9]. The method is to use additional transistor's non-linearly to cancel the non-linearity of the main operation device. The additional transistor works in weak inversion, so there is no more power consumption. The LNA proposed in this paper uses the MGTR approach. In this paper an inductorless complementary-noise-canceling LNA (CNCLNA) used in DVB-C is proposed. The complementary topology can save power; we will show that it also improves the noise performance.

2. Basic noise canceling LNA design

Figure 1 shows the basic-noise-canceling LNA (BNCLNA) presented in Ref. [2]. It consists of a common gate (CG) stage and a common source (CS) stage. In general, the

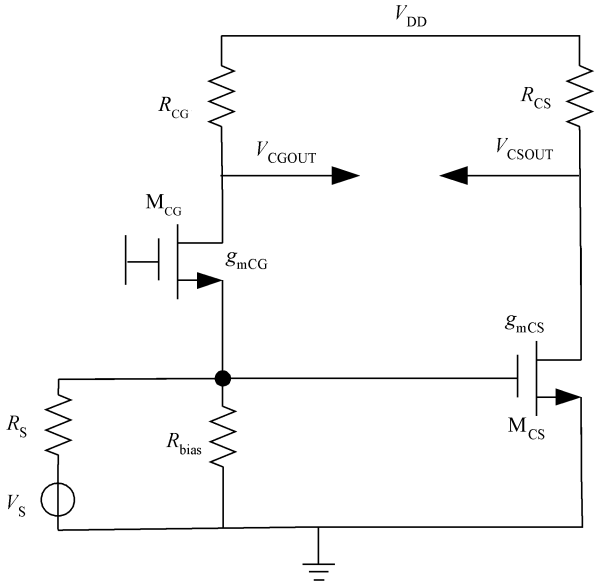

Fig. 1. Basic common-gate-common-source topology with noise cancellation.

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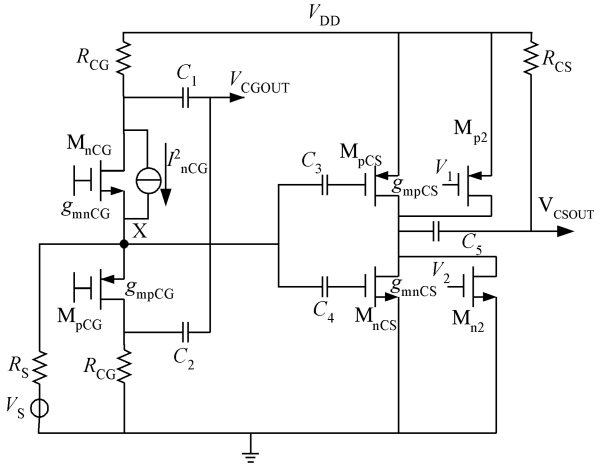

Fig. 2. Schematic of the proposed LNA (bias not shown).

CG-stage gives an input match. The real part of the input impedance is set by $1/g_{mCG}$ of the CG transistor in parallel with resistor R_{bias}. If $1/g_{mCG} \ll R_{bias}$, then $R_S = 1/g_{mCG}$, and the noise of M_{CG} dominants the NF. The NF is equal to $1+\gamma g_{d0}/g_m$, where γ is a fitting parameter and g_{d0} is the channel conductance for $V_{DS} = 0$. For a short channel MOSFET, the NF is greater than 3 dB. However, the signal voltages at the differential output shown in Fig. 1 have opposite sign and the noise voltages from the matching device M_{CG} have the same sign, so the noise from the CG-transistor can be cancelled at the differential output. In Ref. [2], the noise factor derived does not include the noise from the bias resistor, the noise factor $F_{R_{bias}}$ is

$$F_{R_{bias}} = R_S I^2_{nbias}/4, \tag{1}$$

where R_S is source impedance and I^2_{nbias} is the noise current of the bias resistor ($= 4kT/R_{bias}$). Then the more complete noise factor is

$$F = F_{CG} + F_{CS} + F_R + F_{R_{bias}}. \tag{2}$$

The second part in Eq. (2) is the noise contribution from the CG-transistor. If the gains of the CG and CS stages are designed to be equal, then F_{CG} = 0. The third part is from the CS-transistor, and the fourth part is from the load resistors. For getting a good noise performance, the value of the bias resistor is chosen as several hundred Ohm, typically. For example, with R_{bias} of 500 Ω, simulation results show that the noise contribution is about 25%. So the bias resistor is an important noise source in the circuit.

3. Proposed noise canceling LNA

The proposed CNCLNA is depicted in Fig. 2. In our design, a complementary current reuse topology is used. An nMOS CG amplifier M_{nCG} is stacked on top of a pMOS CG amplifier M_{pCG} to reuse the DC current. The advantage of this topology is that the two amplifiers do not require bias circuitry to define the source voltage. The bulk of the transistors are tied to their source in order to reduce the threshold voltage, hence the voltage headroom is increased. The CS stage is also a complementary topology. The transistors M_{n2} and M_{p2} operate in the sub-threshold region to improve the linearity. C_1–C_5 are AC coupling capacitances. R_S is the source impedance. R_{CG} and R_{CS} are load resistors. The bias circuit and output buffer for measurement are not shown.

3.1. Noise analysis

First, assuming that $g_{mnCG} = g_{mpCG} = g_{mCG}$, then for impedance matching, the input impedance of the circuit in Fig. 2 is

$$R_{in} = \frac{1}{g_{mnCG}} // \frac{1}{g_{mpCG}} = \frac{1}{2g_{mCG}} = R_S, \tag{3}$$

R_S is the source impedance, and the gain of the CG stage is

$$A_{VCG} = (g_{mpCG}V_{in} + g_{mnCG}V_{in})\frac{R_{CG}}{2}/V_{in} = g_{mCG}R_{CG}. \tag{4}$$

The CS stage gain is

$$A_{VCS} = (g_{mpCS} + g_{mnCS})R_{CS}. \tag{5}$$

For getting the balun operation, $A_{VCG} = -A_{VCS}$, and

$$g_{mCG}R_{CG} = -(g_{mpCS} + g_{mnCS})R_{CS}, \tag{6}$$

the noise current I^2_{nCG} ($= 4kT\gamma g_m$) due to M_{nCG} generates a noise voltage at node X, and this voltage is

$$V_{XnCG} = I_{nCG}\frac{1}{g_{mnCG}} // R_S // \frac{1}{g_{mpCG}} = \frac{R_S}{1+2g_{mCG}R_S} I_{nCG}. \tag{7}$$

The noise voltages at the outputs of CG and CS stages respectively are

$$V_{nCG} = \frac{I_{nCG}}{1+2g_{mCG}R_S}\frac{R_{CG}}{2}, \tag{8}$$

$$V_{nCS} = -(g_{mpCS} + g_{mnCS})R_{CS}\frac{R_S}{1+g_{mCG}R_S} I_{nCG}. \tag{9}$$

The output noise voltage provided by M_{nCG} is $V_{nCG} - V_{nCS}$. The noise voltage from M_{pCG} is equal to that from M_{nCG}. So the noise factor from the CG stage is

$$NF_{CG} = \frac{2\gamma g_{mCG}[R_{CG}/2 - (g_{mpCS} + g_{mnCS})R_{CS}R_S]^2}{A_V^2 R_S}. \tag{10}$$

If Equation (6) is satisfied, the noise from the CG-transistors can be cancelled. After canceling the noise from the CG-transistors, the noise figure is dominated by the CS-transistors, R_{CS} and R_{CG}. The following expressions describe how these noise sources determine the noise performance.

$$NF_{CS} = \frac{\gamma(g_{mnCS} + g_{mpCS})R^2_{CS}(1+2g_{mCG}R_S)^2}{R_S A_v^2}, \tag{11}$$

$$NF_R = NF_{R_{CG}} + NF_{R_{CS}} = \frac{(R_{CG}/2 + R_{CS})(1+g_{mCG}R_S)^2}{R_S A_v^2}. \tag{12}$$

Then the total noise factor can be approximated as

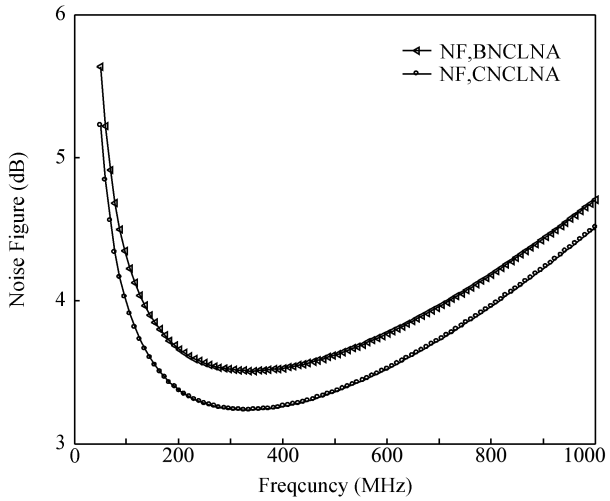

Fig. 3. NF comparison between BNCLNA and CNCLNA.

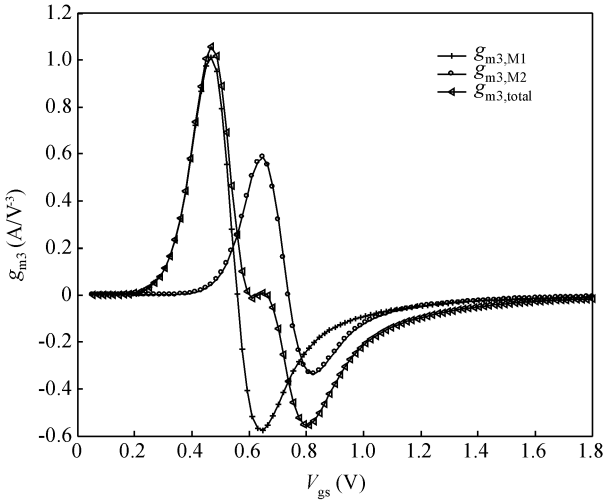

Fig. 5. Illustration of g_{m3} cancellation technique.

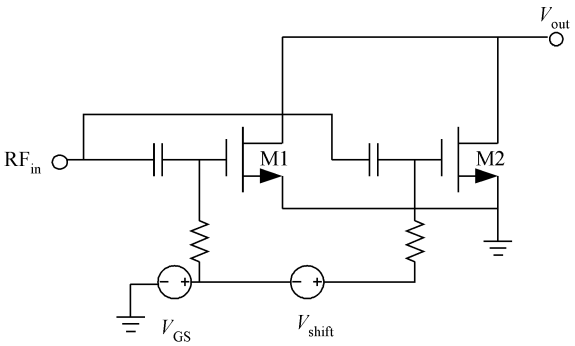

Fig. 4. Linearity improved by using MGTR.

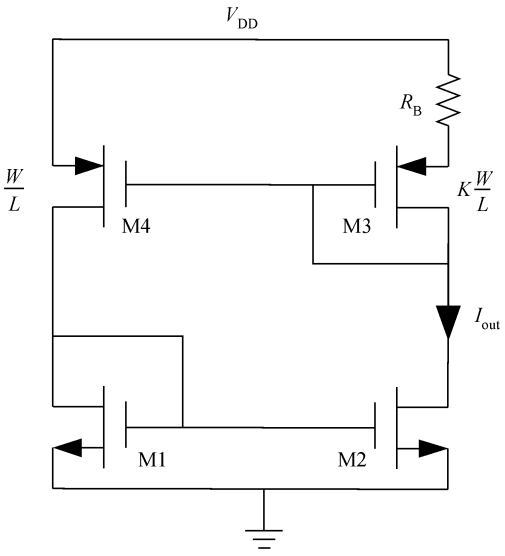

Fig. 6. Constant-g_m bias circuit.

$$\mathrm{NF} = 1 + \mathrm{NF_{CS}} + \mathrm{NF_R}. \tag{13}$$

In contrast to BNCLNA, the noise from the bias resistor is eliminated in CNCLNA. Figure 3 depicts the SpectreRF simulation comparison of the NF between BNCLNA and CNCLNA with the same differential gain; the noise figure is improved by 0.3 dB.

3.2. Linearity analysis

As derived in Ref. [1], not only the noise of the CG-transistor is cancelled but also its nonlinearity. Then only the CS-transistor nonlinearity needs to be improved.

The drain current of a common source MOSFET can be expressed by the Taylor series as

$$i_{\mathrm{DS}} = I_{\mathrm{dc}} + g_{\mathrm{m}} v_{\mathrm{gs}} + \frac{g_{\mathrm{m2}}}{2!} v_{\mathrm{gs}}^2 + \frac{g_{\mathrm{m3}}}{3!} v_{\mathrm{gs}}^3 + \cdots, \tag{14}$$

where v_{gs} is the small signal gate-to-source voltage and g_{mn} is the n th order transconductance. We know that the third order transconductance g_{m3} plays a very important role in the linearity of the MOSFET. The MGTR topology shown in Fig. 4 can minimize the g_{m3} by superposing several transistors with proper bias in parallel[9]. The g_{m3} is illustrated in Fig. 5. We can see that the g_{m3} has a negative peak value in the voltage range of 0.55 to 0.9, which is the normal operating gate voltage to achieve a better power efficiency, i.e. $g_{\mathrm{m}}/I_{\mathrm{D}}$. Then the negative value can be cancelled by the positive value of the transistor M2, whose DC bias is shifted by changing the overdrive voltage. Because M2 operates in the subthreshold region, this method effectively improves IIP3 without any extra power consumption. The transistors Mn2 and Mp2 shown in Fig. 3 are used for compensation of the main transistors' IM3, leading to higher linearity.

3.3. Bias discussion

As derived above, if the gains of the two stages are equal in magnitude, the noise from the CG-transistors can be cancelled. So the gain imbalance determines the noise performance.

For this reason, it is desirable to bias the circuit such that the gain balance does not depend on the temperature, process and supply voltage (PVT)[10].

In this design, the constant-g_{m} bias shown in Fig. 6 is used to minimize the gain difference. Discussed in Ref. [10], the bias

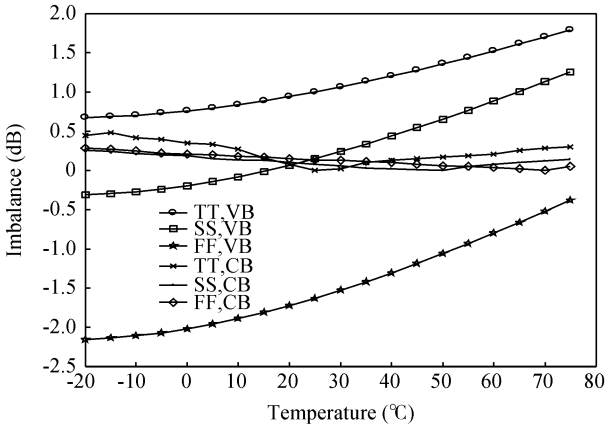

Fig. 7. Imbalance over process and temperature.

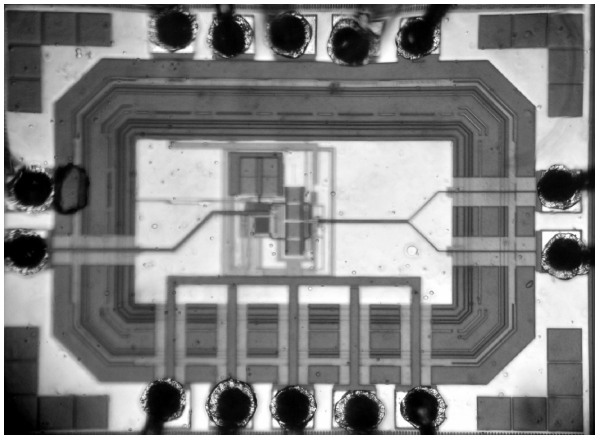

Fig. 8. Chip micrograph of the LNA (0.2×0.2 mm^2).

current I_{out} is

$$I_{\text{out}} = \frac{2}{\mu_{\text{p}} C_{\text{ox}} (W/L)_{\text{p}}} \frac{1}{R_{\text{B}}^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2, \qquad (15)$$

where μ_{p} and C_{ox} are process parameters and K is a constant. According to Eq. (15), the bias current is still a function of process and temperature. But the g_{m} equals

$$g_{\text{m}} = \frac{2}{R_{\text{B}}} \left(1 - \frac{1}{\sqrt{K}}\right), \qquad (16)$$

a value independent of the MOS device parameter. Then the gains of the two stages can be expressed as

$$A_{\text{VCG}} = 2 g_{\text{mCG}} R_{\text{CG}} = 2 \frac{2R_{\text{CG}}}{R_{\text{BCG}}} \left(1 - \frac{1}{\sqrt{K_{\text{CG}}}}\right), \qquad (17)$$

$$A_{\text{VCS}} = g_{\text{mCS}} R_{\text{CS}} = \frac{2R_{\text{CS}}}{R_{\text{BCS}}} \left(1 - \frac{1}{\sqrt{K_{\text{CS}}}}\right). \qquad (18)$$

After the value of R_{B} and K are properly chosen, the gain imbalance can be minimized. As shown in Fig. 7, the constant-g_{m} bias circuit (CB) can provide a good balance over temperature and process, while the voltage bias (VB) cannot.

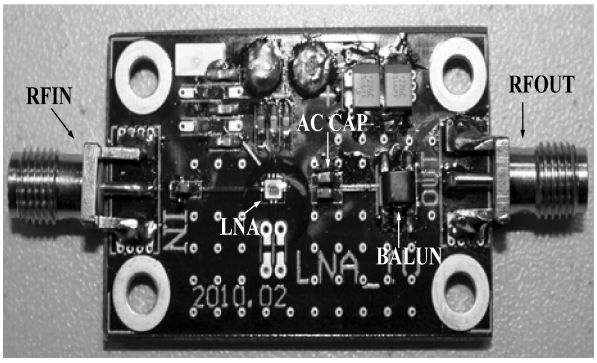

Fig. 9. Test board of the LNA.

4. Measured results

The proposed LNA was fabricated in SMIC 0.18 μm RF CMOS technology. A source follower is added for measurement. Figure 8 depicts the chip micrograph. The chip core area is 0.2×0.2 mm^2, excluding ESD-pads.

The LNA is mounted on an FR-4 PCB test board (COB), shown in Fig. 9. It is measured using a 50 Ω single-ended input port and a balun that converts the differential output to single-ended. Figure 10 shows the measured S-parameter by an Agilent 8722ES vector network analyzer versus that from the simulation results. The measured S_{11} and S_{22} are below –8 dB and –7.5 dB across 50–860 MHz, respectively. The reverse isolation S_{12} is below –40 dB up to 1 GHz. To convert S_{21} to voltage gain, 6 dB needs to be added. Then the voltage gain shown in Fig. 10(c) is 13.5–16 dB. All the measurement results agree well with the simulation results at low frequency. As the frequency increases, the departure from simulations is due to inaccuracy in the high-frequency modeling and parasitic capacitances which degrade the performance.

The NF is measured by an Agilent 8974A NF analyzer. Figure 11 shows both the simulated and the measured NF. The measured NF has a minimum value of 2.9 dB. The difference between the two curves at low frequency is because of the inaccuracy of the flicker noise modeling. At high frequency, the drops in gain and PCB parasitic resistors increase the NF.

Figure 12 gives the measured $P_{1\text{dB}}$ with the value of –10 to –7.5 dBm. The linearity is not very good. First, the linearity is inversely proportional to the overdrive voltage, the common gate stage does not have enough voltage headroom, although the MGTR is exploited. Second, there is trade-off between the NF and the linearity. According to Figs. 11 and 12, it is clear that the trade-off does exist. So, increasing the supply voltage or reducing the gain can improve the linearity.

5. Conclusion

In this paper, the complementary-noise-canceling LNA for a TV tuner is designed and measured. The complementary topology that can simultaneously achieve better noise performance and lower power is confirmed by the theoretical analysis and the measurement results. The linearity and bias condition of the LNA is also analyzed. The proposed LNA is fabricated in SMIC 0.18 μm CMOS technology. Measurement results show that the power consumption is 10.8 mW, and the NF is below

Table 1. Summary and performance comparison.

Parameter	Ref. [1]	Ref. [3]	Ref. [11]	Ref. [12]	Ref. [13]	This work
Technology (μm)	0.18 CMOS	0.065 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS
Freq. band (GHz)	0.2–2	0.2–5.2	0.47–0.87	0.47–0.76	0.05–0.86	0.05–0.86
NF (dB)	< 2.4	< 3.5	4.3	4.5	4.2	< 4.5
Voltage gain (dB)	10–14	13–15.6	16	25	15	13.5–16
P_{1dB} (dBm)*	–9.6	> –9	–10.9	–13.6	–7	> –10
P_{dc} (mW)	35	21	22	16	10	10.8
S_{11} (dB)	< –8	< –10	< –11	N/A	< –10	< –8
Area (mm^2)**	0.075	0.009	0.32	0.52	0.29	0.04

*P_{1dB} = IIP3 – 9.6 dBm, ** not including PAD.

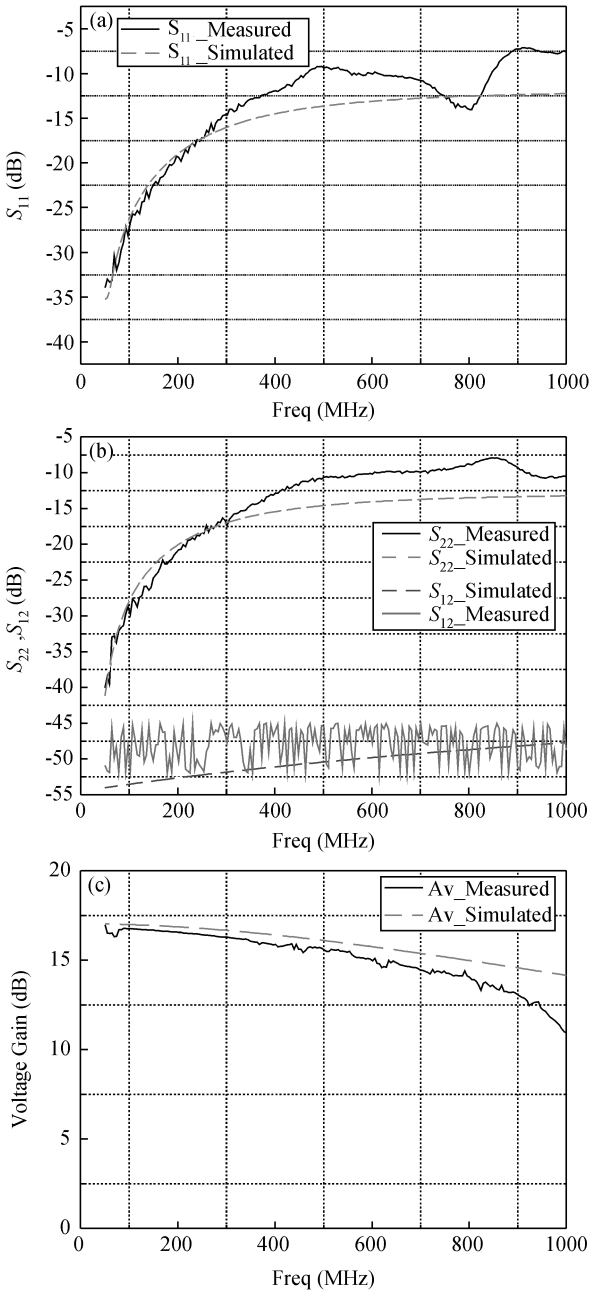

Fig. 10. Measured and simulated S-parameter. (a) S_{11}. (b) S_{22} and S_{12}. (c) Voltage gain.

4.5 dB. This topology is suitable for realizing low power wide-band LNA designs in CMOS technology. Table 1 summarizes

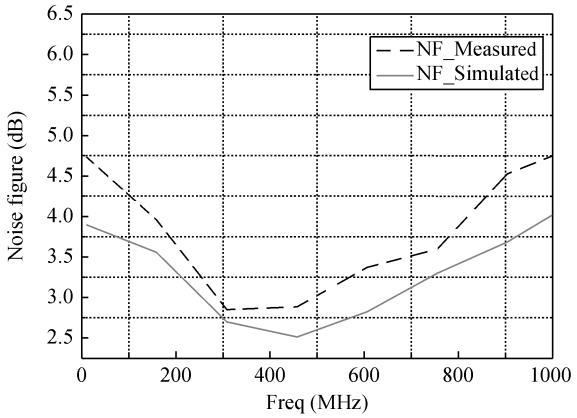

Fig. 11. Measured and simulated NF.

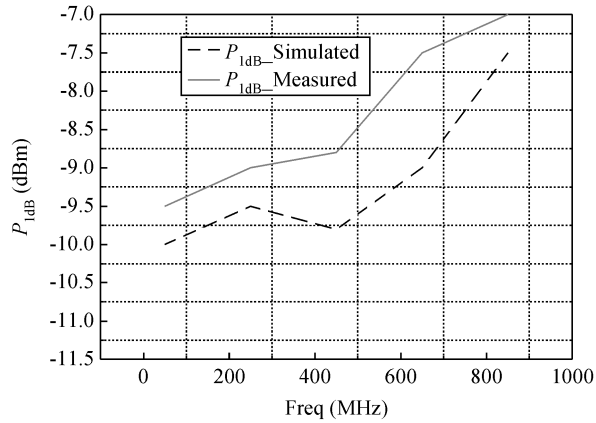

Fig. 12. Measured and simulated input 1 dB compression point.

the performances of the proposed LNA. Among all the LNAs without off-chip balun used for TV tuner applications, the CN-CLNA provides a better NF and consumes less power with less area. The linearity is not very good because the complementary topology consumes more voltage headroom. Combined with the constant-g_m bias circuit, the CNCLNA achieves a good gain balance over PVT, while other LNAs do not present the bias consideration. The performance comparison is listed in Table 1.

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