An asymmetrical sensing scheme for 1T1C FRAM to increase the sense margin*

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Abstract: A novel asymmetrical current-based sensing scheme for 1T1C FRAM is proposed, in which the two input transistors are not the same size and a feedback NMOS is added at the reference side of the sense amplifier. Compared with the conventional symmetrical scheme in Ref. [8], the proposed scheme increases the sense margin of the readout current by 53.9% and decreases the sensing power consumption by 14.1%, at the cost of an additional 7.89% area of the sensing scheme. An experimental FRAM prototype utilizing the proposed asymmetrical scheme is implemented in a 0.35 μm three metal process, in which the function of the prototype is verified.

Key words: FRAM; sense margin; current-based sense amplifier; asymmetrical
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1. Introduction

Ferroelectric random access memory (FRAM) has the advantage of low power consumption and fast access time. However, the density of FRAM is not high enough, because each storage cell is composed of two transistors and two capacitors. This is known as a 2T2C cell structure[1−3]. A more area-efficient FRAM uses only one transistor and one capacitor per storage cell, known as a 1T1C cell structure[4−7]. Figure 1[8] illustrates the schematics of the two cells along with provisions for their data sensing. The 1T1C cell consumes half of the area of the 2T2C cell, but sacrifices the sense margin. Here, the sense margin of the readout signal is defined as the minimum difference between the readout signal and the reference signal[9]. The larger the sense margin amplitude, the more reliable the reading operation will be. Normally, in 1T1C FRAM, the symmetrical sensing scheme is used and the reference signal is the arithmetic mean of S_0 and S_1, where S_0 and S_1 stand for the readout signal corresponding to a stored "0" and a stored "1", respectively. The maximal sense margin of the 1T1C structure is thus $(S_1 - S_0)/2$, only half of the 2T2C structure. In the scheme proposed by Wilson and Meadows[10], a symmetrical voltage sense amplifier is used. The reference voltage is $(V_1 + V_0)/2$ and the sense margin is $(V_1 - V_0)/2$. To balance the fatigue evenly between the memory cells and the reference cells, as shown in Fig. 2, a symmetrical current-based sensing scheme is proposed by Ref. [8], in which the bitline voltage is converted to current and is compared against a reference current $(I_1 + I_0)/2$, and the sense margin is $(I_1 - I_0)/2$. In this paper, an asymmetrical current-based sensing scheme to enlarge the sense margin of 1T1C FRAM is proposed. In this scheme, the readout signal should also be compared in the form of current, but the reference current is not fixed at $(I_1 + I_0)/2$. The reference current automatically rises when the readout current is small, and falls when the readout current is large.

2. Asymmetrical sensing scheme

In the scheme of Ref. [8] (see Fig. 2), current mirrors are used to mirror the currents converted from the readout voltages to a current sense amplifier. The current sense amplifier compares the currents and provides a voltage output signal. Because the input NMOS transistors are between the output nodes and GND, when the current mirror is working, there is current flowing through the input NMOS transistor. The output cannot be pulled up to VDD, and the sensing process cannot be completed, unless the current mirror is cut off. In this way, a lot of additional power consumption is needed. Therefore, a novel current-based sensing scheme is proposed. As a reference, a modified symmetrical sensing scheme with an improved current sense amplifier (see Fig. 3(a)) is proposed firstly, in which the input NMOS transistors (M1 and M2) are relocated between the source of M3/M4 and GND, where M3–M6 compose a current latched sense amplifier. Thus there is no current flowing from the output nodes to the ground, although the current mirrors are active, after the sensing process is completed. Therefore, the power consumption is reduced and the sense margin is nearly unchanged in the modified symmetrical scheme.

Based on the modified symmetrical sensing scheme above, an asymmetrical sensing scheme is proposed further, in which there are two special design approaches in the asymmetrical sensing scheme (see Fig. 3(b)). Firstly, the sizes of M1 and M2 are not the same. Secondly, there exists a feedback NMOS transistor connected in parallel to M2. The sense margin of the readout signal is the difference between I_{M3} and I_{M4}, where I_{M3} and I_{M4}, respectively, represent the current in M3 and M4. Here, I_{M3} equals the readout current I_x, which is converted from the bitline voltage V_x (V_1 or V_0). I_{M4} is the sum of the current in M2 and in the feedback NMOS transistor. In the modified symmetrical structure, the sizes of M1 and M2 are the same, so I_{M4} is fixed at $(I_1 + I_0)/2$, no matter whether BL is "0" or "1". However, in the proposed asymmetrical scheme, the

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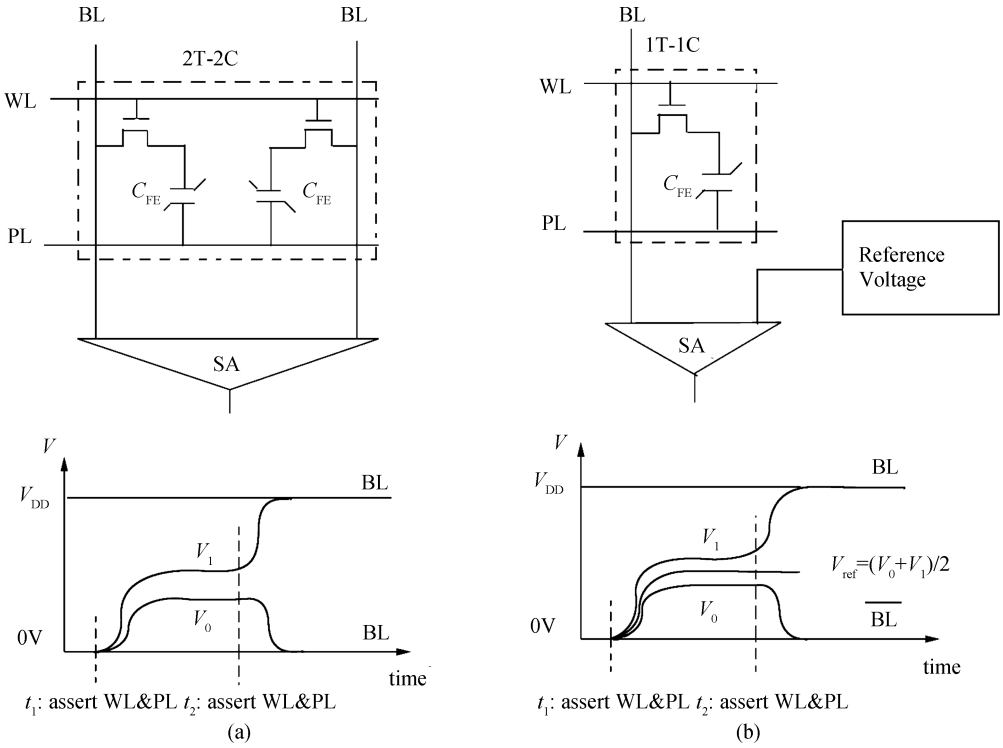

Fig. 1. Reference voltage generation for (a) 2T-2C architecture and (b) 1T-1C architecture[1].

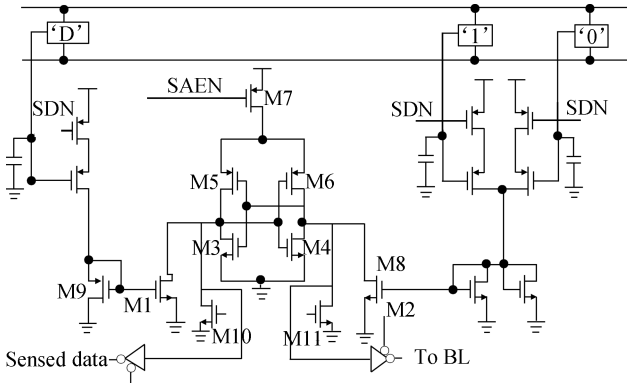

Fig. 2. Conventional symmetrical current-based sensing scheme[8].

size of M2 is smaller than M1, and the static reference current is relatively small. The feedback NMOS transistor provides a dynamic reference current depending on the bitline voltage. Therefore, the reference current in M4 will decrease when the readout current is large, and increase when the readout current is small. During the reading process, the readout voltages on BL (V_x), RBL (V_1) and /RBL (V_0) are converted to currents I_x, I_1 and I_0 by identical PMOS transistors. The reference current I_{M4} is formed by the current in M2 (I_{M2}) and the current in the positive-feedback-NMOS transistor (I_n). The current in M2 is $\alpha(I_1 + I_0)/2$ ($\alpha < 1$), and the current in the feedback NMOS is I_{n1} (large) when BL is "1" and is I_{n0} (small) when BL is "0". Because the voltages are converted to currents by PMOS transistors, the high voltage means a small current. In this way, when BL is "0", the current mirrored to M1 is large and the node OUT is pulled down to GND. The sense margin is $I_{n1} + I_{M2} - I_1$ when BL is "1", and $I_0 - I_{n0} - I_{M2}$

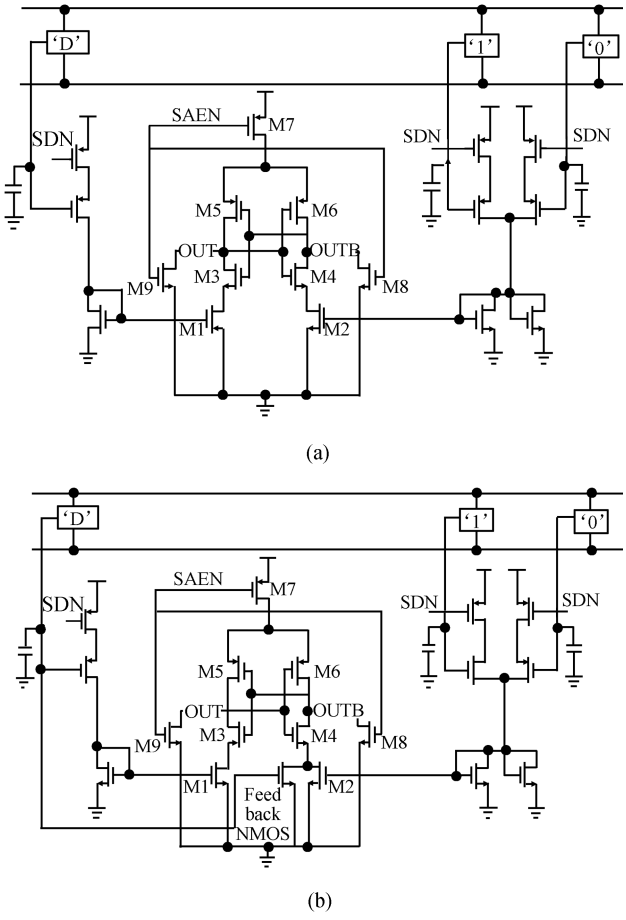

Fig. 3. (a) Modified symmetrical current-based sensing scheme. (b) Proposed asymmetrical current-based sensing scheme.

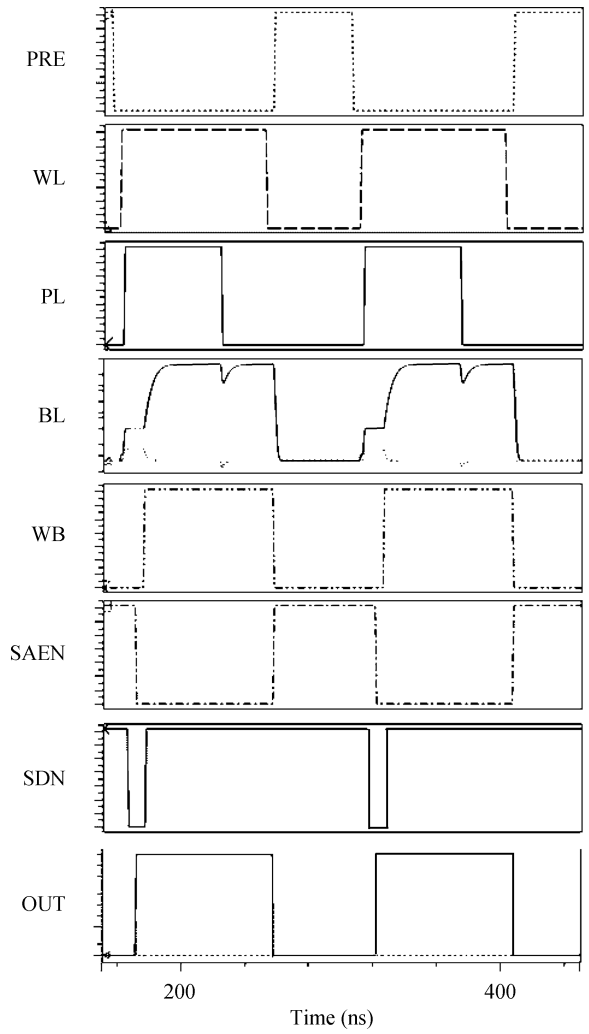

Fig. 4. Timing diagram of the proposed asymmetrical sensing scheme.

when BL is "0". In both cases, the sense margin in the proposed asymmetrical scheme is larger than the modified symmetrical scheme. At the same time, the power consumption of the sense scheme is nearly unchanged. Therefore, the proposed asymmetrical scheme can provide a larger sense margin and lower power consumption compared with the scheme of Ref. [8] (see Fig. 2).

After the read operation, a write-back must be taken, because the reading process is destructive, which is achieved by using an inverter controlled by a WB signal. This inverter reinforces the appropriate data on the bitline during the write-back cycle. Figure 4 shows the control signals and the critical voltages of the proposed asymmetrical sense amplifier as functions of time. After precharging nodes OUT and OUTB to GND and raising the selected WL and PL to VDD, the sensing process starts with the activation of the SDN signal that converts the voltages on BL, RBL, and RBL to currents. Once the currents are set up, the sense amplifiers are turned on by pulling the SAEN down. Then the currents in M3 and M4 compete to pull down their corresponding nodes, i.e. OUT and OUTB. The side with the smaller current will be VDD, forcing the other side falling down to GND. The sense operation is completed in less than 5 ns from the time of activating SDN.

3. Discussion and comparison

In this paper, the scheme proposed in Ref. [8], the modified symmetrical scheme and the proposed asymmetrical scheme are compared in the 0.35 μm FRAM technology with a bitline capacity of 0.6 pF. Figure 5 shows the simulated sense margins of the proposed asymmetrical scheme and the modified symmetrical scheme in a read cycle. It can be found that the sense margin of the former scheme is 117 μA, which is 1.5 times as large as the latter one (78 μA). Because of the dynamic reference current, the limitation of the sense margin in 1T1C FRAM is broken. The reference current in M4 is no longer fixed at a static value. Instead, it can change towards the opposite direction of the readout current, which enlarges the current difference between both sides of the sense amplifier. How large the sense margin could be depends on three important coefficients, α, β and γ, which are defined in Eqs. (1)–(3).

$$I_{\mathrm{M2}} = \alpha \frac{I_0 + I_1}{2}, \quad \alpha < 1, \tag{1}$$

$$I_{\mathrm{n0}} = \beta I_{\mathrm{n1}}, \quad \beta < 1, \tag{2}$$

$$I_0 = \gamma I_1, \quad \gamma > 1. \tag{3}$$

In the proposed asymmetrical scheme, M2 is half the size of M1, α is thus 1/2. I_1 and I_0 are 44.2 μA and 184 μA, respectively, and β is therefore 0.24. I_{n1} and I_{n0} are 133 μA and 5.64 μA, respectively, and γ is therefore 23.6. It is notable that current flows through the feedback NMOS transistor no matter whether BL is "0" or "1". Therefore, Equation (4) must be satisfied to make the sense margins of "1"and "0" the same,

$$\frac{I_0 + I_1}{2} = I_{\mathrm{M2}} + \frac{I_{\mathrm{n0}} + I_{\mathrm{n1}}}{2}. \tag{4}$$

In this way, the sense margin of the readout signal is shown in Eq. (5). In contrast, it is only $(\gamma - 1)I_1/2$ if the reference current is generated by a modified symmetrical scheme.

$$\begin{aligned} \mathrm{SenseMargin} &= (I_{\mathrm{M2}} + I_{\mathrm{n1}}) - I_1 \\ &= \frac{I_0 - I_1}{2} + \frac{I_{\mathrm{n1}} - I_{\mathrm{n0}}}{2} \\ &= \frac{(\gamma - 1)I_1}{2} + \frac{(1-\beta)(1+\gamma)}{2(\beta+1)} I_1(1-\alpha). \end{aligned} \tag{5}$$

The sense margin can be adjusted by α, β and γ. β and γ are decided by the process character, and can not be modified by designers. So the changeable coefficient α has a linear relation to the sense margin (smaller α means a larger sense margin). α is decided by the W/L of M2, which has the minimum size. The smallest α in the proposed scheme is chosen as 0.5 to reach the largest sense margin of 117 μA. Figure 6 shows a comparison of the sensing courses between the proposed schemes in this paper and the scheme in Ref. [8]. An experimental FRAM prototype utilizing the proposed asymmetrical scheme is implemented in a 0.35 μm three metal process, in which the function of the prototype are verified.

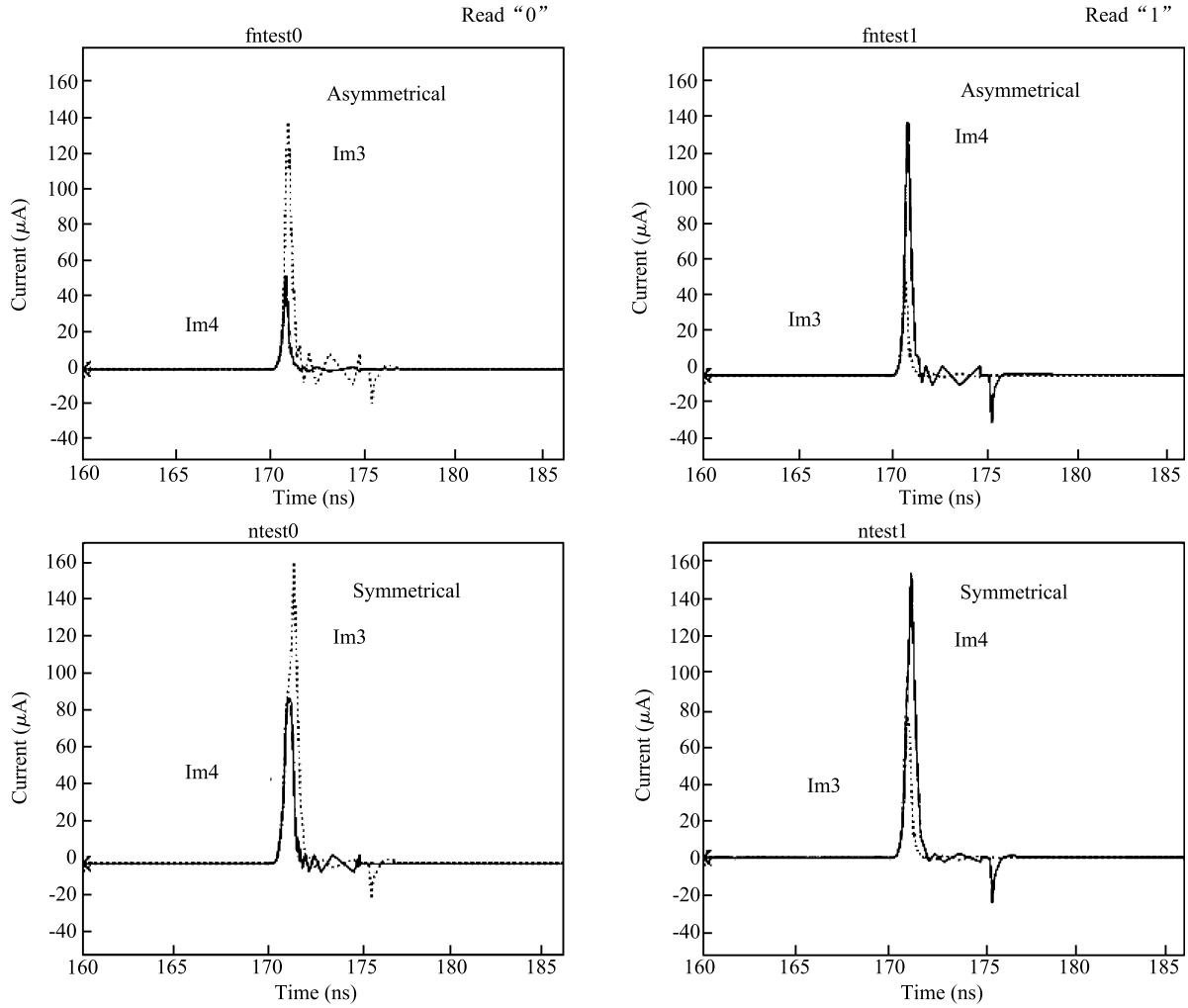

Fig. 5. Sense margins in a read cycle of the proposed asymmetrical scheme and the modified symmetrical scheme.

Table 1. Comparison of the key performances of the sensing schemes mentioned in this paper.

Parameter	Scheme proposed by Joseph and Yadollah[8]	Modified symmetrical scheme	Proposed asymmetrical scheme
Sense margin (μA)	76	78	117
Sensing time (ns)	5.9	5.7	5.6
Sensing power (mW)	1.35	1.16	1.16
Area (μm^2)	26.6	26.6	28.7

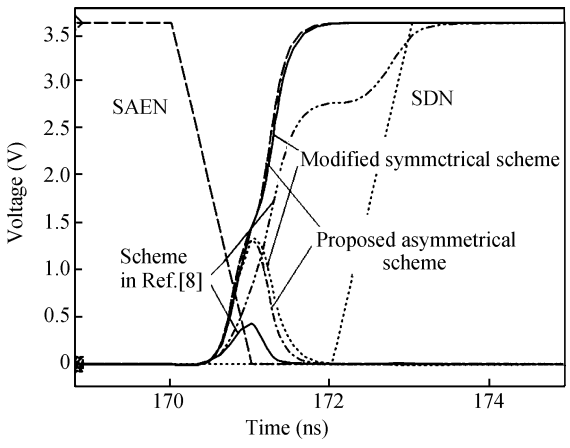

Fig. 6. Comparison of the sensing courses of the schemes mentioned in this paper.

4. Conclusion

An asymmetrical current-based sensing scheme for 1T1C FRAM is proposed, in which, due to two input transistors with different sizes and an added feedback NMOS at the reference side of the sense amplifier, the reference current can be adjusted automatically depending on the readout current in order to enlarge the sense margin. As a reference in the analysis, a modified symmetrical current-based sensing scheme based on the conventional symmetrical scheme in Ref. [8] is also proposed. Compared with the two symmetrical schemes above, the proposed asymmetrical scheme increases the sense margin of the readout current obviously by over 50% at the expense of the addition of less than 8% of the area of the sensing scheme. An experimental FRAM prototype utilizing the proposed asymmetrical scheme is implemented in a 0.35 μm three metal process, in which the function of the prototype is verified. Furthermore, the proposed asymmetrical sensing scheme

can be used in other memories, such as DRAM and Flash.

All the details of the key performances of the schemes mentioned above are illustrated in Table 1. Since the output is not connected to the bitline directly in the current-steering sense amplifier, the output loads of all three schemes are small. Thus the sensing speed can be improved less in the proposed scheme, as shown in Fig. 6. Both the proposed asymmetrical scheme and the modified symmetrical scheme show the same sensing power consumption, but less than that in the scheme in Ref. [8] by 14.1%. By adding a feedback NMOS transistor, the area of the proposed asymmetrical sensing scheme is increased only by 7.89% in contrast with the modified symmetrical structure and the scheme in Ref. [8].

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