A wideband low power low phase noise dual-modulus prescaler

Lei Xuemei(雷雪梅)[1,2], Wang Zhigong(王志功)[1,†], and Wang Keping(王科平)[1]

[1]Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China
[2]Inner Mongolia University, Hohhot 010021, China

Abstract: This paper describes a novel divide-by-32/33 dual-modulus prescaler (DMP). Here, a new combination of DFF has been introduced in the DMP. By means of the cooperation and coordination among three types, DFF, SCL, TPSC, and CMOS static flip-flop, the DMP demonstrates high speed, wideband, and low power consumption with low phase noise. The chip has been fabricated in a 0.18-μm CMOS process of SMIC. The measured results show that the DMP's operating frequency is from 0.9 to 3.4 GHz with a maximum power consumption of 2.51 mW under a 1.8 V power supply and the phase noise is –134.78 dBc/Hz at 1 MHz offset from the 3.4 GHz carrier. The core area of the die without PAD is 57×30 μm^2. Due to its excellent performance, the DMP could be applied to a PLL-based frequency synthesizer for many RF systems, especially for multi-standard radio applications.

Key words: dual-modulus prescaler; wideband; low power; low phase noise; frequency synthesizer; multi-standard radio

DOI: 10.1088/1674-4926/32/2/025011 **EEACC:** 2570

1. Introduction

In a frequency synthesizer, the frequency divider is a critical block in the feedback path, which works at a high frequency and consumes a lot of the circuit power. In order to reduce the power consumption, the DMP is most widely applied in integer or fractional-N frequency synthesizers. In most cases, the clock signals of the DMP are directly supplied by a VCO (voltage controlled oscillator) so that the structure optimization of synchronous counter is essential to increase the operating frequency of the prescaler and to lower the power consumption in the design[1]. With the development of wireless communications, the wireless communication scenario is dominated by the simultaneous presence of a variety of standards, which cover different applications and employ a wide range of frequency. Thus, the DMP must have a wide frequency range too. In consequence, the design efforts are to reduce the power consumption and to increase the operating frequency, and the range of operating frequency should be comprehensively considered in the process of the DMP design.

A high-speed DMP is usually based on one type of topology: SCL (source couple logic)[2–4], TSPC (true-single-phase-clock)[1,5,6] or E-TSPC (extended true-single-phase-clock)[7–9], and the remarkable characteristic of it is high wideband or low power. But wideband and low power are not achieved simultaneously. On the other hand, a typical DMP based on SCL or TPSC has three parts: a synchronous dual-modulus divider, an asynchronous divider, and the combination logic circuits. Optimization of these structures was focused on the synchronous dual-modulus divider to obtain high speed and lower power consumption and was not concerned with other parts in the design. In practice, three parts of the DMP are the cooperation and coordination and should be comprehensively considered. Furthermore, the DMP with high speed, wide band, low power consumption, and high spectrum purity is more and more important for multi-standard radio applications.

In this paper, we present a high-speed, wide-band, low-power, and low phase noise divide-by-32/33 DMP for multi-standard radio frequency synthesizers. The DMP is based on SCL, TSPC and CMOS static flip-flop. The basic circuit structure of the synchronous dual-modulus divider is SCL, and the asynchronous divider includes TSPC and CMOS static flip-flop. The architecture of the divide-by-4/5 divider and the asynchronous counter ensure that the whole circuit is suited to multi-standard radio applications. The circuit is implemented in a 0.18 μm CMOS technology of SMIC.

2. Architecture of the DMP

The block diagram of the proposed DMP is shown in Fig. 1. In this diagram, three blocks can be identified. The first block is composed of three SCL fall edge-triggered D-flip flops (D-FF) without external logic gates. It is a synchronous divide-by-4/5 divider. The second block is composed of one TPSC and two CMOS static flip-flop DFFs. It is an asynchronous divide-by-8 divider. The last block is a combination logic circuit to generate internal signal V_c through the MC signal and the asynchronous divider output signal. When internal signal V_c is logical high ($V_c = 1$), the division ratio of the divide-by-4/5 counter is 4; otherwise, the division ratio is 5. The signal MC is used to select the dual-modulus division ratio 32 or 33. When the internal signal MC is logical high (MC = 1), the division ratio of the DMP is 32; otherwise, the division ratio is 33.

The divide-by-4/5 divider is the most crucial block in the whole circuit. It works at the highest frequency, consumes the most power, and limits the range of operating frequency that the DMP could reach. A lot of effort has been put into the design of the divide-by-4/5 divider. Many optimization methods have already been proposed[1,2]. We choose the SCL structure

† Corresponding author. Email: zgwang@seu.edu.cn
Received 10 June 2010, revised manuscript received 13 October 2010

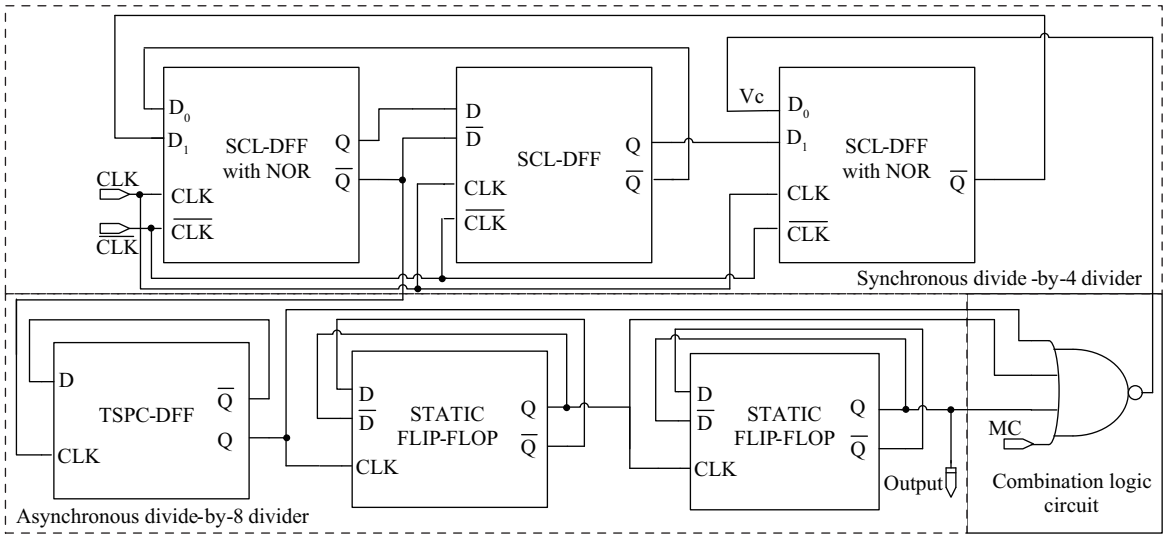


Fig. 1. Architecture of the DMP.

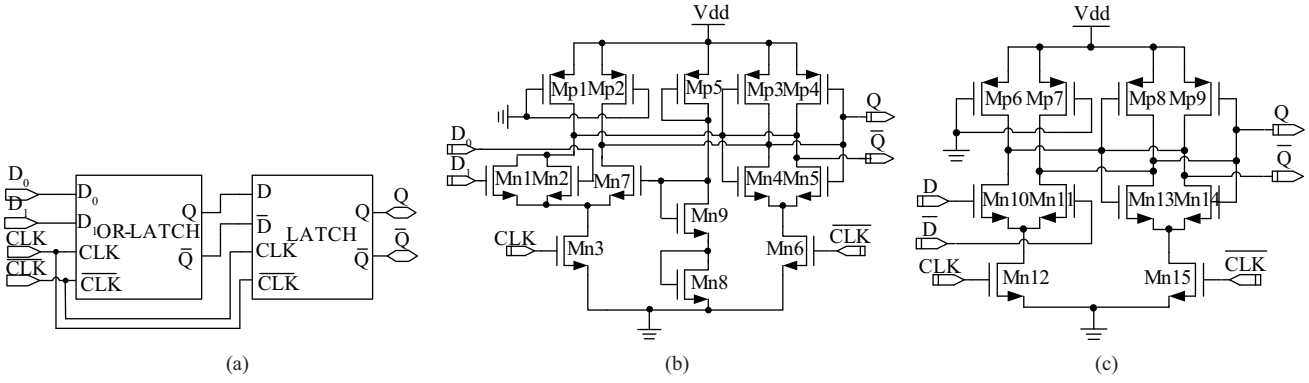


Fig. 2. Schematic of (a) the DFF with OR, (b) OR-latch, and (c) D latch.

including one D-flip-flop (DFF) and two OR-flip-flops (OR-FFs)[2]. Merging the OR gate and DFF based on the SCL ensure that the divide-by-4/5 divider can achieve a high speed and a low power. Many modifications and the parameter optimization are made to adapt the speed and wideband requirements of the DMP.

Figure 2 shows the block diagram of the DFF with OR and the schematic of two kinds of latch used in the divide-by-4/5 divider. It uses a master-slave structure. Each D latch is triggered by two differential clock signals, CLK or $\overline{\text{CLK}}$. These two latches always operate periodically and alternately between the sampling mode and the holding mode. Compared to the original one in Ref. [2], the gate of the load transistors in the proposed DFF is connected to the ground instead of the drain in order to the VDD instead of a transistor in order to lower the power consumption and increase the swing of the output signals. The disadvantage of the modifications is that the output signals are asymmetrical. Fortunately, the circuit following the proposed DFF is edge-triggered TSPC DFF in the DMP and does not affect the performance of the whole circuit.

The asynchronous counter consists of three D-flip-flops. Its operating frequency is one-fourth or one-fifth of the input frequency, so the speed requirement is decreased. However, it is required that the DFF has low power consumption, a wide band, and a low phase noise. According to the efficiency and demands of speed and low power consumption, the TSPC shown in Fig. 3(a)[10] was chosen for the first D-flip-flop, and the parameters of the transistors were optimized to suit the requirements of the speed and operating frequency range. However, this structure is not suitable for low speed and good noise performance. The demands of the next two DFFs shown in Fig. 3(b) are low power consumption and good noise performance. According to the analysis above, a CMOS static DFF was chosen. Using such a structure, a good phase noise performance and a large operating frequency range can be obtained. Moreover, it consumes zero static power.

3. Circuit design

In this design, an SCL circuit structure has been employed in the design since it can work at a high speed and wide band. The TSPC circuit structure has been employed in the design since it can work at high speed with low power consumption. The CMOS static flip-flop circuit structure has been employed to ensure suitable speed and the low phase noise with low power. So the optimization of SCL and TSPC is focused on maximum operating frequency; the optimization of the CMOS static flip-flop is focused on good noise performance.

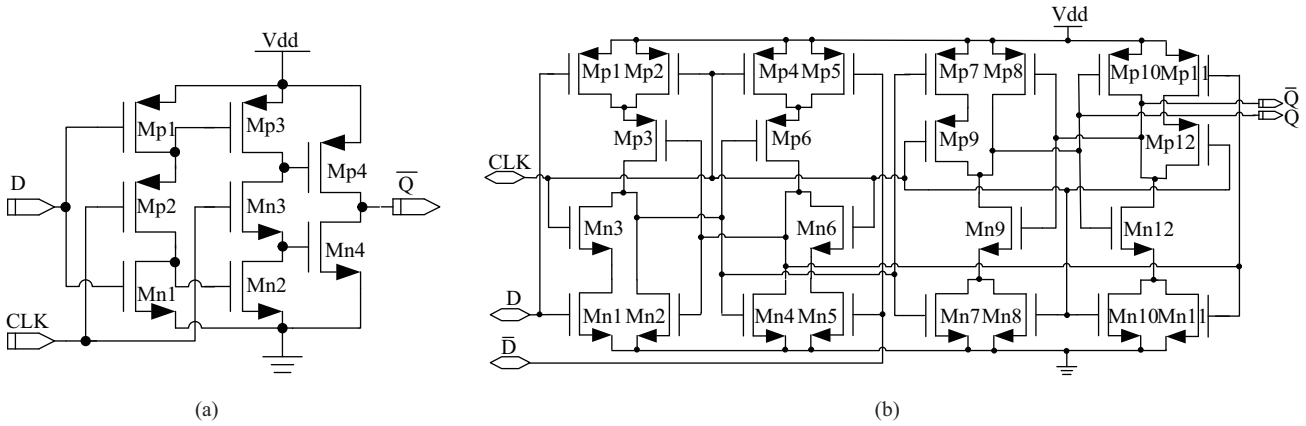


Fig. 3. Schematics of the in asynchronous counter. (a) TSPC DFF. (b) CMOS static DFF.

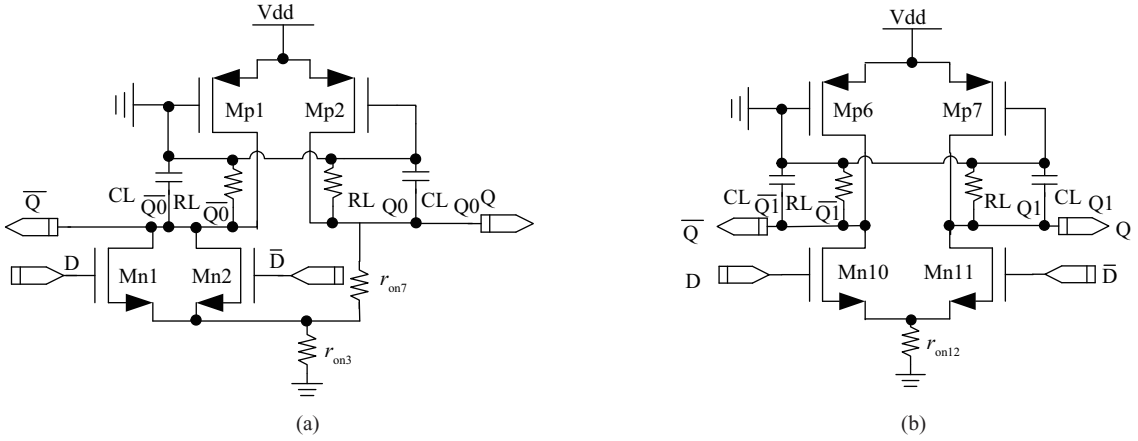


Fig. 4. Simplified schematic of (a) OR-latch in sampling mode and (b) latch in sampling mode.

3.1. Optimization of SCL DFF

The maximum operating frequency of the DMP is decided by the divided-by-4/5divider and SCL-DFF with OR and is the key module in the divide-by-4/5 divider. The speed of the proposed divided-by-4/5 divider is determined by the sampling time of the SCL-DFF. To predict the maximum operating frequency of the SCL DFF with OR, the simplified schematics of the sampling are shown in Fig. 4.

3.1.1. Sampling time of OR-type D-latch

It is supposed that at the beginning, the CLK signal is at the high level and the $\overline{\text{CLK}}$ signal is at the low level. The OR-type D-latch is in the sampling state and the D latch is in the holding state.

Figure 4(a) shows the simplified schematic of the OR-type D-latch in sampling mode. It is supposed that at the beginning, D_0 or D_1 and $\overline{Q}$ ports are at the high level, then Q port is at the low level. Thus, one of Mn1 and Mn2 turns on; another turns off. The charge-down time constant ($\tau_{d\overline{Q11}}$) is given by

$$\tau_{d\overline{Q11}} \approx (C_{DSMp1} + C_{DSMn1} + C_{DSMn2} + CL_{\overline{Q0}}) \times \left[r_{onMp1} || (r_{on3} + r_{onMn2}) || RL_{\overline{Q0}}\right]. \quad (1)$$

And the charge-up time constant (τ_{uQ11}) is given by

$$\tau_{uQ11} \approx \left(C_{DSMp2} + CL_{Q0}\right) \times \left[(r_{on7} + r_{on3}) || r_{onMp2} || RL_{Q0}\right], \quad (2)$$

where r_{on3}, r_{onMp1}, r_{onMn2}, r_{onMp2} and r_{on7} are the on-resistance of Mn3, Mp1, Mn2, Mp2 and Mn7. $RL_{\overline{Q0}}$ and RL_{Q0} include the parasitic and load resistance. $CL_{\overline{Q0}}$ and CL_{Q0} include the load and parasitic capacitance.

If D_0, D_1, and $\overline{Q}$ ports are at the high level, then Q port is at the low level, and Mn1 and Mn2 turn on. The charge-down time constant ($\tau_{d\overline{Q12}}$) is given by

$$\tau_{d\overline{Q12}} \approx (C_{DSMp1} + C_{DSMn2} + C_{DSMn1} + CL_{\overline{Q0}}) \times \left[r_{onMp1} || (r_{on3} + r_{onMn1} \| r_{onMn2}) || RL_{\overline{Q0}}\right], \quad (3)$$

and the charge-up time constant (τ_{uQ12}) is given by

$$\tau_{uQ12} \approx \left(C_{DSMp2} + CL_{Q0}\right) \times \left[(r_{on7} + r_{on3}) || r_{onMp2} || RL_{Q0}\right], \quad (4)$$

where r_{onMn1} is the on-resistance of Mn1.

If D_0, D_1, and $\overline{Q}$ ports are at the low level, then Q port is at the high level, and Mn1 and Mn2 turn off. The charge-down time constant (τ_{dQ11}) is given by

$$\tau_{dQ11} \approx \left(C_{DSMp2} + CL_{Q0}\right) \times \left[(r_{on7} + r_{on3}) || r_{onMp2} || RL_{Q0}\right], \quad (5)$$

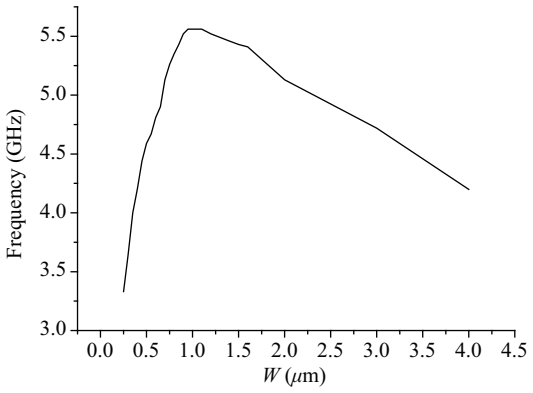


Fig. 5. Maximum operation frequency versus width of Mn1 and Mn2.

and the charge-up time constant ($\tau_{u\overline{Q1}}$) is given by

$$\tau_{u\overline{Q1}} \approx (C_{\mathrm{DSMp1}} + C_{\mathrm{DSMn1}} + C_{\mathrm{DSMn2}} + CL_{\overline{Q0}}) \left[r_{\mathrm{onMp1}} || RL_{\overline{Q0}}\right]. \quad (6)$$

3.1.2. Sampling time of D-latch

It is supposed that at the beginning, the CLK signal is at the low level and the $\overline{\mathrm{CLK}}$ signal is at the high level. The OR-type D-latch is in holding state and the D-latch is in the sampling state.

Figure 4(b) shows the simplified schematic of the D-latch in sampling mode. If D and $\overline{\mathrm{Q}}$ ports are at the high level, then, $\overline{\mathrm{D}}$and Q ports are at the low level, Mn10 turns on and Mn11 turns off. The charge-down time constant ($\tau_{\overline{dQ21}}$) is given by

$$\tau_{\overline{dQ21}} \approx (C_{\mathrm{DSMp6}} + C_{\mathrm{DSMn10}} + CL_{\overline{Q1}}) \times \left[r_{\mathrm{onMp6}} || \left(r_{\mathrm{on12}} + r_{\mathrm{onMn10}}\right) || RL_{\overline{Q1}}\right], \quad (7)$$

and the charge-up time constant (τ_{uQ21}) is given by

$$\tau_{\mathrm{uQ21}} \approx \left(C_{\mathrm{DSMp7}} + C_{\mathrm{DSMp11}} + CL_{\mathrm{Q1}}\right) \times \left(r_{\mathrm{onMp7}} || RL_{\mathrm{Q1}}\right), \quad (8)$$

where r_{on12}, r_{onMp6}, r_{onMn10}, and r_{onMp7} are the on-resistance of Mn12, Mp6, Mn10, and Mp7. respectively; $RL_{\overline{Q1}}$ and RL_{Q1} include parasitic and load resistance; $CL_{\overline{Q1}}$ and CL_{Q1} include load and parasitic capacitance.

3.1.3. Circuit optimization of the SCL DFF with OR

To compare the sampling time of the OR-type D-latch and the D-latch, the sampling time of the OR-type D-latch is larger than that of the D-latch because it is integrated with the "OR" logic gate. So the maximum operation frequency is determined by the $\overline{\mathrm{Q}}$ ports of the OR-type D-Latch. According to the analysis above, the sizes of Mn1 and Mn2 are the key of the SCL DFF with OR. The relation of the maximum operation frequency and the sizes of Mn1 and Mn2 are shown in Fig. 5. The maximum operation frequency of DMP is 3 GHz, so the width of Mn1 and Mn2 is set to 750 nm.

3.2. Optimization of TSPC divided-by-2 divider

The operation frequency of TSPC DFF is one-quarter or one-fifth of the divided-by-4/5 divider and the range of it is from 200 to 800 MHz. To decrease the power consumption and keep high speed, the split-output latch stage is applied. To predict the suitable size of transistors, the sampling and holding time constants of the key nodes are analyzed, according to Fig. 3(a).

It is supposed that at the beginning, the CLK signal is at the low level. Thus, Mp2 turns on and Mn3 turns off. If D is at the high level, Mp1 turns off and Mn1 turns on, otherwise Mn1 turns off and Mp1 turns on. At the gates of Mp3 and Mn2, the charge-down time constant (τ_{down1}) and the charge-up time constant (τ_{up1}) are given by

$$\tau_{\mathrm{down1}} \approx \left[C_{\mathrm{GMp3}} + C_{\mathrm{DSMp1}} + (C_{\mathrm{GMn2}} + C_{\mathrm{DSMn1}}) \,\|\, C_{\mathrm{DSMp2}}\right] \times \left(r_{\mathrm{onMn1}} + r_{\mathrm{onMp2}}\right), \quad (9)$$

$$\tau_{\mathrm{up1}} \approx \left[C_{\mathrm{GMn2}} + C_{\mathrm{DSMn1}} + \left(C_{\mathrm{GMp3}} + C_{\mathrm{DSMp1}}\right) \,\|\, C_{\mathrm{DSMp2}}\right] \times \left(r_{\mathrm{onMp1}} + r_{\mathrm{onMp2}}\right), \quad (10)$$

where r_{onMn1}, r_{onMp1} and r_{onMp2} are the on-resistance of Mn1, Mp1 and Mp2, respectively. At the same time, the gates of Mn4 pre-charge down or Mp4 pre-charge up. If the CLK changes to low level, Mn3 turns on and Mp2 turns off. The gate level of Mn4 or Mp4 has already reached and begins to hold. Thus, Mn4 or Mp4 turns on. The $\overline{\mathrm{Q}}$ port begins to charge up or down. The charge-down time constant (τ_{down2}) and charge-up time constant (τ_{up2}) are written as

$$\tau_{\mathrm{down2}} \approx (C_{\mathrm{GMp1}} + C_{\mathrm{GMn1}} + C_{\mathrm{DSMp4}} + C_{\mathrm{DSMn4}} + C_{\mathrm{L}}) \times (r_{\mathrm{onMn4}} \,\|\, R_{\mathrm{L}}), \quad (11)$$

$$\tau_{\mathrm{up2}} \approx (C_{\mathrm{GMp1}} + C_{\mathrm{GMn1}} + C_{\mathrm{DSMp4}} + C_{\mathrm{DSMn4}} + C_{\mathrm{L}}) \left(r_{\mathrm{onMp4}} \,\|\, R_{\mathrm{L}}\right), \quad (12)$$

where r_{onMn4} and r_{onMp4} are the on-resistance of Mn4 and Mp4, respectively. Then, when the CLK changes to high level, the $\overline{\mathrm{Q}}$ port begins to hold and the gates of Mn4 and Mp4 stop to share charge. Thus the holding time constant (τ_{hold}) of $\overline{\mathrm{Q}}$ port is given by

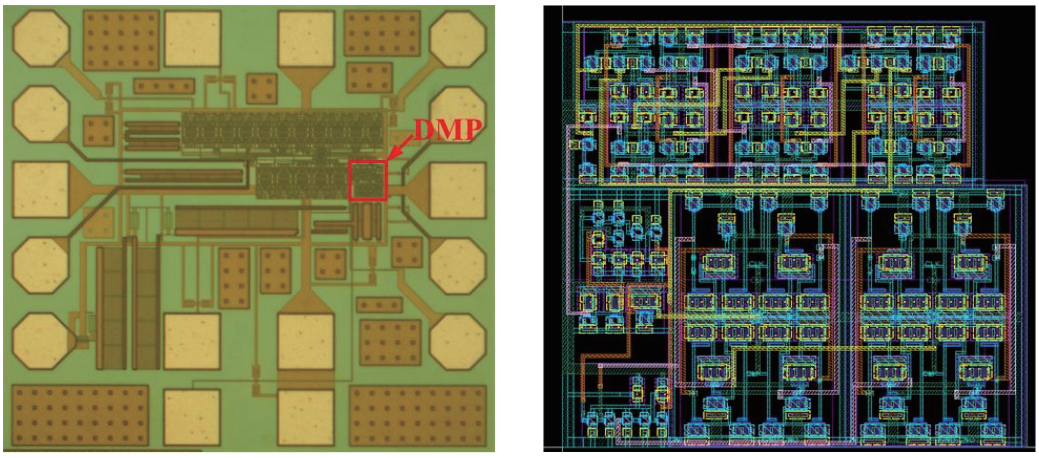
$$\tau_{\mathrm{hold}} \approx \left(C_{\mathrm{GMp1}} + C_{\mathrm{GMn1}} + C_{\mathrm{DSMn4}} + C_{\mathrm{DSMp4}} + C_{\mathrm{L}}\right) \times (r_{\mathrm{DSMn4}} \,\|\, R_{\mathrm{L}}), \quad (13)$$

or

$$\tau_{\mathrm{hold}} \approx \left(C_{\mathrm{GMp1}} + C_{\mathrm{GMn1}} + C_{\mathrm{DSMn4}} + C_{\mathrm{DSMp4}} + C_{\mathrm{L}}\right) \times \left(r_{\mathrm{DSMp4}} \,\|\, R_{\mathrm{L}}\right), \quad (14)$$

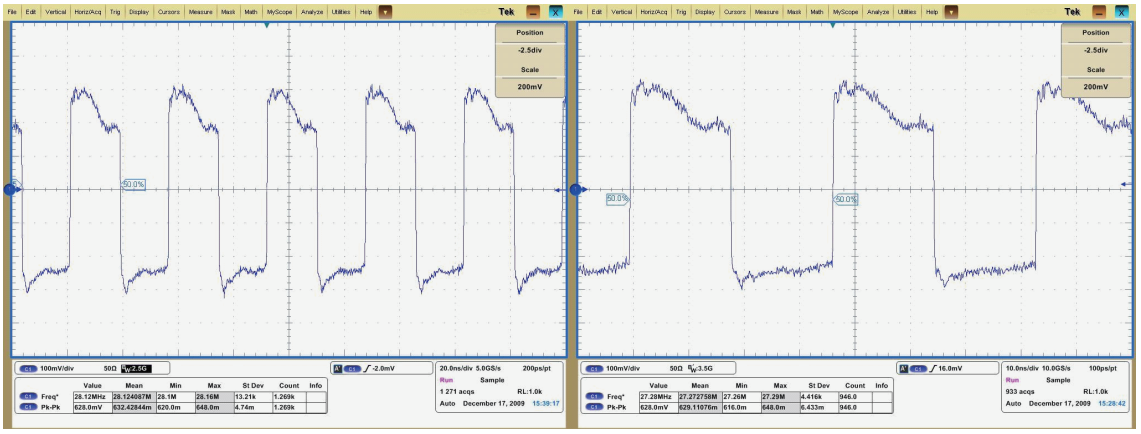
where r_{DSMn4} and r_{DSMp4} are off-resistance of Mn4 and Mp4; R_{L} is the load resistance and C_{L} is the load capacitance.

According to the analysis above and the characteristics of TSPC circuit, the NMOS transistor size is minimum technology size and the PMOS transistor size is nearly twice that of the NMOS to ensure the maximum operation frequency and low power consumption.

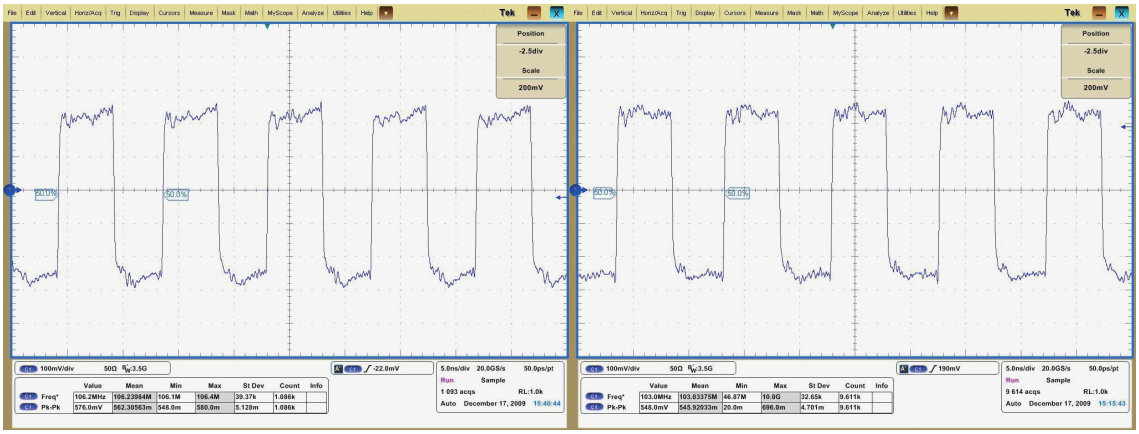


(a) (b)

Fig. 6. (a) Chip photograph, and (b) layout of the proposed DMP.



(a) (b)



(c) (d)

Fig. 7. Measured output waves of the proposed (a) divide-by-32 with input frequency 0.9 GHz, (b) divide-by-33 with input frequency 0.9 GHz, (c) divide-by-32 with input frequency 3.4 GHz, and (d) divide-by-33 with input frequency 3.4 GHz.

3.3. Optimization of CMOS static DFF divided-by-2 divider

The maximum operation frequency of the CMOS static DFF is 400 MHz and it is easy to realize in the SMICs 0.18-μm CMOS process. The size of transistors in Fig. 3(b) is needed to achieve the best noise performance. Thus, the NMOS transistors sizes should ensure route length equalization according to the branching effort of the logic gate with minimum size.

4. Measured results

To verify the performance of the DMP, a circuit was implemented in the SMICs 0.18-μm CMOS process. Figure 6 shows the micrograph of the fabricated DMP (which is marked). The core area is 57×30 μm^2.

Figure 7 shows the measured output waveforms of the fabricated DMP divided by 32 and 33 when the input signal frequency is 3.4 GHz and 0.9 GHz, respectively, with the power

Table 1. Comparaision with published results.

Reference	Technology	Operating frequency range (GHz)	Division ratio	Power consumption (mW)
Ref. [1]	0.25 μm CMOS	2.5	64/65	35 (include buffers)
Ref. [2]	0.18 μm CMOS	4.5	8/9	5.76
Ref. [3]	0.35 μm CMOS	2.6–2.4	4/5	36.4
Ref. [9]	0.18 μm CMOS	3–4.6	16/17	9.7
This work	0.18 μm CMOS	0.9–3.4	32/33	2.51

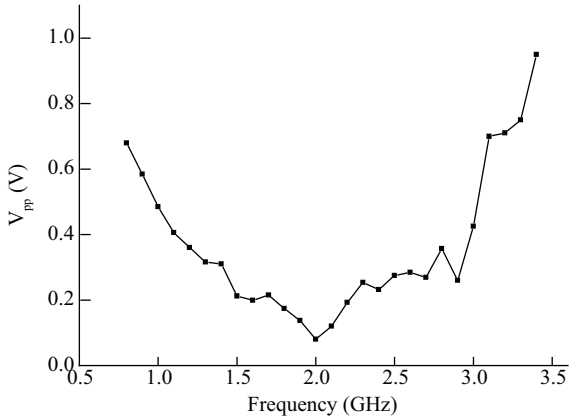


Fig. 8. The sensitivity measured from the proposed DMP.

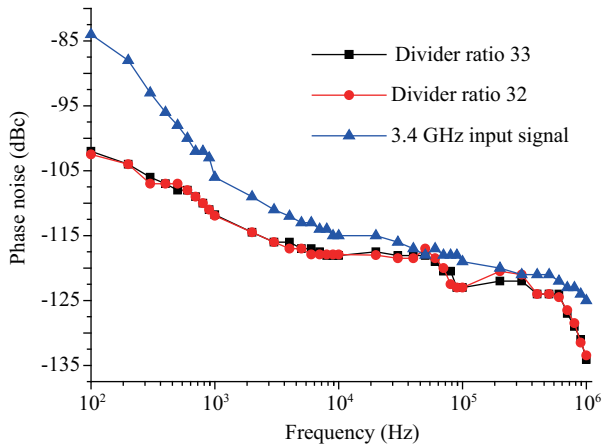


Fig. 9. Phase noise measured from the proposed DMP at the input signal frequency of 3.4 GHz.

supply voltage of 1.8 V. Above the minimum input voltage, reliable operation is guaranteed. The measured minimum input sensitivity V_{P-P} versus the input frequency of the DMP is plotted in Fig. 8. The minimum input voltage of the frequency dividers is less than 0.95 V in the frequency range of 0.9–3.4 GHz. The minimum input signal peak for a DMP working at 3.4 GHz and 0.9 GHz is 0.95 V and 0.59 V, respectively. The maximum power supply current measured was 4 mA, including power-hungry larger output buffers. According to the simulated results, we estimate the maximum current of the DMP core to be about 1.71 mA.

The phase noise of the output signal and the 3.4 GHz input signal is measured by means of a spectrum analyzer. The results are shown in Fig. 9. We can see that the phase noise does not change with division ratio obviously. On the other hand, the phase noise of the output signals is not reduced in proportion with the phase noise of the input signal. This is because the phase noise of the output signals include the effect of the input signal phase noise (PN_{ein}), the phase noise of the sampling effect (PN_{sp}), the phase noise of the measuring instrument (PN_{mi}), the phase noise of test circuits of proposed frequency divider (PN_{tc}) and the phase noise of the proposed frequency divider circuit (PN_{fd}). The relation of them is

$$\begin{aligned} PN_{total} &= PN_{fd} + PN_{ein} + PN_{sp} + PN_{mi} + PN_{tc} \\ &= PN_{fd} + PN_{in} - 10\lg N + PN_{sp} + PN_{mi} + PN_{tc}, \end{aligned} \tag{15}$$

where PN_{in} is the phase noise of the input signal and N is the divider ratio.

5. Conclusion

In this paper, a divide-by-32/33 DMP based on three kinds of topology DFF is proposed. An OR-FF SCL structure is applied to improve performance of the synchronous divider. A TSPC and CMOS static DFF structure is used to assure the high speed, wideband, low power consumption and low phase noise. The design circuit was implemented in a SMICs 0.18-μm CMOS process. The measured results show that the operating frequency range of the DMP is from 0.9 to 3.4 GHz; the phase noise is –134.78 dBc/Hz at 1 MHz offset from 3.4 GHz carrier; the static power consumption is 2.14 mW; and the average power consumption is 2.51 mW at 3.4 GHz with a 1.8 V supply voltage. A comparison of this DMP with other recently published results is listed in Table I. It is shown that the proposed structure has the lowest power consumption and the largest range of operating frequency. The presented DMP is thus particularly suited to a multi-standard, ultra-wideband, low-power consumption frequency synthesizer.

Acknowledgement

The authors are grateful for the help and support of Zhou Jianzheng and Li Wei. Technology access from SMIC is also appreciated.

References

[1] Chi Baoyong, Shi Bingxue. A novel CMOS dual-modulus prescaler based on new optimized structure and dynamic circuit technique. Chinese Journal of Semiconductors, 2002, 23(4): 357

[2] Xu Yong, Wang Zhigong, Li Zhiqun, et al. A novel high-speed lower-jitter lower-power dissipation dual-modulus prescaler and applications in PLL frequency synthesizer. Chinese Journal of Semiconductors, 2005, 26(1): 176

[3] Li Zhiqiang, Chen Liqiang, Zhang Jian, et al. A programmable 2.4 GHz CMOS multi-modulus frequency divider. Journal of Semiconductors, 2008, 29(2): 521

[4] Shu K, Sánchez-Sinencio E, Silva-Martínez J, et al. A 2.4-GHz monolithic fractional-N frequency synthesizer with robustphase-switching prescaler and loop capacitance multiplier. IEEE J Solid-State Circuits, 2003, 38(6): 866

[5] Huang Q, Rogenmoser R. Speed optimization of edge-triggered CMOS circuits for gigahertz single-phase clocks. IEEE J Solid-State Circuits, 1996, 31(3): 456

[6] De Miranda F P H, Navarro Jr S J, van Noije W A M. A 4 GHz dual modulus divider-by 32/33 prescaler dual modulus divider-by 32/33 prescaler in 0.35pm CMOS technology. SBCCIPemanbuca, Brazil, 2004: 94

[7] Guo C, Zhu S, Hu J, et al. Design and optimization of dual modulus prescaler using the extended true-single-phase-clock. International Conference on Microwave and Millimeter Wave Technology, Chengdu, China, 2010: 636

[8] Bazzazi A, Nabavi A. Design of a low-power 10 GHz frequency divider using extended ture single phase clock (E-TSPC). Electronic and Photonic Devices & Systems, 2009:173

[9] Guo S, Huang L, Bai X. A 4-GHz CMOS dual-modulus prescaler with enhanced input sensitivity over extended operation range. 11th IEEE International Conference on Communication Technology Processing, 2008: 331

[10] Yuan J, Svensson C. High-speed CMOS circuit technology. IEEE J Solid-State Circuits, 1989, 24(1): 62