A novel analog/digital reconfigurable automatic gain control with a novel DC offset cancellation circuit*

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Abstract: An analog/digital reconfigurable automatic gain control (AGC) circuit with a novel DC offset cancellation circuit for a direct-conversion receiver is presented. The AGC is analog/digital reconfigurable in order to be compatible with different baseband chips. What's more, a novel DC offset cancellation (DCOC) circuit with an HPCF (high pass cutoff frequency) less than 10 kHz is proposed. The AGC is fabricated by a 0.18 μm CMOS process. Under analog control mode, the AGC achieves a 70 dB dynamic range with a 3 dB-bandwidth larger than 60 MHz. Under digital control mode, through a 5-bit digital control word, the AGC shows a 64 dB gain control range by 2 dB each step with a gain error of less than 0.3 dB. The DC offset cancellation circuits can suppress the output DC offset voltage to be less than 1.5 mV, while the offset voltage of 40 mV is introduced into the input. The overall power consumption is less than 3.5 mA, and the die area is 800 × 300 μm^2.

Key words: automatic gain control; analog/digital reconfigurable; DC offset cancellation
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1. Introduction

Most of the previously reported RFICs are designed to cooperate with a certain companion digital baseband chip. This limits the portability of the radio chip, i.e., its ability to operate with different digital baseband chips, which have different requirements or certain desirable functionalities. Above all things, in multi-band multimode solutions, it is desirable that the choice of the digital baseband chip should be relatively independent of the AGC control mode. To achieve maximum compatibility toward a multitude of baseband chips, a flexible baseband interface and flexible AGC control mode are set as goals for this design, in addition to the obvious goals of good performance, low power, and low cost.

The zero-IF receiver has been used for almost all multi-band multimode wideband applications. Figure 1 shows a diagram of a multi-mode multiband zero-IF receiver system where the proposed AGC can be used.

The AGC, which outputs the signal with stable amplitude in order to reduce the requirements of the A/D converter behind, is a necessary block in the chain of the RF front-end chip. And the multi-mode reconfigurable AGC can amplify signals according to different accuracy requirements and the means of gain control in different systems with various base band chips.

Based on all of the above, an analog/digital reconfigurable automatic gain control with a novel DC offset cancellation is presented. Under analog control mode, the AGC can be applied in the more accurate requirements, where the control voltage is provided by the charge pump. Under digital control mode, the analog control unit is shut down to save power and the control voltage of the VGA is generated by the baseband chip.

2. System architecture

In order to decrease the extra hardware waste and system complexity, a novel reconfigurable method, shown in Fig. 2, is proposed by reusing the variable gain amplifier. In this architecture, the variable gain amplifier can be switched between the two kinds of control modes flexibly.

When the AGC is set under analog control mode, the baseband chip turns on the switch connecting to the charge pump, while the digital control feedback loop, which includes the DAC circuit, is shut down, and the control voltage of the VGA is generated from the output of the charge pump. The signal amplified by the variable gain amplifier is compared with the reference voltage, and then the charge pump adjusts the charge and discharge current until the amplitude of the output signal satisfies the set criterion. When the AGC is set under digital control mode, the baseband chip turns on the switch connecting to the DAC, while the analog feedback loop, which includes the charge pump and comparison circuit, is shut down. Now the gain control of the AGC circuit is provided by the baseband chip. The output signal of the baseband chip is then converted to an analog voltage by the DAC. The output of the DAC is used as the gain control signal.

3. Circuit design

The portion of the AGC circuits in Fig. 2, including the VGA with V–I conversion circuit, analog control circuit, digital control circuit and DC offset cancellation circuit, is designed based on the 0.18 μm CMOS process.

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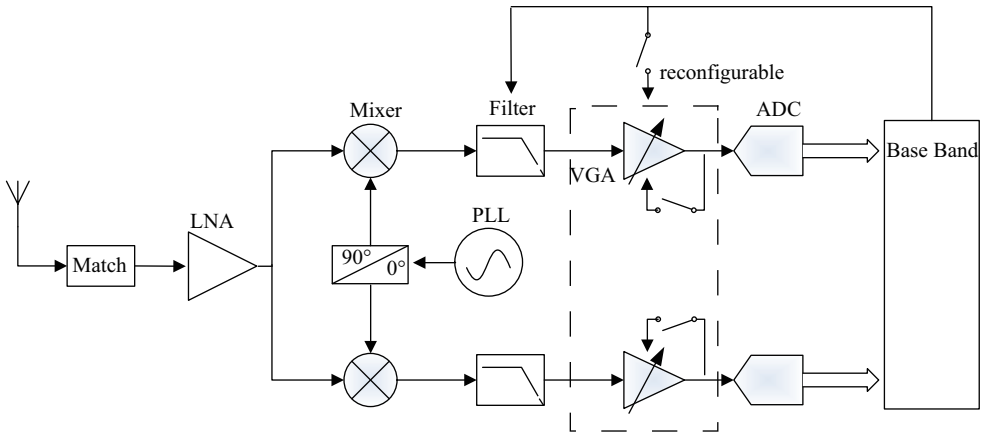

Fig. 1. Multi-band multimode zero-IF receiver.

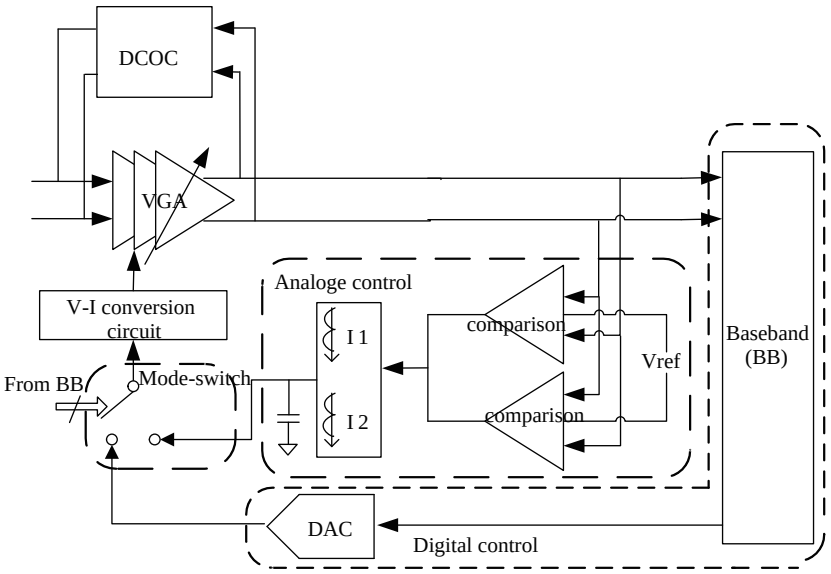

Fig. 2. Architecture of the proposed analog/digital reconfigurable AGC loop.

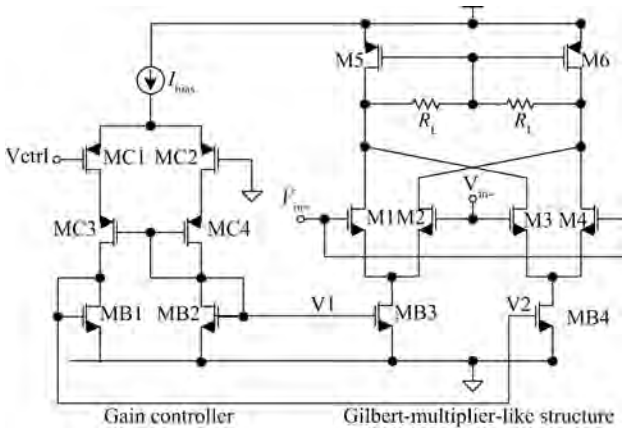

Fig. 3. Schematic of the VGA cell with V–I converter.

3.1. VGA with V–I conversion circuit

Figure 3 shows the fully differential VGA cell with a V–I converter, which is composed of a gain controller and a Gilbert cell. The gain of the Gilbert cell can be written as

$$\begin{aligned} A_{\mathrm{v}} &= \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{R_{\mathrm{on}}(I_1 + I_3 - I_2 - I_4)}{V_{\mathrm{in}}} \\ &= R_{\mathrm{on}}(g_{\mathrm{m1}} - g_{\mathrm{m3}} + g_{\mathrm{m2}} - g_{\mathrm{m4}}) \\ &= R_{\mathrm{on}}\sqrt{K_{\mathrm{n}}(W/L)_{1-4}}\left(\sqrt{I_{\mathrm{MB3}}} - \sqrt{I_{\mathrm{MB4}}}\right). \end{aligned} \quad (1)$$

The resistant R_{on} is the load of the VGA circuit. The current I_{bias} is the tail current of MB3 and MB4, imaging from MB1 and MB2, the tail current of the gain control circuit.

If the AGC loop settling time has to be input signal level independent, the gain of the VGA should have an exponential relationship with respect to the control voltage of the VGA[15]. From Ref. [11], we can conclude that this Gilbert cell can provide a characteristic, as follows,

$$A \infty \sqrt{I_{\mathrm{MB3}}} - \sqrt{I_{\mathrm{MB4}}} \approx \frac{i}{\sqrt{2I_{\mathrm{bias}}}}. \quad (2)$$

As a result, we can get the relationship between gain and the V_{c} as follows,

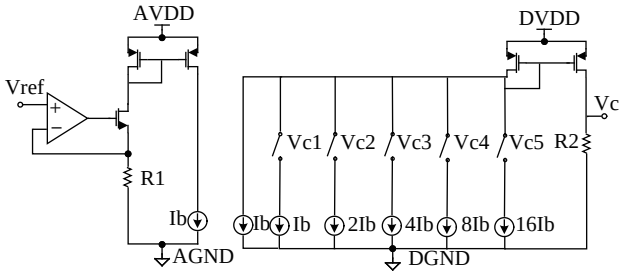

Fig. 4. Architecture of the DAC circuit.

$$A_{\mathrm{V}} \propto 2R_{\mathrm{on}}\sqrt{2K_{\mathrm{n}}\frac{W}{L}}\frac{k_1\exp(k_2V_{\mathrm{c}})}{\sqrt{I_{\mathrm{bias}}}}. \tag{3}$$

The relationship between the VGA gain and the control voltage shows the that VGA gain in decibels is linearly proportional to the control voltage.

3.2. Analog control circuit

In comparison with the traditional AGC[7], comparators and charge pump are adopted instead of a peak detector, which is limited by process and temperature variations, and a loop filter in an analog control AGC configuration. The VGA output signal is compared with the reference voltage and the charge pump adjusts the charge and discharge current to generate the control signal, which feeds back to control the gain of the VGA. The accuracy of the AGC is governed by the offset voltage of the comparator and the matching between the charge and discharge currents of the chare pump.

The comparator consists of three parts: the preamplifier, the positive feedback latched circuit and the output buffer. The preamplifier plays a key role in the comparator, which can reduce the input-referred offset and kickback noise of the clocked comparators. If the preamplifier has a high voltage gain, the offset voltage is dominated by the preamplifier, which can be given by[7]

$$V_{\mathrm{OS}} = \frac{V_{\mathrm{GS}}-V_{\mathrm{th}}}{2}\left[\frac{\Delta(W/L)}{W/L}+\frac{\Delta R_{\mathrm{D}}}{R_{\mathrm{D}}}\right]-\Delta V_{\mathrm{th}}, \tag{4}$$

where ΔW, ΔR_{D} and ΔV_{th} are technology mismatch parameters. The most direct way to reduce the offset voltage of the preamplifier is to increase the size of the device while maintaining the gain of the preamplifier and W/L unchanged[16].

The charge pump circuit is composed of a pair of symmetric pump circuits and a wide-swing current mirror circuit. To ensure more accurate charge pumping operation, a weak pull-up circuit is inserted in the symmetric pump circuit. The charge pump circuit has a wide output range and no jump phenomenon[17].

3.3. Digital control circuit

In the digital control mode, the control voltage of the variable-gain amplifier is provided by the output of DAC. The DAC circuit in Fig. 4 adopts a 5-bit current-mode DAC form, which ensures the value of the control voltage is independent of the power supply voltage and the process variation. The reference voltage of the DAC is generated from the bandgap circuit in the RF front-end circuit. The control voltage of the overall circuit can be written as

$$V_{\mathrm{c}} = V_{\mathrm{ref}}R_2/R_2(V_{\mathrm{c1}}+V_{\mathrm{c2}}\times 2+V_{\mathrm{c3}}\times 4+V_{\mathrm{c4}}\times 8+V_{\mathrm{c5}}\times 16). \tag{5}$$

The ratio between the resistor values R_1 and R_2 is process and temperature independent, and the baseband chip controls the V_{c1}–V_{c5} to vary from 00000 to 11111 when the control voltage is changed from 0.35 to 0.85 V.

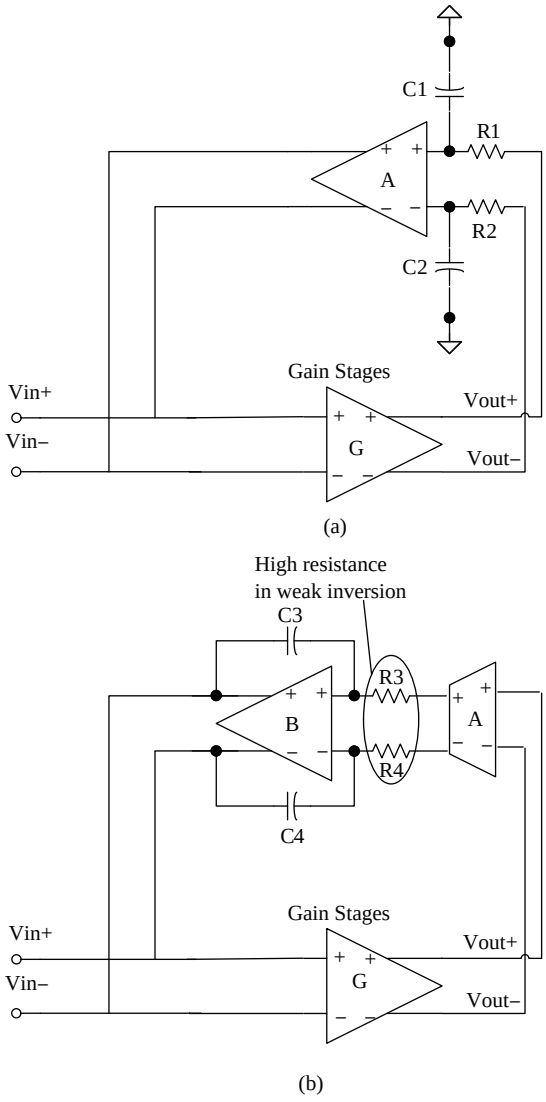

Fig. 5. Block diagram of the DC offset cancellation circuit. (a) Conventional cancellation circuit. (b) The proposed cancellation circuit.

3.4. DC offset cancellation circuit

The architecture of the DC offset cancellation circuit is shown in Fig. 5. The conventional one[11] consists of an integrator and a transconductance amplifier, with the disadvantage that large capacitances are needed to obtain a low enough HPCF (high pass cutoff frequency). In this work, a novel method is introduced to reduce capacitances.

DC offset voltage is extracted from the integrator, then amplified by a transconductance amplifier and finally subtracted from the input signal. The transfer function can be calculated as follows,

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{G(V_{\text{in}} - V_{\text{bak}})}{V_{\text{in}}} = \frac{1 + sRC}{1 + s\dfrac{RCB}{AG+1}}G, \tag{6}$$

where G is the gain of the VGA, A is the gain of the transconductance amplifier and B is the gain of the amplifier in the integrator. From the last equation, the HPCF can be written as

$$\omega_{\text{H}} = \frac{AG+1}{RCB}. \tag{7}$$

In Fig. 5(a), the cutoff frequency of the conventional DCOC circuit is $\frac{AG+1}{RC}$. Therefore, capacitances required in the proposed topology can be B times less compared with the conventional DCOC circuit，while suppressing the DC offset to the same level. Capacitances, however, which are B times less, are still too large to be integrated on the chip.

If a single loop cancellation is utilized, such a low cutoff frequency will demand large loop capacitors, and inevitably it will be implemented in off-chip components at the expense of extra package pins. Instead of utilizing a single-loop cancellation, multi-loop cancellation can effectively reduce the required loop capacitances. As the signal chain is uniformly divided into M segments in cascade and each segment has an independent servo-loop for DCOC, the gain of signal stage and the used capacitance in each loop can be expressed by $A^{1/M}$ and C_{p}/M, respectively, where A is the total gain of the signal chain and C_{p} is the total capacitance required in M loops. To maintain the same high-pass corner frequency in the single-loop and multi-loop implementations, the ratio of the total required loop capacitance in single-loop calibration to that in multi-loop can be approximated as

$$\frac{C_{\text{p}}}{C_{\text{l}}} = \frac{M}{A^{1-1/M}}, \tag{8}$$

where C_{l} is the total capacitance required in single-loop cancellation. From the equation above, less total capacitance is required in the multi-loop cancellation compared with a single loop implementation.

Considering that the required HPCF is below a few kHz, the DC offset cancellers in Fig. 5 still need a few nF capacitances, which will increase the chip size and the cost dramatically. To solve this problem, a few MΩ resistances can be implemented in Fig. 6, which reduces the value of capacitances largely. The resistances are realized by the MOSFETs working in the sub-threshold. Since the voltage of the input and output of the source follower is almost the same, the V_{gs} of MD in Fig. 6 is nearly the same as that of MR. To ensure MR operates in the sub-threshold region, MD is forced to operate in the same region. The resistance of MR is

$$R = \frac{\partial V_{\text{DS}}}{\partial I_{\text{DS}}} \approx N\frac{V_{\text{T}}}{I_{\text{bias}}}\frac{L}{W}V_{\text{T}}\exp\left(\frac{nV_{\text{T}}}{V_{\text{GS}}} + \frac{V_{\text{T}}}{V_{\text{DS}}}\right). \tag{9}$$

To solve the PVT problem, the temperature and process independent current is introduced to reduce the change in the MOS channel resistance value.

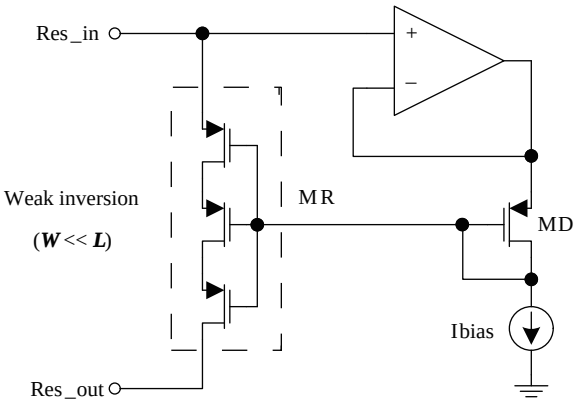

Fig. 6. Architecture of the proposed sub-threshold resistor.

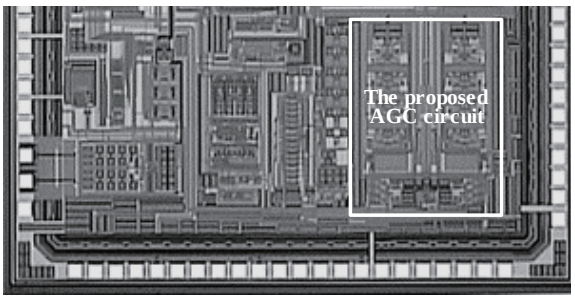

Fig. 7. Die micrograph.

4. Measurement results

The analog/digital reconfigurable AGC circuit is fabricated in the 0.18 μm single-poly six-metal CMOS process. Figure 7 shows the micrograph of the fabricated chip. For testing purposes, a buffer is added to the output of the AGC block to ensure that the external loading capacitance will not affect the AGC block.

The total current consumption of the AGC is 3.46 mA when the AGC is powered up in a 1.8 V power supply. Therefore, the total power consumption is only 6.23 mW.

4.1. Function of AGC

The AGC is configured in analog control mode and the output amplitude stabilizes automatically. The output single-end amplitude shown in Fig. 8 is about 436 mV, which matches the simulation result closely.

4.2. Dynamic range

When the AGC is configured in analog control mode, the gain of the VGA varies with the control voltage. Figure 9 shows the dynamic range of the AGC block. The measured curve is quite close to the simulated one. Its gain changes from 10 to 80 dB when the control voltage changes from 0.05 to 0.9 V.

When the AGC is configured in digital control mode, the gain of the VGA varies with the digital control word. In Fig. 10, the output differential amplitude changes with the input signal by 2 dB, every step corresponding to the digital control word changing from 0 to 31, and the gain error is less than 0.3 dB.

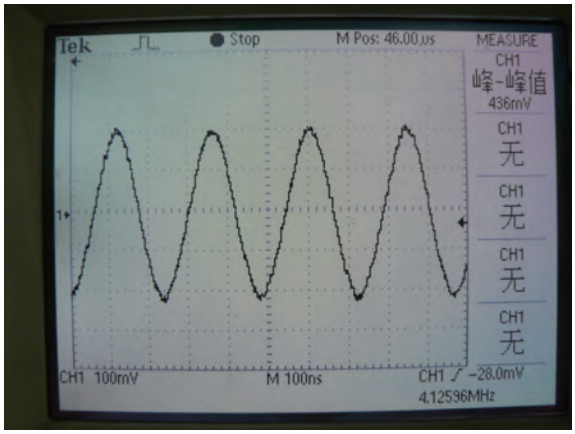

Fig. 8. Output of the analog control AGC.

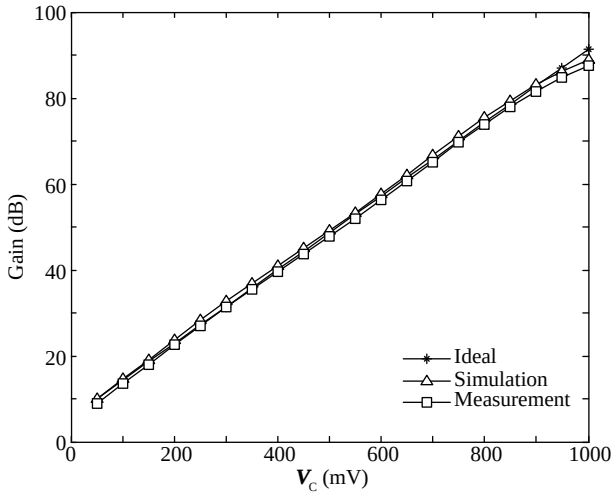

Fig. 9. Measured dynamic range of AGC in analog control.

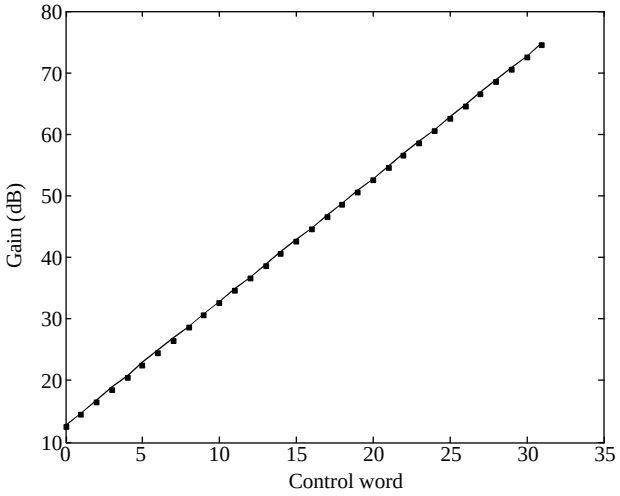

Fig. 10. Measured dynamic range of AGC in digital control.

4.3. Frequency response

The AC response of the VGA is measured and shown in Fig. 11 and the band-pass characteristic is evident. The curves from top to bottom correspond, respectively, to the control voltage from high to low: the top curve for V_c = 1 V and the bottom curve for V_c = 0.26 V. The high pass cutoff frequency is 10 kHz and the –3 dB bandwidth is 60 MHz for all values of V_c (or all levels of gain).

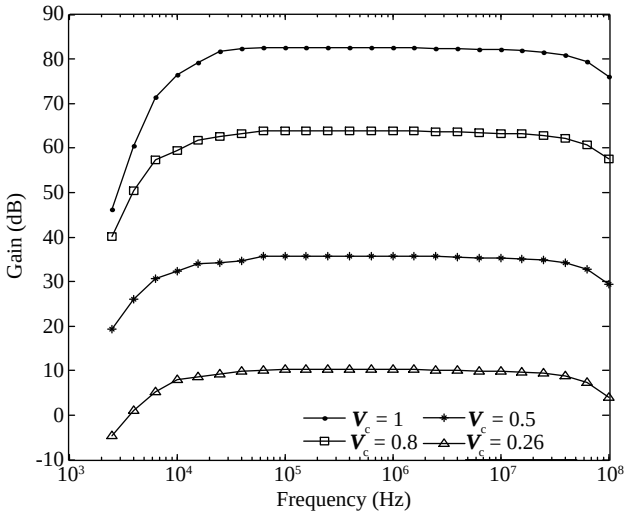

Fig. 11. Frequency response of the VGA under different control voltages.

Table 1. Overall performance of the proposed AGC.

Parameter	Specification
Technology	0.18 μm
Die area	0.24 mm^2
Supply voltage	1.8 V
Current consumption	3.5 mA
3 dB bandwidth	[10 kHz, 60 MHz]
Gain tuning range	70 dB (analog control)
	65 dB (digital control)

4.4. DC offset cancellation effect

The measured result of DC offset cancellation is shown in Fig. 12. A DC offset is intentionally added at the input of the AGC, and the dc voltage is measured at the output. For each control voltage, the input DC offset is increased from 0 to 40 mV and the final output DC offset versus the input DC offset is shown in Fig. 12. It is shown that the DC offset cancellation loops keep the DC offset output of the VGA less than 1.5 mV, irrespective of the control voltage.

The overall AGC performance is summarized in Table 1.

A comparison of the proposed AGC with designs published in the past is given in Table 2. As shown in Table 2, the proposed AGC can be configured in either analog or digital control mode through the reconfigurable mode-switch circuit while reusing the variable gain amplifier. This hardware reuse reduces the power consumption and area to a large extent. Moreover, the proposed AGC exhibits superior results compared with one mode AGC ICs and the proposed DC offset cancellation circuit has a competitive HPCF and DC attenuation compared with other designs.

Table 2. Performance comparison of the proposed and previously reported AGCs.

Reference	Ref. [11]	Ref. [7]	Ref. [1]	Ref. [3]	Ref. [5]	This work
Process (μm)	CMOS 0.35	CMOS 0.18	CMOS 0.35	CMOS 0.35	CMOS 0.35	CMOS 0.18
Gain control	Analogue	Analogue	Analogue	Digital	Digital	Analog/digital reconfigurable
Bandwidth (Hz)	[230k, 20M]	[600k, 16M]	[67k, 2.5M]	[*, 95M]	[2.25k, 17.1M]	[10k, 60M]
Gain error	*	*	*	0.3	1	0.3
Power (mW)	7	11.2	16.3	32.7	7.9	6.3
max gain (dB)	50	32	60	40	30	80
Dynamic range (dB)	40	40	60	70	52	70 (analog control) 65 (digital control)
DC attenuation (dB)	*	*	50	*	25	30
Die area (mm^2)	0.289	0.5625	*	0.28	0.22	0.24

(*) not found.

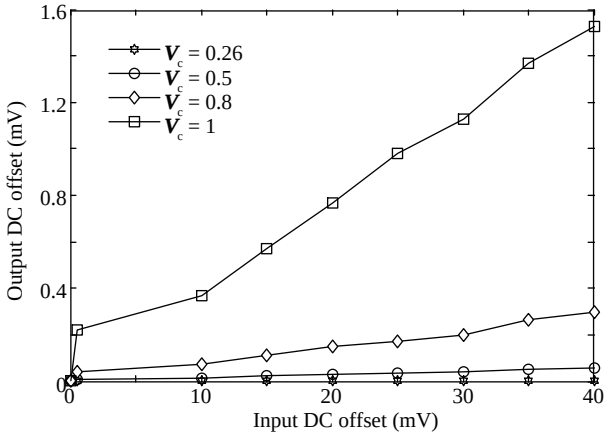

Fig. 12. Performance of the DC offset cancellation circuit.

5. Conclusions

This paper has proposed an analog/digital reconfigurable automatic gain control with a novel DC offset cancellation circuit. The stable output amplitude of the AGC is 430 mV and the maximum gain is about 80 dB, with a dynamic range of 70 dB and a bandwidth greater than 60 MHz under the analog control loop. The AGC in digital control mode provides a 64 dB gain control range by 2 dB every step with a gain error less than 0.3 dB while operating at 60 MHz. The novel DC-offset compensation circuitry suppresses the DC offset voltage to less than 1.5 mV with the input offset voltage of 40 mV, which is more effective at suppressing the DC offset voltage compared with a conventional feedback circuit.

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