Avalanche behavior of power MOSFETs under different temperature conditions

Lu Jiang(陆江), Wang Lixin(王立新), Lu Shuojin(卢烁今), Wang Xuesheng(王雪生), and Han Zhengsheng(韩郑生)†

Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

Abstract: The ability of high-voltage power MOSFETs to withstand avalanche events under different temperature conditions are studied by experiment and two-dimensional device simulation. The experiment is performed to investigate dynamic avalanche failure behavior of the domestic power MOSFETs which can occur at the rated maximum operation temperature range (–55 to 150 ℃). An advanced ISE TCAD two-dimensional mixed mode simulator with thermodynamic non-isothermal model is used to analyze the avalanche failure mechanism. The unclamped inductive switching measurement and simulation results show that the parasitic components and thermal effect inside the device will lead to the deterioration of the avalanche reliability of power MOSFETs with increasing temperature. The main failure mechanism is related to the parasitic bipolar transistor activity during the occurrence of the avalanche behavior.

Key words: UIS test; device simulation; electrothermal; parasitic bipolar transistor; power MOSFETs
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1. Introduction

In recent years, to save energy and reduce greenhouse gas emissions has become an important direction in the information technology area. This leads to high demands on energy-efficiency and a more reliable power electronics device. The power MOSFETs have been widely used in industrial and automotive electronics system applications such as DC–DC power supplies, AC–DC adapters, automobile diesel injection engine management and automobile ABS system because of their high input impedance, low on-resistance, great ruggedness, and fast switching speed[1]. Generally, most of these devices as switch power supply application are used to drive unclamped inductive loads. It is required that the device during the off-state is able to dissipate all of the energy stored in the inductor loads during the on-state. Because most of power MOSFETs are the key components in such power supplies systems, they must have high avalanche ruggedness and be able to withstand all possible extreme temperature conditions that can occur during their lifetime, especially in automobile application. Thus, it is important to investigate the avalanche failure mechanism of the power MOSFETs and how avalanche behavior affects the device reliability at a wide range of temperature. The unclamped inductive switching (UIS) test is a routine method to determine the reliability of power MOSFETs when the avalanche happens. Lots of efforts have been made to investigate the avalanche behavior of the power MOSFETs under UIS stress. Many researchers have attempted to explain the avalanche events of the low-voltage or trench power MOSFETs by experiment and numerical simulation[2−6]. Some have specifically focused on better understanding of the device ruggedness under repetitive avalanche stress[7, 8]. However, very little experimental data is available concerning the avalanche ability of the power MOSFETs at the rated maximum temperature range (–55 to 150 ℃). In this paper, we investigate the avalanche behavior of the domestic power MOSFETs from low temperature (–55 ℃) to high temperature (150 ℃). Then an advanced two-dimensional (2D) mixed mode device and circuit simulator is used to analyze the inner avalanche failure mechanism of the power MOSFETs. In order to study the self-heat effect and parasitic component effect in the device during UIS test, the thermodynamic model with the non-isothermal equation is incorporated into the device simulation.

2. Experimental setup and results

The device under test (DUT) was manufactured by using a planar stripe-cell design and integrating millions of single cells in parallel on a chip. All sample devices developed by the Institute of Microelectronics, CAS[9] were selected from the same wafer and manufactured by the same package type. Figure 1 shows the cross-section of one cell of an N-channel vertical DMOSFET structure and its equivalent circuit. From the diffused structure of the power MOSFETs, we can know the inherent parasitic bipolar transistor inside the device. Here the n^+ source acts as the emitter, p-well as the base and the epitaxial layer as the collector. When this parasitic bipolar transistor turns on under certain circumstances, it will lead to a detrimental effect.

To evaluate the power MOSFETs avalanche energy handling ability under extreme temperatures conditions, the Tesec 3702-LV avalanche inductance load tester is used to measure the max avalanche voltage and current. The Votsch VTM 7004 Temperature Test Chamber is used to produce different temperature atmosphere during the UIS test. Figure 2(a) shows the structure of the UIS test circuit used for the experiment. It consists of a voltage source V_{dd}, a pulse voltage generator, a load inductance L, a temperature test chamber and the DUT. Before the UIS test, the static characteristic of the sample devices are tested by the Tesec-3630tt discrete tester. During the UIS test,

† Corresponding author. Email: zshan@ime.ac.cn
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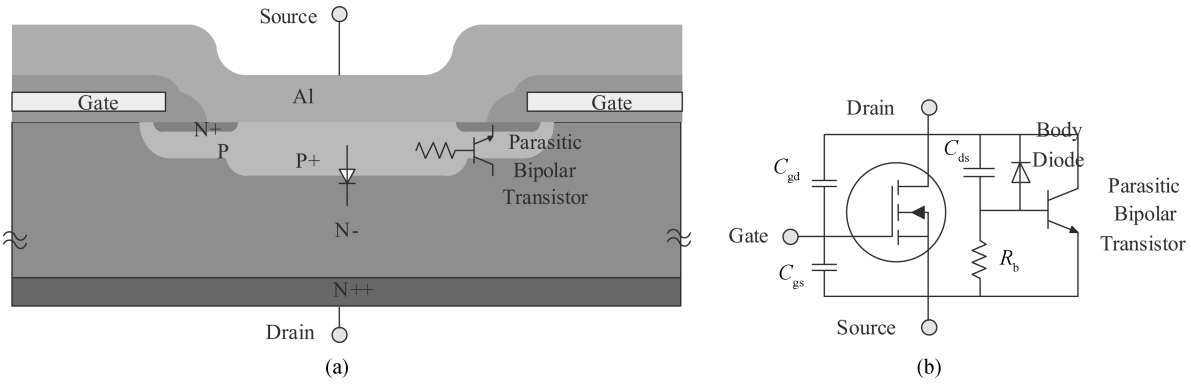

Fig. 1. (a) Cross-sectional view of the power MOSFETs structure (not drawn to scale). (b) Equivalent circuit.

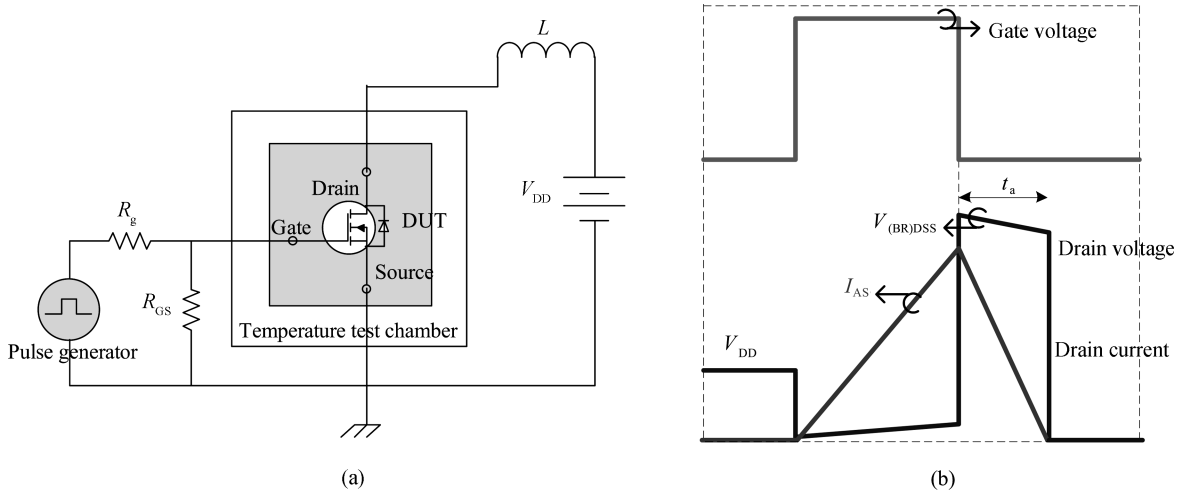

Fig. 2. (a) UIS test circuit and (b) current and voltage waveforms of the DUT under UIS test.

the DUT is switched on by the pulse voltage generator and the current continues to flow through the inductance L to achieve the required drain current. Once the desired current level is reached, the DUT is switched off immediately. Meanwhile, the drain voltage rises up until it reaches the rated breakdown voltage and the device will enter the avalanche breakdown mode. The energy which stored in the inductance is dissipated on the DUT during the time t_a. The period t_a in the Fig. 2(b) is defined as the avalanche time and it is given by

$$t_a = \frac{LI_{AS}}{V_a} = \frac{LI_{AS}}{V_{(BR)DSS} - V_{DD}}, \quad (1)$$

where I_{AS} is the peak avalanche current after the gate is turned off and $V_{(BR)DSS}$ is the avalanche mode breakdown voltage. It can be seen from Fig. 2(b) that the total energy which released on the device during the avalanche time can be calculated by

$$E_{AS} = P_d t = \frac{1}{2} I_{AS} V_{(BR)DSS} t_a. \quad (2)$$

Thus, the avalanche energy during the avalanche mode can be obtained by inserting Eq. (1) into Eq. (2):

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}} \quad (3)$$

The UIS measurement test conditions are defined by V_{DD} = 25 V, L = 10 mH, V_G =12 V and R_{GS} = 25 Ω. To evaluate the influence of the temperature variation on the device, twenty sample devices are divided to five groups of –55, –25, 25, 75, 125 and 150 ℃, respectively. During the UIS test procedure, we fix the load inductance value and then increase the drain current by every 0.5 A per step until the DUT is destruction. Failure results are detected that the DUT is in "Post-Short" status by using the Tesec 3702-LV avalanche inductance

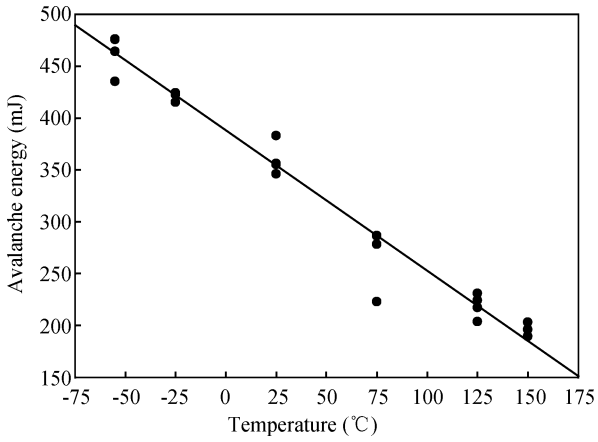

Fig. 3. Avalanche energy during UIS test failure occurs as a function of the temperature of the sample devices. In the plot the temperature increases from –55 to 150 ℃.

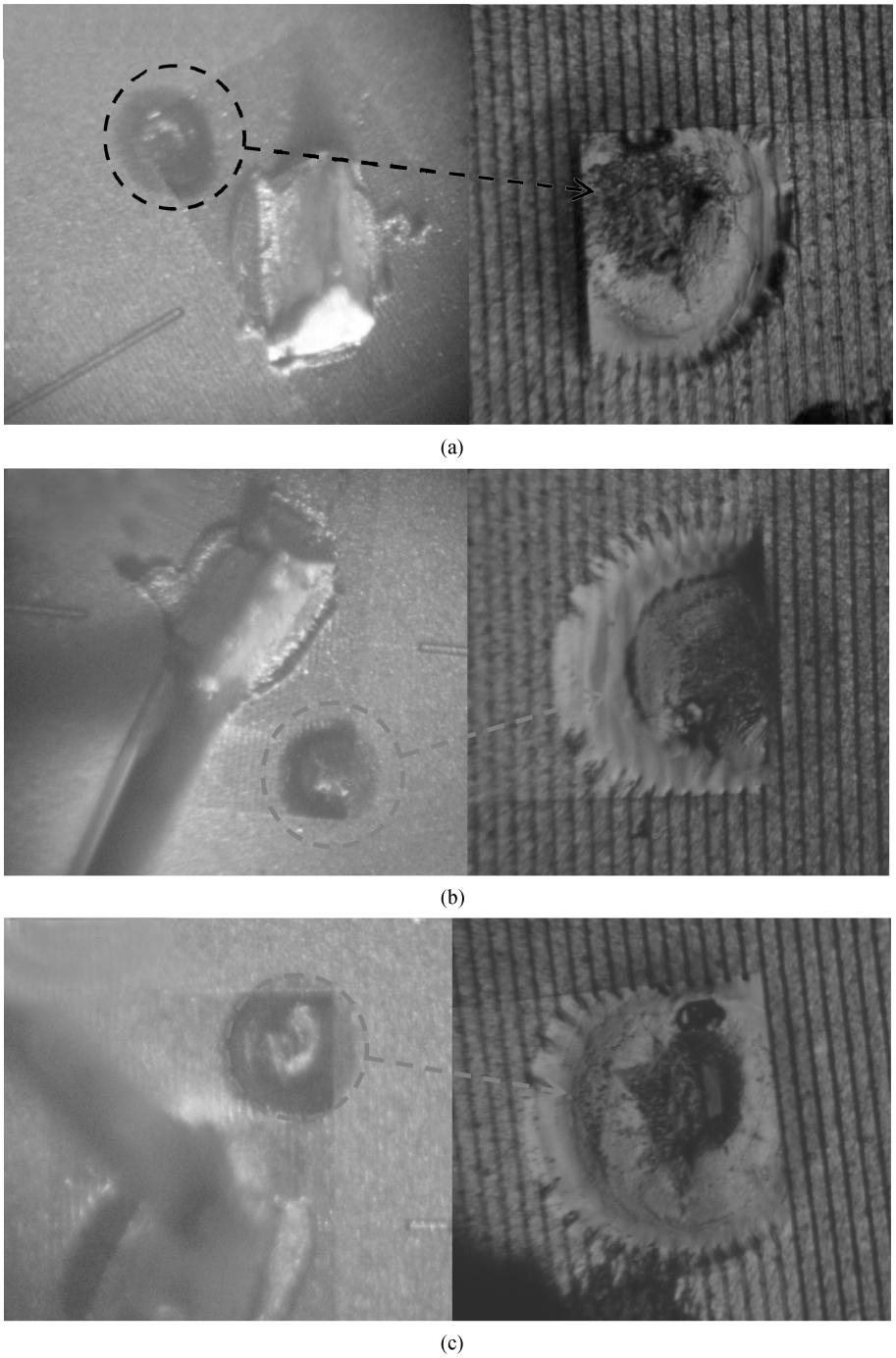

Fig. 4. Light microscopic image of the failure sample power MOSFETs at three different temperatures. Circles indicate the magnified image of the avalanche failure spot. (a) At low temperature (–55 ℃). (b) At room temperature (25 ℃). (c) At high temperature (150 ℃).

load tester. The "Post-Short" means that even if the gate voltage is off after UIS test, the drain current is still high, that is to say, the device is already punched through and cannot be controlled by the gate voltage. At each temperature condition, the burned avalanche energy is calculated by using Eq. (3). Figure 3 provides the scatter plot of the burned energy with the temperature varying from –55 to 150 ℃. Results show that the device maximum avalanche energy value decreases quasi linearly with increasing temperature. Figure 4 shows the microscopic graph of the decapsulation device after avalanche failure at 25, –55 and 150 ℃ respectively. It can be seen that the excess avalanche energy on the DUT will cause catastrophic destruction. The noticeable damage is observed on the die surface (discoloration and metal melted regions) by the light microscope.

3. Numerical simulations results and discussions

The advanced 2D mix-mode simulator ISE TCAD is used to investigate the device's inner dynamic behavior during the UIS test. Initially, the TCAD process simulation tool DIOS is used to generate the sample power MOSFETs device structure. Due to the massive requirement of the CPU simulation time and memory during electrothermal simulation, the device

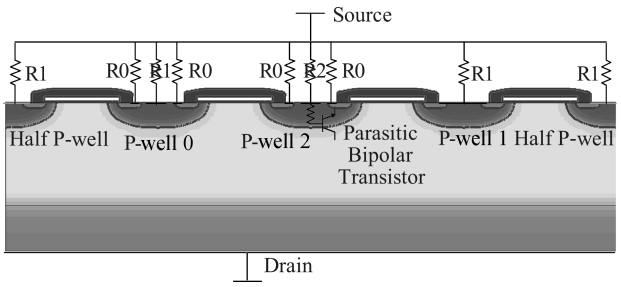

Fig. 5. Simulation set up of source contact.

structure is proposed with reducing area factor compared to the actual die size. Then the MDRAW tool is used to generate optimized grid size manually. Finally the mixed device and circuit simulator DESSIS is used to simulate the dynamic avalanche behavior of the device which based on the UIS test structure in Fig. 2 (a). During the occurrence of avalanche, the self-heat phenomenon will cause the lattice temperature continuously increasing because of the presence of high current and high-voltage. Therefore, the basic semiconductor equations (Poisson and current continuity equations) and the thermodynamic model with non-isothermal equation are used to evaluate the electrothermal effects of the device. Considering the wide temperature range requirement for the electron-hole pair avalanche generation simulation, the University of Bologna Impact Ionization Model is used to analyze the device's inner electrothermal behavior. It covers a wide range of electric fields (50 kV/cm to 600 kV/cm) and temperatures (26.85 to 426.85 ℃)[10].

Generally, the N^+ source (parasitic bipolar transistor emitter) and the P-well (parasitic bipolar transistor base) is shorted by the source metal to suppress the parasitic bipolar transistor operation. Due to the simulation purpose, some source contacts are defined by splitting the source contact into separate connections with different resistances in Fig. 5, where the resistance value $R_2 > R_1 > R_0$. The contact to the P-well (parasitic bipolar transistor base) is set as the source_p and the contact to the N^+ source (parasitic bipolar transistor emitter) is set as the source_n. In this way, it will help to solve the simulation convergence problem. Meanwhile, the source contact with the different series resistance can help us to investigate the deteriorative trend of "weak" cell in device.

In order to achieve better comparison results and save the simulation time simultaneously, the same avalanche energy applies to the simulation structure by fixing the inductance load value and pulse generation time. The only difference is the thermal boundary conditions, which are set at 26.85 and 151.85 ℃, respectively. It aims to compare the device's inner electrothermal behavior at different temperature conditions. The simulation results of various inner physical parameters distribution are shown in Fig. 6. The total current flow distributions in the multi-cell structure are shown in Fig. 6(a). The result presents in the left panel that the current flow triggered by avalanche multiplication effect is located in the inner parasitic diode structure of the device at room temperature 26.85 ℃. Therefore, the parasitic bipolar transistor is in off state. That means this avalanche energy in the device cannot trigger the turning on of the parasitic bipolar transistor at this temperature. However, the right panel in Fig. 6(a) shows that the same avalanche energy which dissipates on the device can lead to the parasitic bipolar transistor to be activated and the hot spot is located in the current flow path "A" at P-well 2. Comparing the two temperature simulation results with the same avalanche energy in Fig. 6(a), it is clear that the parasitic bipolar transistor is activated at high temperature condition. That means the handling avalanche energy ability of the device will deteriorate with increasing temperature. In fact, the parasitic bipolar transistor will also be activated at room temperature or low temperature conditions, once the avalanche energy is enough by increasing inductance value or pulse time. Figures 6(b) and 6(c) show the corresponding inner lattice temperature distribution and the inner power density distribution. From the left panel in Fig. 6(b), the hot spot equally distributes in the each P-well structure and the maximum lattice temperature only rises to about 97 ℃. In contrast, the temperature mapping illustrated in the right panel of Fig. 6(b) shows that the hot spot "A" within the device reaches a highest temperature close to 308.85 ℃. Because the parasitic bipolar transistor is in on state, the lattice temperature will increase sharply. This temperature already exceeds two times of the maxim operation junction temperature and it will cause permanent destroy in the device. According to the source contact connect in Fig. 5, the source series resistor of P-well 2 is larger than other P-well series resistor. If the voltage drop across the base resistor is sufficiently high to forward bias the parasitic bipolar transistor's base-emitter, it will turn on subsequently. The result indicates that the bad source contact with large contact resistor which might be induced by manufacturing process or fabrication will trigger the turning on of the parasitic bipolar transistor more easily. When the device enters these conditions, current density and voltage are both in the high level locally.

Due to the simultaneous large current and voltage when the parasitic bipolar transistor is activated, the considerable power dissipation (P_D) occurs within the DUT according to the following equation:

$$P_D = I_C V_{CE} = \frac{T_J - T_A}{R_{\theta JC}}, \tag{4}$$

where T_J is the maximum permissible junction temperature, $R_{\theta JC}$ is the thermal resistance and T_A is the ambient temperature. The current density within the bipolar is given by[11]:

$$I_C = \frac{A_E q D_n n_i^2}{W N_B} \exp\left(q\frac{V_{BE}}{kT}\right), \tag{5}$$

where A_E is the area of the emitter, D_n is the diffusion coefficient for electrons, n_i is the intrinsic carrier concentration, W is the base width and N_B is the base doping concentration. If the collector current density increases in a local region, the power dissipation in this region also becomes larger. Inserting Eq. (5) into Eq. (4) gives the relationship of local temperature T_J:

$$T_J = I_C V_{CE} R_{\theta JC} + T_A = \frac{A_E q D_n n_i^2}{W N_B} e^{q\frac{V_{BE}}{kT}} V_{CE} R_{\theta JC} + T_A. \tag{6}$$

The intrinsic carrier concentration in Eq. (6) strongly depends on the temperature by[11]:

$$n_i = 3.87 \times 10^{16} T^{3/2} \exp\left(-\frac{7.02 \times 10^3}{T}\right) \quad (\mathrm{cm}^{-3}). \tag{7}$$

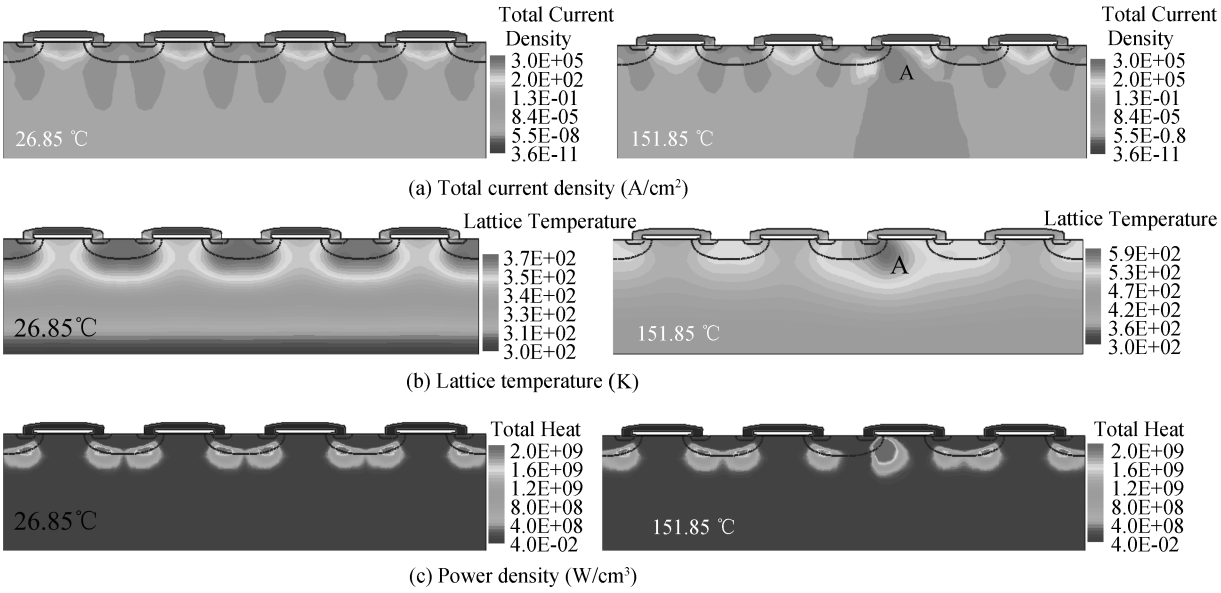

Fig. 6. 2D physical parameter distribution simulation results of the UIS test at room temperature (26.85 ℃, left panel) and high temperature (151.85 ℃, right panel), respectively. (a) Total current flow distribution. (b) Maxim lattice temperature distribution. (c) Power density distribution.

Equation (6) shows as the collector current density increasing, the local temperature in this region increases simultaneously. This positive feedback mechanism will lead to the concentration of the total current on a few source areas where the formation of a current filament occurs and cause the catastrophic device failure. This demonstrates that the device sustaining the avalanche energy ability will severely deteriorate with rising temperature when the parasitic bipolar transistor is activated, which is in good agreement with the experiment result in Fig. 3. We can conclude that the parasitic bipolar transistor action will influence the power MOSFETs avalanche reliability and how to suppress it becomes a major concern in the device structure design and application.

In general, the switch on of the parasitic bipolar transistor is related to the fabrication defects, current density, junction temperature and the quality of the source metal contact. Some design considerations have been used to optimize the device structure. Historically, the device avalanche performance is improved by increasing the P-well doping concentration with high doping P^+ region and optimizing the P-well cell layout. It will help to reduce the parasitic bipolar transistor base resistance and suppress the parasitic bipolar transistor operation. Another way is to reduce the N^+ source doping concentration, which reduces the parasitic bipolar transistor injection efficiency (hence, reduces the parasitic bipolar transistor gain). However, there is a dilemma in our design consideration. When optimizing the device's avalanche capability, we need to be careful not to sacrifice the device's electrical performance. For example, the increment of the P-well doping concentration will affect the device threshold voltage. And when the source doping concentration decreased, it will increase the source contact resistance and may influence the overall on-resistance of the device. On the other hand, there are also some countermeasures to suppress the parasitic bipolar transistor action in practical application [1]. For instance, the large current path wiring is adjusted as short and thick as possible to reduce the series inductance. A gate series resistance R_g or a zener diode is inserted in application circuit to reduce the surge voltage when the device is off. Ultimately, achieving the best avalanche performance and suitable electrical performance requires better device structure optimization, proper manufacture process selection and appropriate application design.

4. Conclusion

In this work, the UIS experiment was used to investigate the avalanche behavior of domestic power MOSFETs at the rated maximum temperature conditions. The goal of this research was to examine how temperature influences the power MOSFETs avalanche ability. The UIS test results provided convincing evidence that the handling avalanche energy ability of the power MOSFETs will severely deteriorate with the increasing ambient temperature. The main reason of the device failure mechanism is that the parasitic bipolar transistor action triggers the high voltage and high current density in the inner the device simultaneously. This positive feedback mechanism will lead to the lattice temperature increasing sharply. Advanced numerical 2D simulation was used to analyze the device inner behavior and the simulation result was in good agreement with the experimental data. Some optimizing ways to suppress the parasitic bipolar transistor effect were presented. It will help to enhance the device sustain avalanche capability through the device structure design and manufacturing process adjustment.

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