A current-steering self-calibration 14-bit 100-MSPs DAC*

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Abstract: This paper presents the design and implementation of a 14-bit, 100 MS/s CMOS digital-to-analog converter (DAC). Analog background self-calibration based on the concept of analog current trimming is introduced. A constant clock load switch driver, a calibration period randomization circuit and a return-to-zero output stage have been adopted to improve the dynamic performance. The chip has been manufactured in a SMIC 0.13-μm process and occupies 1.33 $\times$ 0.97 mm^2 of the core area. The current consumption is 50 mA under 1.2/3.3 V dual power supplies for digital and analog, respectively. The measured differential and integral nonlinearity is 3.1 LSB and 4.3 LSB, respectively. The SFDR is 72.8 dB at a 1 MHz signal and a 100 MHz sampling frequency.

Key words: DAC; high speed; high resolution; self-calibration; calibration period randomization
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1. Introduction

Digital-to-analog converters (DACs) with hundreds of MHz sampling rate and a resolution higher than 10-bit[1−4] are always required in wireless communication systems, and current-steering DAC is the best choice for such DACs owing to its intrinsic high speed. Various techniques have been used to ensure the static and dynamic performances of high-speed high-resolution DAC, mainly including foreground and background calibration. Compared to foreground calibration, background calibration can remove not only the mismatch errors of the current-sources caused by chip manufacture but also the time-varying errors, such as on-die temperature-dependent offset and slowly bias condition changes.

The DAC of this design adopts a background self-calibration strategy, which is based on the concept of analog current trimming. In order to improve the dynamic performance, design considerations such as a constant clock load switch driver, a calibration period randomization circuit and a return-to-zero output stage have been investigated. When operating at a 100-MHz clock rate and 1-MHz output sinusoid signal, the measured SFDR improves from 55.75 to 72.81 dB when calibration is turned on.

2. DAC architecture

The basic architecture of this design is depicted in Fig. 1. The DAC is segmented into a 5 thermometer coded most significant bits (5 MSB), 4 thermometer coded upper least significant bits (4 ULSB) and 5 binary coded lower least significant bits (5 LLSB).

The current of MSB current-sources will be calibrated, while the current of the sources in the 9-bit LSB array comprising the ULSB and LLSB arrays is not trimmed since it needs only to maintain 9-bit accuracy, which is practically achievable to an acceptable yield without calibration. 32 unary current-sources (31 MSB current-sources and one for generating 16 ULSB current by accurate current splitting) are connected to the calibration circuit in turn.

3. Circuit implementation

3.1. Calibration circuit

Generally speaking, intrinsic accuracy can ensure static performance of DACs by enlarging the dimension of the current-sources, while the entailed large parasitic capacitances will deteriorate the dynamic performance. Therefore, calibration techniques are widely used to realize high-speed and high-resolution DACs.

The schematic of the background self-calibration block, including MSB current-sources and calibration loop, is shown in Fig. 2. To fulfill the background scheme, floating current-source[1] (composed of M1–M4), which can be calibrated and kept in operation at the same time, is adopted in the MSB array. The current through M2 accounts for 90% of the MSB current (500 μA), and the current through M3 is about 50 μA, which can be modified by adjusting the voltage at node B. M7 and

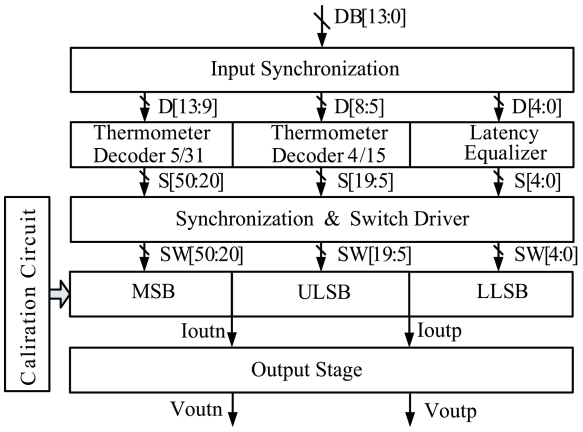

Fig. 1. Block diagram of the DAC.

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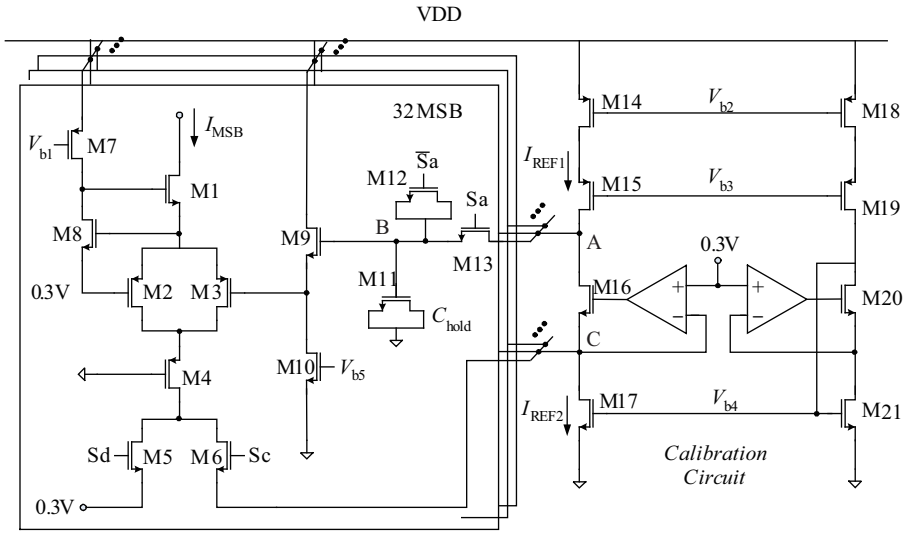

Fig. 2. Schematic of the background self-calibration block.

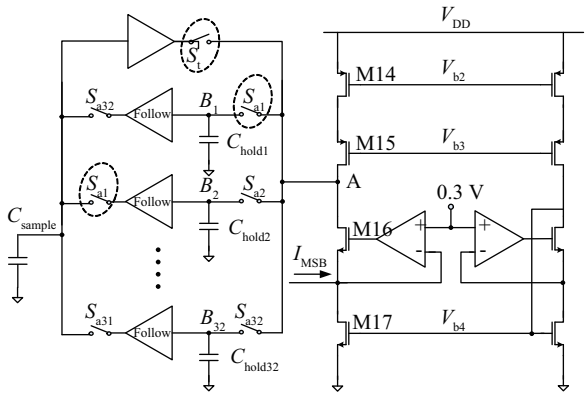

Fig. 3. Glitch reduction circuit.

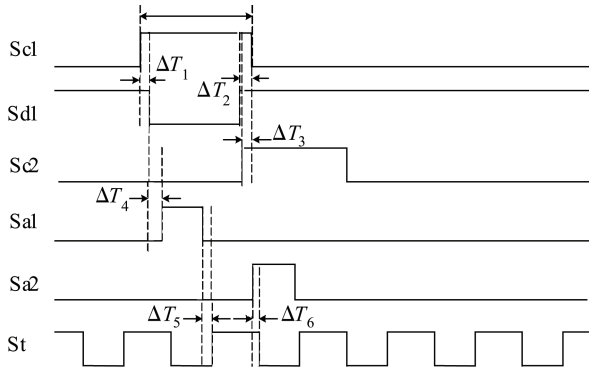

Fig. 4. Timing of calibration control signals.

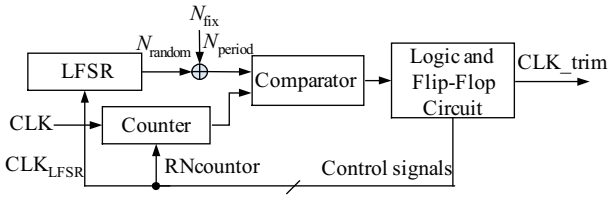

Fig. 5. Block diagram of randomized clock generator.

M8 form a gain-boosted structure to further increase the output impedance.

When the current-source is connected to the calibration circuit, its current is compared with $I_{REF2} - I_{REF1}$. If $I_{MSB} < I_{REF2} - I_{REF1}$, there must be a current from nodes B to A to meet Kirchhoff current law. Thus, the MOS capacitor M11 is discharged and the current of M3 will increase until I_{MSB} is equal to $I_{REF2} - I_{REF1}$. And in order to limit the fluctuation of I_{REF2}, which influences I_{MSB} directly, an OTA with 40 dB DC gain is added here to clamp the drain voltage of M17.

Since node A in Fig. 1 has a high impedance, and its voltage is uncertain when switch M13 is off (Sa is low), the voltage at node B can be quite different from that at node A and glitches will be generated whenever the calibration loop is connected. Thus, a circuit shown in Fig. 3 is used to reduce these glitches. Timing of the calibration control signals is shown in Fig. 4. Assuming Sa1 is high, the voltage at node B of the next MSB to be trimmed (voltage at B2) is sampled and held on the capacitor (C_{sample}). And this voltage transfers to node A through the voltage buffer when St turns to high. Hence, when node B2 is connected to the calibration loop (Sa2 goes high), the voltage there is almost the same as that at node A.

Although a glitch reduction circuit is adopted, spurious tones still exist in the output signal at multiples of the refresh frequency because the MSB currents are compared with the reference current sequentially. So, a random clock generator is utilized here to randomize the refresh period so that discrete calibration spurs can be converted into wideband noise[3]. Its block diagram is shown in Fig. 5. Considering that the longest calibration period cannot exceed 320 μs in order to keep the error caused by leakage on C_{hold} shown in Fig. 2 less than 0.5 LSB, the period-randomization circuit is implemented to generate a randomized clock (CLK_trim) changing from 2.5 to 5 μs with a minimum step of 20 ns when the input clock (CLK) is 100 MHz. In consequence, the calibration period varies from 80 to 160 μs and the minimum variable step is 640 ns.

3.2. Switch driving circuit

Non-synchronization of the switch-control signals is one of

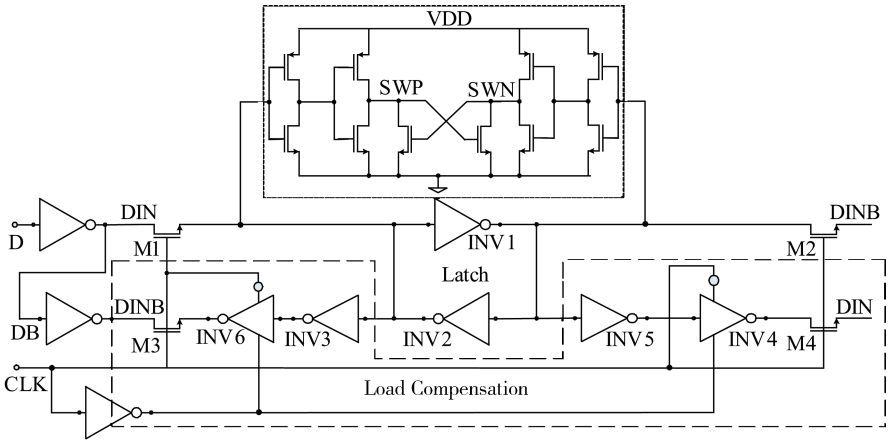

Fig. 6. Constant clock load switch driver.

the key elements that affect the dynamic performance. It will cause time-shift of the output samples, which result in data-dependent interference. A special case for this comes from the varying load of the final retiming clock. As we know, for different combinations between the state of the latch and the input (the drain and source voltage level of M1 and M2), the effective loads to the clock are not the same. While the switching number of current-sources is proportional to the slope of the output signal, which indicates that the arriving time of the switch signals is related to the output absolute value. To solve this problem, a constant clock latch[4] is adopted here to provide a constant load for the clock. The part in the dashed box of Fig. 6 provides a compensation load through transistors M3/M4. It has an opposite state to M1/M2 when the clock is low. This ensures a constant load, which is invariant with the data pattern for the clock. The circuit depicted upon the latch (in the dotted box) is used to generate complementary switch signals (SWP and SWN) with low-cross voltage, which can avoid the simultaneously turned-off of PMOS switches.

3.3. Design of current-sources

Thanks to the calibration scheme, the strict stress on the intrinsic accuracy of MSB cells is released. The design of MSB current-sources only needs to ensure that the maximum error is not beyond the calibration range. While the ULSB & LLSB have to maintain a 9-bit resolution with a certain INL and DNL yield, it is the key point in the current-source design.

When k switches of the 16 ULSB are turned on, the standard deviation of INL is $\sigma^2_{\mathrm{u,k}} = \frac{k(16-k)}{16}\sigma^2_{\mathrm{u}}$[7], and σ_{u} is the standard deviation of ULSB current-source. The INL yield can be expressed as[8]

$$G = \prod_{\mathrm{k}=1}^{16} \int_{k\bar{I}-0.5I_{\mathrm{ULSB}}}^{k\bar{I}+0.5I_{\mathrm{ULSB}}} \frac{1}{\sqrt{2\pi}\sigma_{\mathrm{u,k}}} \exp\left(-\frac{(z-u)^2}{2\sigma^2_{\mathrm{u,k}}}\right)\mathrm{d}z, \quad (1)$$

where $z = I_1 + I_2 + \cdot + I_k$, I_k is the current of the k th ULSB cell, $u = k\bar{I}$ and $\bar{I} = \frac{I_1+I_2+\cdots+I_{15}+I_{16}}{16}$.

However, Equation (1) is based on the assumption that there exists no correlation between any of the current-sources. Then, the yield of INL is obtained by multiplying the probabilities that the INL of each output case is smaller than 0.5 LSB. While in this design the current of 16 ULSBs is not independent, the sum of them is equal to the current of one MSB source. The INL yield of the case that all 16 ULSBs are turned on contains the other switching cases. After verification by the Monte Carlo simulation, Equation (1) is optimized as

$$G = \int_{16\bar{I}-0.5I_{\mathrm{ULSB}}}^{16\bar{I}+0.5I_{\mathrm{ULSB}}} \frac{1}{\sqrt{2\pi}\sigma_{\mathrm{u,16}}} \exp\left(-\frac{(z-u)^2}{2\sigma^2_{\mathrm{u,16}}}\right)\mathrm{d}z. \quad (2)$$

Given a 99.7% yield, $\sigma_{\mathrm{u}} = 0.2\ \mu A$ is figured out from Eq. (2) and then the dimension can be obtained according to the Pelgom model[5],

$$\frac{\sigma^2}{I^2} = \frac{1}{WL}\left(A^2_\beta + \frac{4A^2_{\mathrm{Vt}}}{V^2_{\mathrm{ov}}}\right), \quad (3)$$

where V_{ov} is the overdrive voltage and $A_\beta = 0.0139\ \mu$m, $A_{\mathrm{Vt}} = 6.98\ \mathrm{mV}\cdot\mu\mathrm{m}$ for PMOS[6].

3.4. Return-to-zero output stage

In order to enlarge the output voltage swing, which is limited by 5 stacked transistors below the floating source output (the drain of M1 in Fig. 2), and reduce the impact of the current-sources' limited output impedance, a folded output stage is adopted, as shown in Fig. 7. The drain voltages of M3 and M4 are clamped by the inputs of the OTA. And to maintain signal-independent accuracy, which means the signal-dependent fluctuation at node A and B should as small as possible, the OTA is required to retain high gain at high frequency.

The OTA with 40-dB DC gain and 600-MHz GBW is finally chosen by limiting the different currents from bias current-source smaller than 0.5 LSB considering the toughest situation that all the 16-mA current flows through one side. The cost is 12-mA current consumption (4-mA for the gain-boosted OTA), comparing with the direct output structure.

The RTZ (return-to-zero) technique is helpful to improve the SFDR when signal frequencies are high and the RTZ option with cross-coupled switches topology[3] is adopted here. With careful design of the timing relationship between the main clock and RTZ control signal, the glitch generated during the switching transient can be totally masked by setting the output differential voltage to zero at the cost of a shorter settling time.

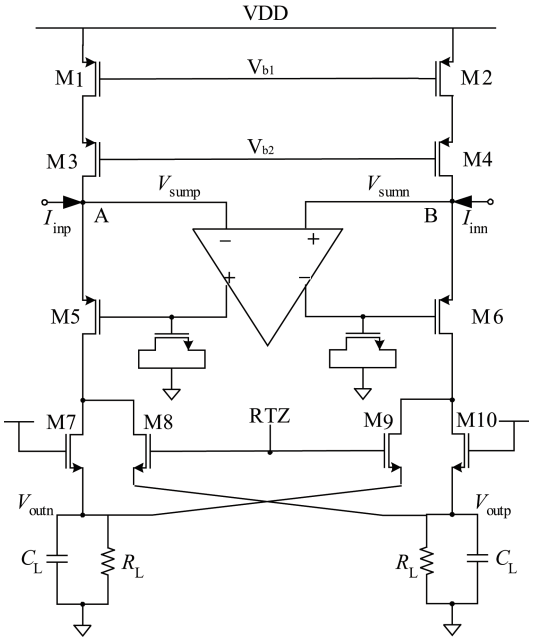

Fig. 7. Schematic of output stage.

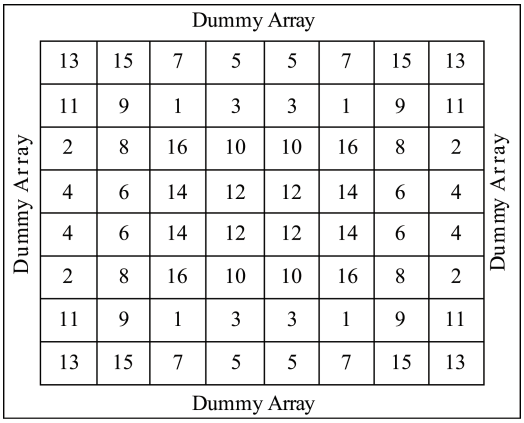

Fig. 8. Layout arrangement of the ULSB.

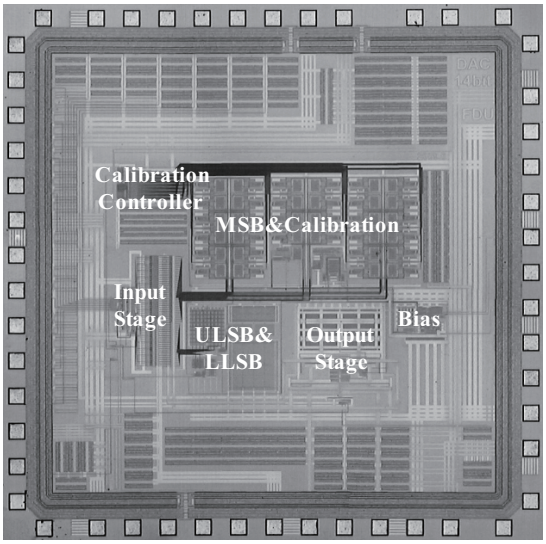

Fig. 9. Die micrograph.

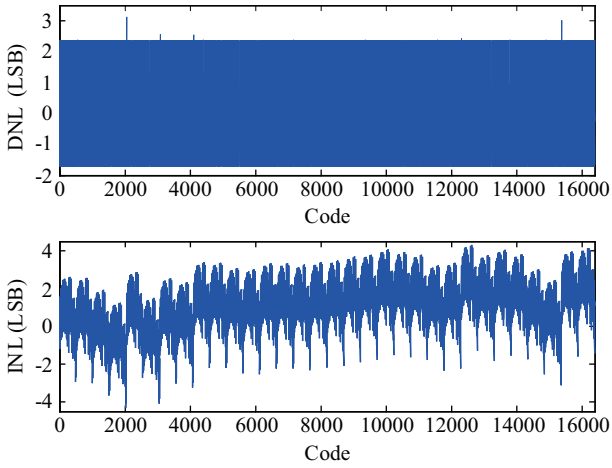

Fig. 10. Measured DNL and INL.

3.5. Layout solutions

Considering the current of MSB cells is trimmed by the calibration circuit, the MSB layout is implemented with a simple two-dimensional common-centroid strategy to reduce the mismatch caused by the manufacture.

While the lower ULSB and LLSB need to obtain 9-bit intrinsic accuracy by layout arrangement. 'INL Bounded Switching Sequences'[9] has been adopted to cancel both the linear and the quadratic errors. Figure 8 shows the layout arrangement of the ULSB arrays, four squares with the same number forming one cell. And because the dimensions of these transistors are somewhat large, substrate contacts should be carefully placed.

4. Experimental results and analysis

The DAC is implemented in a SMIC 0.13-μm CMOS process and its die micrograph is shown in Fig. 9. The die area is around 4 mm^2 with a core area of 1.29 mm^2.

A four-layer evaluation board is designed to test the DAC performance. The measurement results presented here are taken differentially at the output, and a transformer is used while measuring the dynamic performance.

The measured static performances are shown in Fig. 10 with DNL = 3.1 LSB and INL = 4.3 LSB. And the measured SFDR versus output signal frequency with and without RTZ is shown in Fig. 11.

The adopted calibration technique improves the SFDR of the DAC greatly. When the calibration is turned on, the SFDR is 72.81 dB, 17 dB better than that without calibration at the clock rate of 100 MS/s and 1-MHz output sinusoid signal, as shown in Fig. 12.

From Fig. 10, it can be found that the worst case appears at code transition from 2047 to 2048. This indicates that the error of one MSB current-source caused by chip manufacture is beyond the 10% calibration range. And the voltage of 1 LSB, which is 0.044 mV, is easily submerged in the noise, the test statistic results are influenced by the test instruments and test

Table 1. Performance summary and comparison.

Parameter	This work	AD9767[10]	JSSC2007[11]
Technology	CMOS 0.13 μm	CMOS	CMOS 0.18 μm
Resolution (bit)	14	14	14
Update rate (MHz)	100	125	200
INL (LSB)	4.3	3.5	1.37
DNL (LSB)	3.1	3.5	0.76
SFDR (1 MHz @ 100 MSps) (dBc)	72.8	82	81.5
Power dissipation (mW)	165 @ 100 MHz, 3.3 V	450 @ 100 MHz, 5 V	130 @ 100 MHz, 1.8 V
Core area (mm^2)	1.29	N/A	3

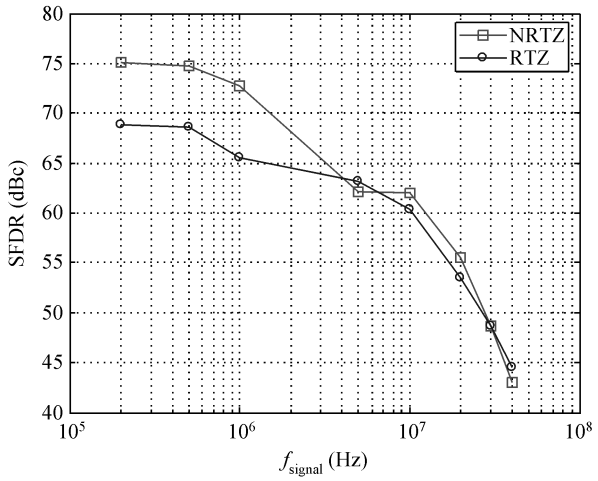

Fig. 11. SFDR performance.

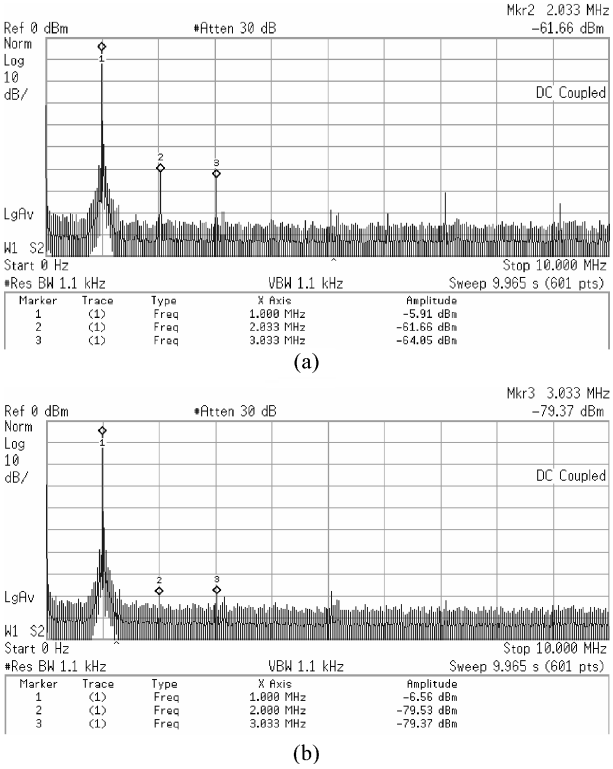

Fig. 12. Output single-tone spectrum at 1 MHz, 100 MSample/s. (a) Calibration off. (b) Calibration on.

environment seriously. And considering the situation that noise with a sinc shape is added to the noise floor when the RTZ is turned on, that the measured SFDR under RTZ mode is not so good as desired is possibly limited by the quality of the clock. The decreased slope of the RTZ control signal increases both noise and harmonic distortions. If so, an on-chip clock reshape circuit is essentially required to solve this problem.

Table 1 summarizes the performance of this chip compared with two 14-bit DACs presented in Refs. [10, 11].

5. Conclusion

This paper has presented the design and implementation of a self-calibrated 14-bit, 100 MS/s DAC. The key features of this DAC are the analog background self-trimming technique, a refresh spur cancellation circuit, a constant load switch driver, a return-to-zero output stage, and an 'INL bounded switching sequences' layout strategy. The measured SFDR is 72.8 dB at the clock rate of 100 MS/s and 1-MHz output sinusoid signal.

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