Process optimization of a deep trench isolation structure for high voltage SOI devices

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Abstract: The process reasons for weak point formation of the deep trench on SOI wafers have been analyzed in detail. An optimized trench process is also proposed. It is found that there are two main reasons: one is over-etching laterally of the silicon on the surface of the buried oxide caused by a fringe effect; and the other is the slow growth rate of the isolation oxide in the concave silicon corner of the trench bottom. In order to improve the isolation performance of the deep trench, two feasible ways for optimizing the trench process are proposed. The improved process thickens the isolation oxide and rounds sharp silicon corners at their weak points, increasing the applied voltage by 15–20 V at the same leakage current. The proposed new trench isolation process has been verified in the foundry's 0.5-μm HV SOI technology.

Key words: deep trench isolation; SOI; weak point; process optimization
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1. Introduction

With the rapid development of IC processes, integrating CMOS with DMOS on the same chip is feasible for analog ICs. Electrical isolation is needed between adjacent devices, especially power devices. Junction isolation was proposed earlier. However, if high voltage devices are isolated with junction isolation, it cannot be accepted for larger inter-device separations and very high temperature dependence[1]. More recently, deep trench isolation in combination with LOCOS has been used in the case of high-voltage devices for analog and power applications[2]. A deep trench isolation process provides very low leakage current, low temperature dependence and minimal space consumption[3]. Therefore, low leakage current from high voltage transistors separated by a deep trench suppresses the trigger of the latch-up mechanism to low voltage circuits. In addition, the chip size is reduced significantly with desirable isolation performance for bad stress conditions, hence reducing the process cost.

Deep trench isolation processes for high voltage SOI (silicon on insulator) integrated circuits have been developed and reported previously. The isolation structure on the SOI wafer is composed of two layers of silicon dioxide with a layer of low doped polysilicon embedded[4]. Then, the vertical isolation is provided by a thick buried oxide layer. Lateral isolation is realized by two layers of silicon dioxide. A deep trench isolation structure makes it possible that every device can be freely designed within adjacent shielded silicon islands, making no crosstalk between devices.

However, two major drawbacks associated with the formation of deep trenches are encountered. One is the damage to the silicon semiconductor material in regions adjacent to the trench caused by subsequent annealing or heat treatment of the wafer. The corners of the trench are known to be the mechanism for generating crystallographic dislocations and faults[5]. Sloped etching at the upper trench corners reduces the subsequent formation of crystal faults due to high temperature oxidation[1, 5]. The other is the weak point of isolation oxide formation at the trench bottom. The weak point increases the leakage current at the same bias voltage[6]. In this paper, the main process factors forming the weak point at the deep trench bottom are firstly analyzed in detail. Furthermore, experiments based on feasible proposals are performed. According to the experimental results of the optimized process using etching partial buried oxide, the isolation oxide layer at the weak point is 1.3 times thicker than that using the standard process. Consequently, the breakdown voltage has been improved by 15–20 V.

2. Experimental details

2.1. Process and structure information

A schematic cross section and SEM cross section of a thick SOI wafer with a 7 μm deep trench isolation structure are shown in Fig. 1. The sidewall oxide and buried oxide ensure the insulating capability. Poly silicon refilling provides the mechanical stability of the structure[1]. Table 1 lists the main process flows of the deep isolation trench. Low pressure TEOS

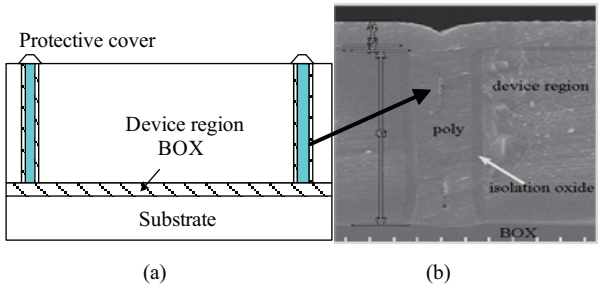

Fig. 1. (a) Schematic cross section and (b) SEM cross section of deep trench isolation on a 7 μm SOI wafer.

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Table 1. Main process flows of deep trench isolation.

Process variant	Content
LPTEOS	200–500 Å
Deposit	Si_3N_4 and photoresist
Etch silicon	Width (1–3 μm)
Removal polymer	Si_3N_4, photoresist and oxide
Thermal isolation oxide	2000–5000 Å
Poly refilling	6000–12000 Å
Poly etch	Etch remainder poly

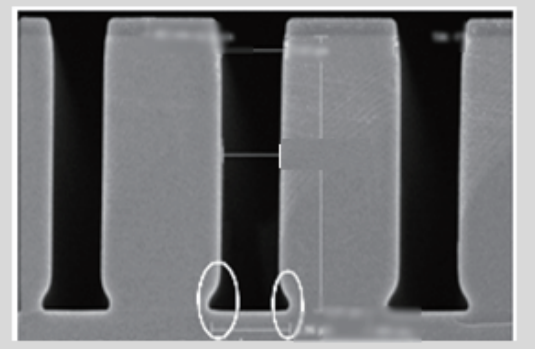

Fig. 2. Fringe effects in the SEM cross section of the SOI deep trench structure after silicon etching.

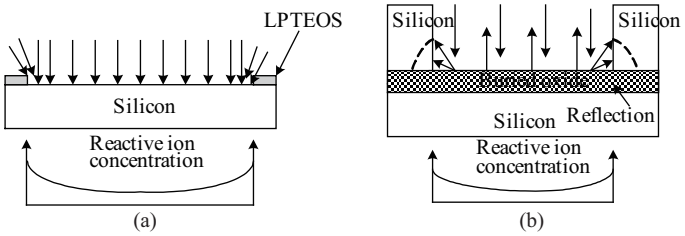

Fig. 3. Fringe effect of the reactive ion concentration. (a) At the top of trench. (b) At the bottom of trench.

(LPTEOS) was patterned as a mask for silicon etching[5]. To prevent trench sidewall to be inversion, P type field implant is also necessary [7].

2.2. Fringe effect at the top and bottom of the deep trench

Figure 2 shows an SEM cross section of the trench after silicon etching. However, lateral over-etching of the bottom silicon can be observed. It is measured that the trench width at the top, in the middle and at the bottom is 109%, 101%, and 131% of the target value, respectively. The width deviation can be explained by the fringe effect during the silicon etching process in Fig. 3.

In Fig. 3(a), the "fringe effect" from Ref. [8] causes the reactive ion concentration in the fringe region of the trench to be higher than that in the middle region of trench, then different etching rates are distributed in different surface regions[8]. So the trench width in the top region is larger than that in the middle region.

The reactive ion concentration at the trench bottom is illustrated in Fig. 3(b). Because of the inactive characteristics of the

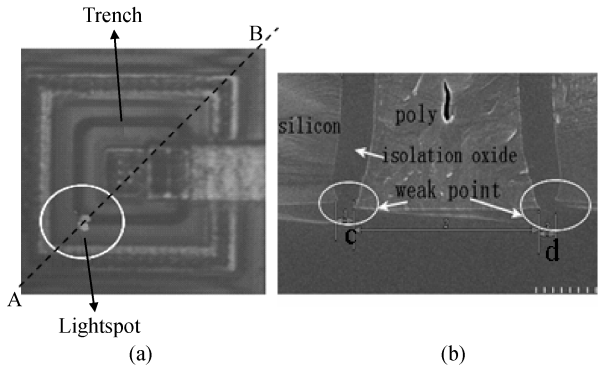

Fig. 4. Inconformity of the isolation oxide layer. (a) Light spot position in the EMMI experiment. (b) SEM cross section of the SOI deep trench following the A–B direction.

buried oxide layer in the SOI structure, the buried oxide layer can reflect reactive ions as a mirror reflecting light. Just like that on the surface of trench, the fringe effect also makes the etching width larger at the bottom of the trench than in the middle region. During the next oxidation process, the density of the reactive oxygen gas in the silicon scallop hole due to over-etching laterally is much less than that on the silicon sidewall. In addition, the exchange of reactive gas in the scallop hole is not adequate. Therefore, over-etching laterally at the bottom of the trench slows the isolation oxide growth rate, helping to form the thinnest oxide layer called the weak point in the next section.

2.3. Weak points for leakage current

Figure 4(a) shows the most serious leakage location, which was displayed as the light spot during EMMI (emission microscope) analysis. While a high voltage was biased at the inner pad, a light spot appeared at the corner of the trench until the isolation oxide of the deep trench suffered dielectric breakdown. Then, an SEM cross section of the SOI deep trench following the A–B direction was carried out, as shown in Fig. 4(b). Obviously, weak points which have the thinnest thermal oxide are located at the region where active silicon, BOX and poly silicon join with the thermal oxide. Therefore, weak points labeled as c and d in Fig. 4(b) should be responsible for the light spot in Fig. 4(a). Weak points or large leakage current at these points are correlated with the oxide thinning effect at the concave corners of the silicon. The oxide thinning effect is caused by stress-dependent oxide growth at the convex and concave corners of the trench structure[9], and accelerated by the previous laterally over-etching silicon, causing lower reactive gas density and a worse exchange rate of oxygen gas at the bottom. Because of these reasons for the isolation oxide thinning effect, sharp corners of silicon and the thinnest isolation oxide are formed. Sharp silicon corners will result in excess stress and defects at the interface between the isolation oxide layer and the silicon film during oxidation, ultimately faulted joints. Moreover, the thinnest isolation oxide will flow through most of the Fowler–Nordheim tunneling current[10]. Therefore, these weak points determine mainly the electrical isolation capability of the deep trench.

Figure 5 shows the distribution of the electrical field and the electrostatic potential at the bottom of the trench following

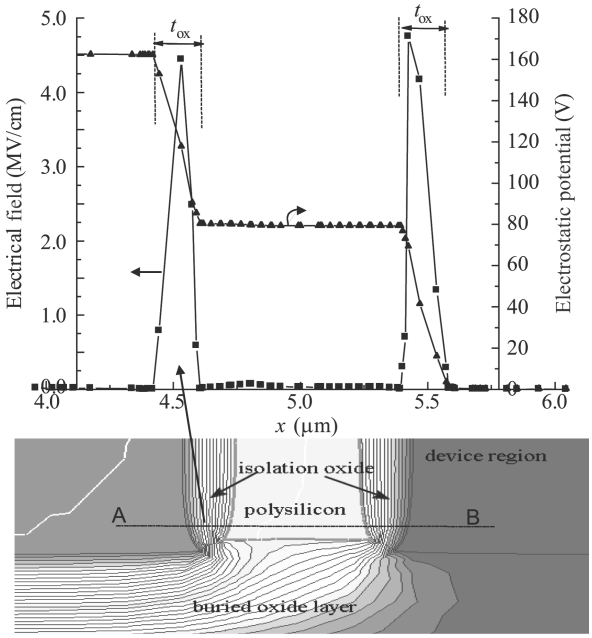

Fig. 5. Distribution of electrical field and electrostatic potential at the bottom of the trench following the A–B direction simulated by a Sentaurus TCAD tool.

the A–B direction using a TCAD simulation tool. The crowding electrostatic potential lines lead to a strong electric field at the bottom of the trench, as can be seen by two peak values in the simulation results. When the voltage bias is large enough, such weak points are firstly closed to a critical electrical field for Fowler–Nordheim tunneling[10] and ultimately dielectric breakdown. So the remarkable leakage current rise and light spot at the trench corner during EMMI analysis can be explained by the weak point.

3. Experimental results and discussion

To obtain superior isolation quality, increasing the isolation oxide thickness and improving the isolation oxide quality at the weak point have been proposed in prior work[7, 10, 11]. However, these methods aim to increase the energy budget and annealing time, probably affecting the N or P well junction depth. Based on the standard process conditions, feasible and effective ways of improving the isolation performance of the deep trench without increasing the process cost is necessarily proposed. According to the test results and the SEM analysis, etching the partial buried oxide layer can improve the weak point. When low pressure TEOS was etched after the etching silicon process, etching the partial buried oxide layer simultaneously for 15%–25% of the thickness of the buried oxide layer can accelerate oxide growth at the trench bottom. Etching partial BOX moves the trench bottom down to promote more reactive gas flowing through the silicon corner above the trench bottom and accelerates the oxide growth at the weak point. Then a thicker isolation oxide layer will be grown at points e and f in Fig. 6. Here, the depth for etching the buried oxide layer is given according to many test results, without decreasing the vertical breakdown voltage of the SOI. Figure 6 shows an SEM cross section of the SOI deep trench below which the BOX (buried oxide layer) was etched for "L" μm. To compare the

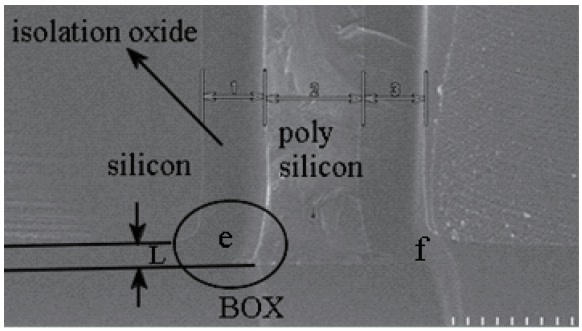

Fig. 6. SEM cross section of the SOI trench with the partial BOX being etched.

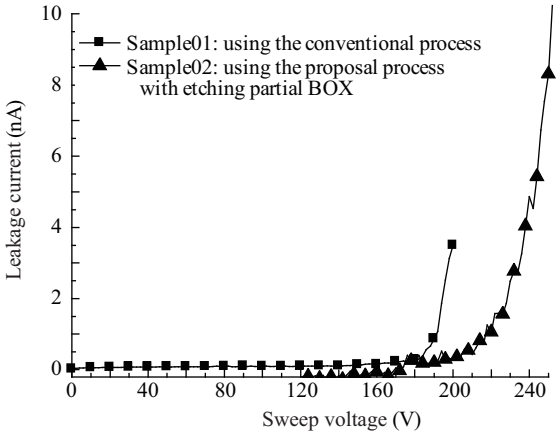

Fig. 7. Leakage current as a function of sweep voltage for the new recipe.

isolation performance of the different structures, the start point of the remarkable leakage current rise is defined as the breakdown voltage. In Fig. 7, the breakdown voltage is improved for 15–20 V by etching the partial BOX recipe, comparing it with the standard process in Table 1.

An additional sacrificial oxide process prior to thermal oxide is also confirmed to be an effective approach. Figure 8 shows the I–V curves for the different process variants. For the standard process with the standard isolation oxide thickness in Table 1, the breakdown voltage is about 180 V, while an increase of about 15 V can be clearly seen for the process with additional sacrificial oxide and the standard isolation oxide layer. This is because that sacrificial oxide process rounds the surface of the sidewall and sharp silicon corners for uniform distribution of the electrical field lines in the insulated oxide. Thus, the peak value of the electrical field at the bottom of the deep trench is lowered under the same voltage bias.

4. Conclusion

The weak point at the trench bottom is one of the key factors for leakage current through the deep trench on the SOI wafer. Thinner isolation oxide at the weak point is crowded by electrical field lines, increasing the Fowler–Nordheim tunneling current. There are two main reasons for forming the weak points. One is over-etching silicon laterally at the bottom of the trench caused by the fringe effect. The other is the slow growth

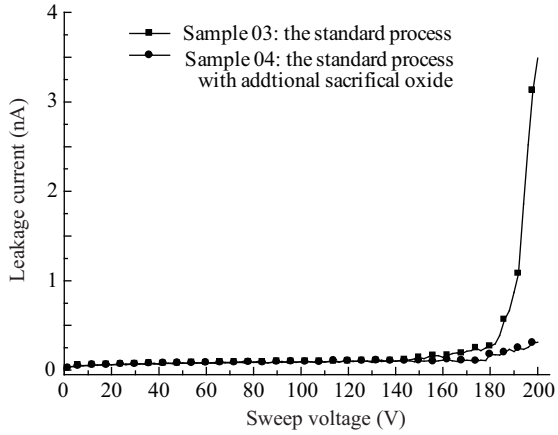

Fig. 8. Leakage current as a function of voltage for different process conditions.

rate of the thermal oxide for the concave silicon corner. Two effective ways to restrain the formation of a weak point are also proposed. It is concluded that etching the partial buried oxide increases the isolation oxide thickness at the weak point and the breakdown voltage has been improved by 15–20 V. Additional sacrificial oxide smoothes the sharp corners on the surface of the sidewall and trench bottom. Thus, the distribution of the electrical field is more uniform at the silicon corners, leading to a breakdown voltage higher than 200 V. The proposed new trench isolation process has been verified in the foundry's 0.5-μm HV SOI technology. According to the optimized trench process, desirable isolation capability of the deep trench satisfies 200 V power IC on the SOI wafer.

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