Complementary charge islands structure for a high voltage device of partial-SOI*

Wu Lijuan(吴丽娟)[1, 2, †], Hu Shengdong(胡盛东)[1, 3], Zhang Bo(张波)[1], and Li Zhaoji(李肇基)[1]

[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China
[2]College of Communication Engineering, Chengdu University of Information Technology, Chengdu 610225, China
[3]College of Communication Engineering, Chongqing University, Chongqing 400044, China

Abstract: A new partial-SOI (PSOI) high voltage device structure named CNCI PSOI (complementary n^+-charge islands PSOI) is proposed. CNCI PSOI is characterized by equidistant high concentration n^+-regions on the top and bottom interfaces of a dielectric buried layer of a PSOI device. When a high voltage is applied to the device, complementary holes and electron islands are formed on the two n^+-regions on the top and bottom interfaces, therefore effectively enhancing the electric field of the dielectric buried layer (E_I) and increasing the breakdown voltage (BV), alleviating the self-heating effect (SHE) by the silicon window under the source. An analytical model of the vertical interface electric field for the CNCI PSOI is presented and the analytical results are in good agreement with the 2D simulation results. BV and E_I of the CNCI PSOI LDMOS increase to 591 V and 512 V/μm from 216 V and 81.4 V/μm of the conventional PSOI with a lower SHE, respectively. The influence of structure parameters on the device characteristics is analyzed for the proposed device in detail.

Key words: PSOI; complementary; charge islands; breakdown voltage; SHE
DOI: 10.1088/1674-4926/32/1/014003 **PACC:** 7340T; 7300; 7340L

1. Introduction

There are two major concerns in the development of SOI technology which increase the breakdown voltage (BV) and reduce the self-heating effect (SHE). Some studies have been carried out to solve the former[1−4]. Enhancing the electric field of the dielectric buried layer is an effective method to increase the BV by the ENDIF (enhanced dielectric layer field)[5, 6] and several new structures have been developed by the ENDIF[7−11]. Moreover, partial-SOI (PSOI) technology can reduce the SHE due to its silicon window connecting the active region to the substrate, which offers a heat conduction path while achieving a high BV[12−14]. In this paper, a new interface charge island structure of a high voltage device on a PSOI (CNCI PSOI) and its analytical model of a vertical interface electric field are proposed. The operation of a CNCI PSOI is different from all of the above-mentioned structures and it provides a new and effective method to enhance the electric field of the dielectric buried layer by introducing interface charges and so increasing the BV, reducing the SHE at the same time. The influences of structure parameters on the BV and the SHE are analyzed and compared with the conventional PSOI and SOI.

2. Structure and mechanism

CNCI PSOI LDMOS and its mechanism are shown in Fig. 1. Equidistant high concentration n^+-regions are made on the interface of the top and bottom dielectric buried layer (SiO_2), and there is a silicon window under the source. t_S, t_I, t_{sub}, t_p and H denote the thicknesses of the top silicon layer, the dielectric buried layer, the substrate layer, the p-top layer and the interface n^+-regions, L_d, L_W, D and W are the lengths of the drift region, the silicon window, the interface n^+-regions, and the spacing of two neighboring n^+-regions, and N_d, N_p, N_{n+} and N_{sub} are the impurity concentrations of the drift region, the p-top layer, the interface n^+-regions and the substrate layer, respectively. When a high positive voltage V_d is applied to the drain while the source, gate and substrate are grounded, the inversion holes are formed in the spacing of equidistant n^+-regions by the vertical electric field (E_V) and located on the top interface by the compositive operation of Coulomb's forces with the ionized donors in the undepleted n^+-regions as well as the force from the lateral electric field (E_L), and electrons are induced and located on the interface of the bottom dielectric buried layer (SiO_2).

For a lateral PSOI LDMOS high voltage device which has been optimized by junction terminal technology, its BV lies on its vertical BV ($V_{B,V}$) and is composed of V_S, V_I and V_{sub}, which are the voltages shared by the top silicon layer, the dielectric buried layer and the substrate layer, respectively. Based on the continuity of the electric displacement with interface charges, E_I of SOI/PSOI can be written as

$$E_I = \frac{q\sigma_{in}}{\varepsilon_I} + \frac{\varepsilon_S}{\varepsilon_I} E_S, \tag{1}$$

where E_S is the electric field of the silicon on the interface, q is the electron charge, σ_{in} is the inversion charge density on the interface, and ε_S and ε_I are the permittivities of silicon and the dielectric buried layer, respectively. From Eq. (1), the BV of

* Project supported by the National Natural Science Foundation of China (Nos. 60806025, 60976060), the NKLAIC Project (No. 9140 C0903070904), and the Youth Teacher Foundation of University of Electronic Science and Technology of China (No. jx0721).
† Corresponding author. Email: ljwu@cuit.edu.cn
Received 1 July 2010, revised manuscript received 8 August 2010

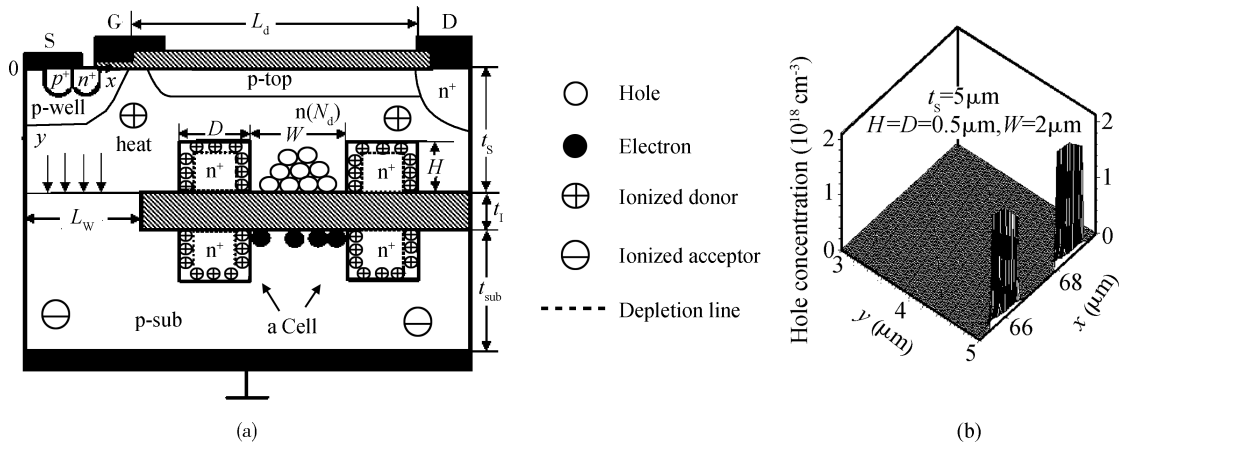

Fig. 1. Schematic cross section of CNCI PSOI LDMOS and the charges in the CNCIs. (a) Device structure. (b) Three-dimensional hole distribution in a pair of neighboring n+-regions near the drain (t_S = 5 μm, t_I = 1 μm, $H = D = 0.5$ μm, W = 2 μm and V_d = 591 V).

Table 1. Device parameters used in the simulation.

Device parameter	CNCI SOI	Con. PSOI	Con. SOI
Drift length, L_d (μm)	30–90	30–90	30–90
Thickness of SOI layer, t_S (μm)	5	5	5
Thickness of buried layer, t_I (μm)	1	1	1
Thickness of p-top layer, t_p (μm)	0.5, 1, 1.5	–	–
Thickness of p-substrate layer, t_{sub} (μm)	30	30	30
p-substrate concentration, N_{sub} (cm^{-3})	(1–8) $\times 10^{14}$	(1–8) $\times 10^{14}$	(1–8) $\times 10^{14}$
Thickness of CNCI, H (μm)	0–1.2	–	–
n^+-region length in CNCI layer, D (μm)	0–2	–	–
spacing of two neighboring n^+-region in CNCI, W (μm)	1–3.5	–	–
n^+-region concentration in CNCI layer, N_{n+} (cm^{-3})	1×10^{19}	–	–

the PSOI is obtained as

$$\mathrm{BV} = \frac{q\sigma_{\mathrm{in}} t_{\mathrm{I}}}{\varepsilon_{\mathrm{I}}} + \left(0.5t_{\mathrm{S}} + \frac{\varepsilon_{\mathrm{S}}}{\varepsilon_{\mathrm{I}}} t_{\mathrm{I}}\right) E_{\mathrm{S}} + V_{\mathrm{sub}}. \qquad (2)$$

The n-type drift region with relative high potential, the buried dielectric layer and the substrate with low potential act as an MIS-like structure, and σ_{in} has the expression as

$$\sigma_{\mathrm{in}} = \left(\frac{2k_0 T \varepsilon_{\mathrm{S}} n_{\mathrm{i}}^2}{q^2 N_{\mathrm{d}}} \exp\frac{q\phi_{\mathrm{S}}}{k_0 T}\right)^{1/2}, \qquad (3)$$

where N_d is the impurity concentration in the drift region, and k_0, T, n_i and ϕ_S are the Boltzmann constant, the absolute temperature (T = 300 K at room temperature), the intrinsic carrier concentration of silicon, and the surface potential on the interface of the top silicon layer and the dielectric buried layer, respectively[15]. From Eq. (3), σ_{in} exponentially increases with ϕ_S and should effectively enhance E_I and the BV by Eqs. (1) and (2). Each adding σ_{in} to 1×10^{12} cm^{-2} can enhance E_I of 46.4 V/μm. In the conventional PSOI, however, σ_{in} is actually ignored because of the extraction of the lateral electric field, and how to fix the inversion charges and utilize them effectively is imperative and significant work.

3. Results and discussion

Two-dimensional device simulations[16] for the proposed CNCI PSOI, the conventional PSOI and the SOI were performed to verify the device operations.The device parameters used in the simulation results are listed in Table l.

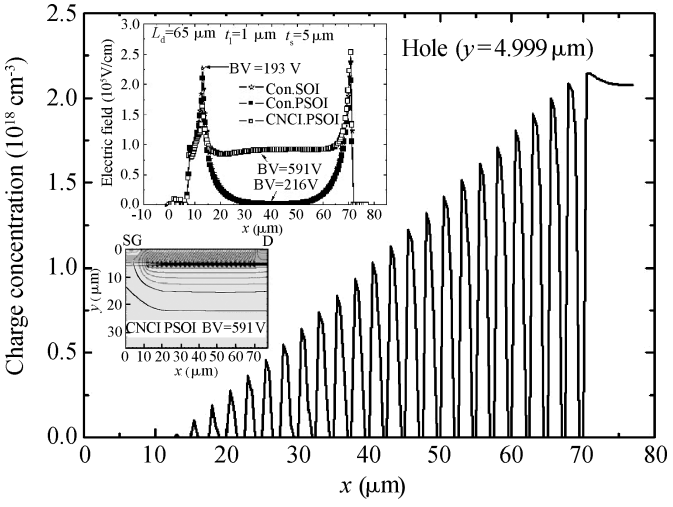

Fig. 2. Distributions of the interface holes (y = 4.999 μm), the surface electric field (y = 0.001 μm) and the equipotential contours for the CNCI PSOI at breakdown.

Figure 2 shows the distribution of the interface holes (y = 4.999 μm), the surface electric field (y = 0.001 μm) and the equipotential contours for the CNCI PSOI at breakdown. It is obvious that there are high concentration holes ($> 1 \times 10^{18}$ cm^{-3}) distributed on the interface whose density increases lin-

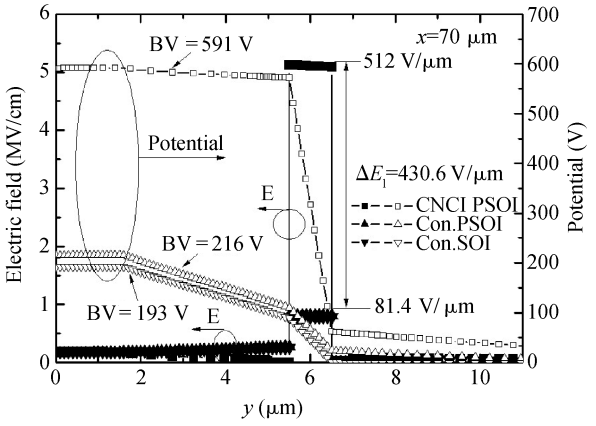

Fig. 3. Electric fields and potential distributions at breakdown for the CNCI PSOI, the conventional PSOI and the SOI. $t_S = 5\ \mu$m, $t_I = 1\ \mu$m, $t_{sub} = 30\ \mu$m, $L_d = 65\ \mu$m, and $N_{sub} = 3 \times 10^{14}$ cm^{-3} for all. N_d is 0.9 $\times 10^{15}$ cm^{-3}, 1.95 $\times 10^{15}$ cm^{-3}, 2.25 $\times 10^{15}$ cm^{-3} for the three structures, respectively. $L_W = 12\ \mu$m for the PSOI. $H = D = 0.5\ \mu$m, $W = 2\ \mu$m, $t_p = 1\ \mu$m, and $N_p = 1.65 \times 10^{16}$ cm^{-3} for the CNCI PSOI.

early from the source to the drain. Because of the modulating effect of the interface holes, the equipotential contours and the surface electric field distributions are more uniform than those of the conventional PSOI and SOI.

Figure 3 illustrates the vertical electric fields and potentials distributions at breakdown for the CNCI PSOI, the conventional PSOI and the SOI. It can be seen that E_I of the CNCI PSOI increases from 81.4 V/μm of the conventional PSOI and 77.9 V/μm of SOI to 512 V/μm due to the enhancement effect of the inversion charges. Moreover, the inversion charges reduce the silicon layer electric field on the interface to 7.6 V/μm and avoid silicon layer premature breakdown for the CNCI PSOI. All of the above-mentioned results in a high BV of 591 V for the CNCI PSOI compared to 216 V for the conventional PSOI and 193 V for the SOI. Moreover, above 85% of the BV for the CNCI PSOI is shared by the dielectric buried layer ($V_I = t_I E_I$ = 512 V) from the potential distributions shown in Fig. 3, and V_I is dominant in the BV. The simulation results are in agreement with the analytical results of Eqs. (1) and (2) in Fig. 1, and it can be concluded that the interface charges accumulated by the proposed CNCI PSOI can assuredly enhance E_I and increase the BV.

Figure 4 shows the influences of the structure parameters on the BV for the CNCI PSOI. Figure 4(a) shows the influences of H, D, W and L_d on the BV. It can be seen from Fig. 4(a) that there is a maximum BV = 591 V with $H = D = 0.5\ \mu$m and $W = 2\ \mu$m, and the BV is improved with increasing L_d, which breaks through the BV limitation of the conventional PSOI just shown in Fig. 4(a), too. Moreover, when H or D is 0 μm, the CNCI PSOI becomes a conventional PSOI whose BV is only 216 V. Figure 4(b) is the influences of the p-top layer and the substrate concentrations (N_{sub}). The maximal BVs are almost equal for different p-top layer thicknesses (t_p) of 0.5, 1 and 1.5 μm. In additions, the maximal BVs appear when $N_p t_p$ is about 1.65 $\times 10^{12}$ cm^{-2}, which satisfies the RESURF (reduced surface field) condition, and after that, the BV sharply decreases because of premature breakdown at the n$^+$–p junction of the drain side. N_{sub} has a faint influence on the BV, and the BV only decreases by 3.56% when N_{sub} increases from 1 $\times 10^{14}$

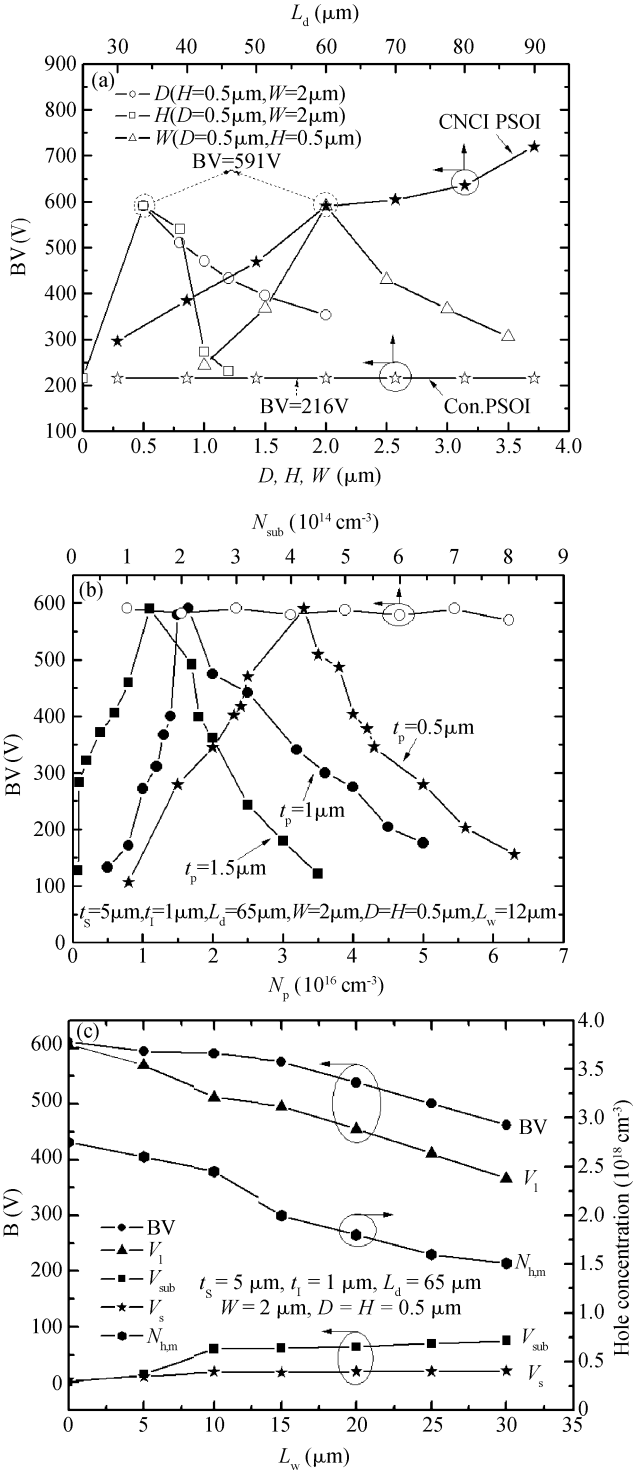

Fig. 4. Influences of device parameters on breakdown voltage. $t_S = 5\ \mu$m, $t_I = 1\ \mu$m, $t_{sub} = 30\ \mu$m for all. (a) H, D, W and L_d on breakdown voltage. $L_d = 65\ \mu$m for H, D, and W. $H = D = 0.5\ \mu$m and $W = 2\ \mu$m for L_d. $N_{sub} = 3 \times 10^{14}$ cm^{-3} for all. (b) N_p (with $N_{sub} = 3 \times 10^{14}$ cm^{-3}) and N_{sub} on breakdown voltage. $H = D = 0.5\ \mu$m, $W = 2\ \mu$m and $L_d = 65\ \mu$m for all. (c) Silicon window length L_W on voltages and hole concentration under the drain. $H = D = 0.5\ \mu$m, $W = 2\ \mu$m, $L_d = 65\ \mu$m, $N_{sub} = 3 \times 10^{14}$ cm^{-3} for all.

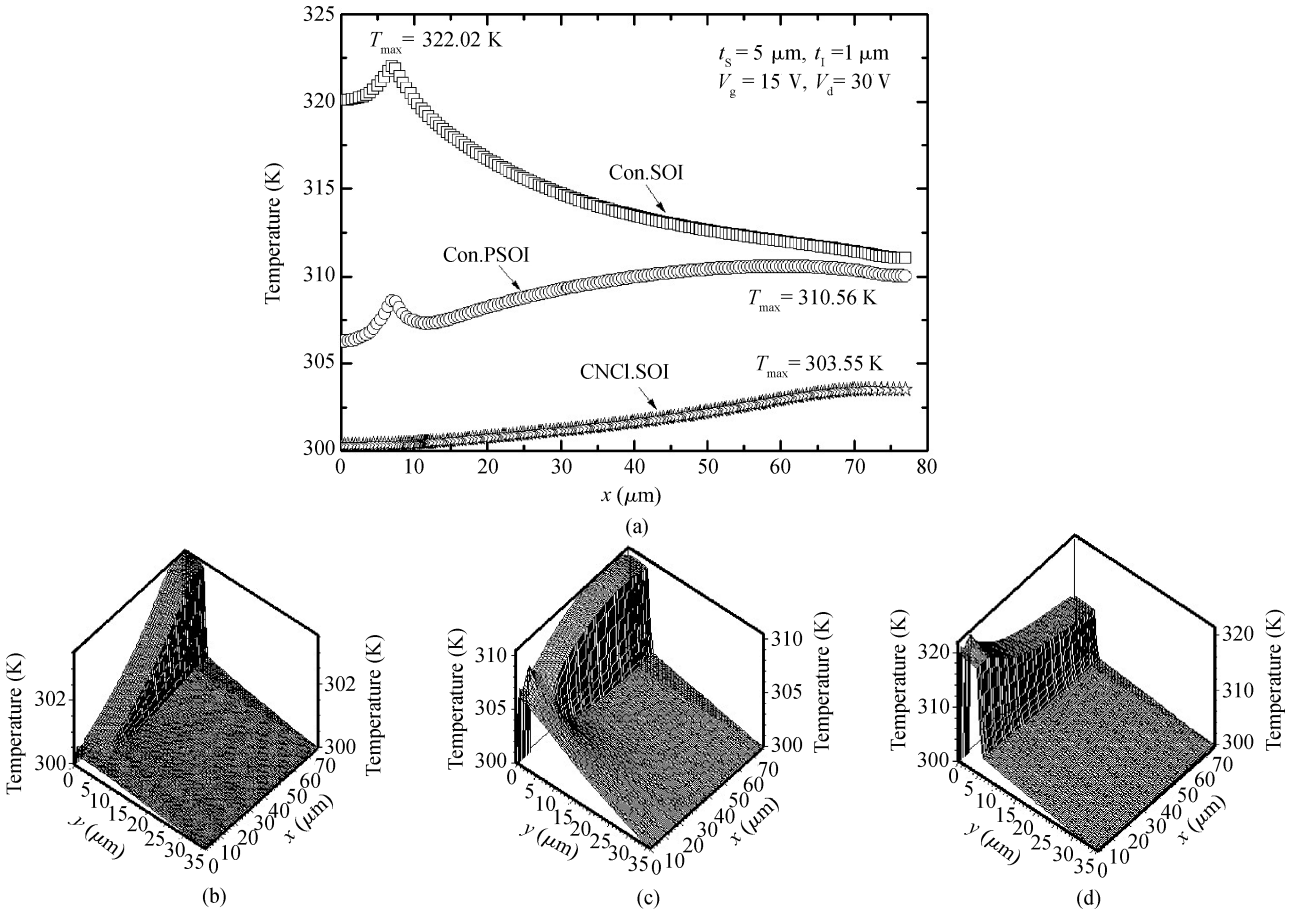

Fig. 5. Thermal characteristics with V_d = 30 V and V_g = 15 V. (a) Surface temperature profiles (y = 0.001 μm) for the CNCI PSOI, the conventional PSOI and the SOI. (b) Three-dimensional temperature profiles of the CNCI PSOI. (c) Three-dimensional temperature profiles of the conventional PSOI. (d) Three-dimensional temperature profiles of the conventional SOI.

to 8×10^{14} cm^{-3}. Figure 4(c) gives the influences of the silicon window length L_W on the voltages and hole concentrations under the drain. Although V_{sub} increases slowly because of the extension of the depletion layer into the substrate, the BV decreases with increasing L_W. This is due to the reduction of the maximal interface hole concentration under the drain side, which results from the more fall of V_I. Therefore, E_I is decreased by Eq. (1).

Figure 5 gives the thermal characteristics of the CNCI POI, the conventional PSOI and the SOI. The bottom of the substrate is held at 300 K, and the gate voltage (V_g) is 15 V for all simulations. With V_d of 30 V, it can be seen that the surface temperatures of the CNCI PSOI are the lowest, and the maximal temperature T_{max} (303.55 K), but that of the conventional SOI is 322.02 K. Moreover, the situations of T_{max} of the CNCI PSOI and the conventional PSOI are under the drain due to the existence of silicon windows under the source, whereas that of the conventional SOI is under the source, which can be seen more clearly in Figs. 5(b)–5(d). It can be concluded that the proposed CNCI PSOI can enhance the breakdown voltage while maintaining the lower SHE.

4. Conclusion

A novel complementary N+-charge island structure of high voltage device on partial-SOI (CNCI PSOI) is proposed in this paper. A CNCI PSOI effectively utilizes the enhancement effect of the interface charges on the electric field of the dielectric buried layer to increase the breakdown voltage while alleviating the self-heating effect by the silicon window under the source. The BV for the CNCI PSOI increases by 174% and 206 % while the maximal temperature at V_g = 15 V and V_d = 30 V decreases by 7.01 K and 18.47 K in comparison with the conventional PSOI and the SOI devices, respectively. The CNCI PSOI has potential for applications in high voltage and power integrated circuits because of its favorable performance and easy fabrication process.

References

[1] Merchant S, Arnold E, Baumgart H, et al. Realization of high breakdown voltage (> 700 V) in thin SOI device. Proc IEEE Int Symp Power Semiconductor Devices and IC's, 1991: 31

[2] Nakagawa A, Yasuhara N, Baba Y. Breakdown voltage enhancement for devices on thin silicon layer/silicon dioxide film. IEEE Trans Electron Devices, 1991, 38(7): 1650

[3] Funaki H, Yamaguchi Y, Hirayama K, et al. New 1200 V MOSFET structure on SOI with SIPOS shielding layer. Proc IEEE Int Symp Power Semiconductor Devices and IC's, 1998: 25

[4] Kapels H, Plikat R, Silber D. Dielectric charge traps: a new structure element for power devices. Proc IEEE Int Symp Power Semiconductor Devices and IC's, 2000: 205

[5] Li Zhaoji, Zhang Bo, Luo Xiaorong, et al. The rule of field en-

hancement for buried dielectric layer of SOI high voltage devices. IEEE International Conference on Communications Circuits and Systems, 2007: 1320

[6] Zhang Bo, Li Zhaoji, Hu Shengdong, et al. Field enhancement for dielectric layer of high-voltage devices on silicon on insulator. IEEE Trans Electron Devices, 2009, 56(10): 2327

[7] Luo Xiaorong, Zhang Bo, Li Zhaoji. A new structure and its analytical model for the electric field and breakdown voltage of SOI high voltage device with variable-*k* dielectric buried layer. Solid-State Electron, 2007, 51(5): 493

[8] Luo Xiaorong, Zhang Bo, Li Zhaoji. A novel 700 V SOI LDMOS with double-side trench. IEEE Electron Device Lett, 2007, 28(5): 422

[9] Hu Shengdong, Zhang Bo, Li Zhaoji. A new analytical model of high voltage silicon on insulator (SOI) thin film device. Chin Phys B, 2009, 18(1): 315

[10] Hu Shengdong, Zhang Bo, Li Zhaoji, et al. A new structure and its analytical model for the vertical interface electric field of partial-SOI high voltage device. Chin Phys B, 2010, 19(3): 037303

[11] Wang Wenlian, Zhang Bo, Li Zhaoji, et al. High-voltage SOI SJ-LDMOS with a nondepletion compensation layer. IEEE Electron Device Lett, 2009, 30(1): 69

[12] Park J M, Grasser T, Kosina H, et al. A numerical study of partial-SOI LDMOSFETs. Solid-State Electron, 2003, 47(2): 275

[13] Tadikonda R, Hardikar S, Narayanan E M S. Realizing high breakdown voltage (> 600 V) in partial SOI technology. Solid-State Electron, 2004, 48(9): 1655

[14] Duan Baoxing, Zhang Bo, Li Zhaoji. A new partial SOI power device structure with P-type buried layer. Solid-State Electron, 2005, 49(12): 1965

[15] Sze S M, Ng K K. Physics of semiconductor devices. 3rd ed. John Wiley and Sons, Inc., 2007

[16] TMA MEDICI 4.2. Palo Alto CA: Technology Modeling Associates Inc.