Prospects of a β-SiC based IMPATT oscillator for application in THz communication and growth of a β-SiC p–n junction on a Ge modified Si $\langle 100 \rangle$ substrate to realize THz IMPATTs

Moumita Mukherjee[1, †] and Nilratan Mazumder[2]

(1 Centre of Millimeter-Wave Semiconductor Devices and Systems, Centre of Advanced Study in Radiophysics and Electronics, University of Calcutta, Girish Vidyaratna Lane, Kolkata 700009, West Bengal, India)
(2 IERCEM Institute of Information Technology, West Bengal University of Technology, Kolkata 700017, India)

Abstract: The prospects of a p^+nn^+ cubic silicon carbide (3C-SiC/β-SiC) based IMPATT diode as a potential solid-state terahertz source is studied for the first time through a modified generalized simulation scheme. The simulation predicts that the device is capable of generating an RF power output of 63.0 W at 0.33 THz with an efficiency of 13%. The effects of parasitic series resistance on the device performance and exploitable RF power level are further simulated. The studies clearly establish the potential of 3C-SiC as a base semiconductor material for a high-power THz IMPATT device. Based on the simulation results, an attempt has been made to fabricate β-SiC based IMPATT devices in the THz region. Single crystalline, epitaxial 3C-SiC films are deposited on silicon (Si) $\langle 100 \rangle$ substrates by rapid thermal chemical vapour deposition (RTPCVD) at a temperature as low as 800 ℃ using a single precursor methylsilane, which contains Si and C atoms in the same molecule. No initial surface carbonization step is required in this method. A p–n junction with an n-type doping concentration of 4×10^{24} m^{-3} (which is similar to the simulated design data) has been grown successfully and the characterization of the grown 3C-SiC film is reported in this paper. It is found that the inclusion of Ge improves the crystal quality and reduces the surface roughness.

Key words: cubic (β)-SiC; single drift IMPATT diode; parasitic resistance; terahertz oscillation; RTPCVD growth; p–n junction formation

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1. Introduction

The terahertz (THz, 300 GHz to 10000 GHz) region is a spectral domain particularly rich in information because numerous physical mechanisms have relevant frequencies that lie in this frequency range. There is strong interest in the exploitation of the THz frequency range in virtually all fields of basic natural science (physics, chemistry, biology) as well as medicine[1]. THz finds its application in radio astronomy also. Nowadays, the potential applications are also beyond this frame with the prospects of using THz radiation for future telecommunication systems, in medical imaging and more generally in biological science. THz imaging can be employed in "homeland defence", and in weapon and contraband detection. It is one of the critical technologies for defence against suicide bombers and other terrorist activities. From the point of view of instruments, access to the terahertz spectrum is tricky owing to the lack of low-cost and compact solid-state sources. Thus research activity in the development of small THz sources has been gaining importance in recent years.

Among all of the two terminal solid-state sources, impact avalanche transit time (IMPATT) diodes are the solid-state sources with the most potential and they are widely used in transmitters, RADARs and missile seekers. The advent of ion implantation and MBE techniques has made possible the realization of IMPATT oscillators based on Si and GaAs, which can provide up to a few mW of RF power ($P_{\rm RF}$) at MM-wave frequencies. For realizing higher $P_{\rm RF}$ from a high frequency (in THz regime) IMPATT device, one should choose a semiconductor material that has a higher value of critical electric field ($E_{\rm c}$), saturated drift velocity ($v_{\rm s}$) and thermal conductivity (K), since $P_{\rm RF}$ of an IMPATT is proportional to $E_{\rm c}^2 v_{\rm s}^2$. Wide band gap semiconductors, such as SiC and GaN, have some excellent material properties that enable these materials as an automatic choice for the fabrication of high power terahertz IMPATT devices. SiC exists in a large number of polytypes which have different stacking sequences of double layers of Si and C atoms. Presently, α (6H, 4H) and β (3C)-SiC are candidate materials for SiC device fabrication. The band gap of SiC lies between 2.35 and 3.2 eV at room temperature. The electron saturation velocity ($v_{\rm s}$) in SiC is twice that in Si. This indicates that IMPATT diodes based on SiC may reach an oscillation frequency greater than 300 GHz. Moreover, these materials offer at least (i) $10E_{\rm c}$ and (ii) $3K$ in comparison to those of conventional Si, GaAs and InP. That means that SiC IMPATTs are likely to produce $400P_{\rm RF}$ more than their counterparts.

Another wide band gap semiconductor, GaN, also has promising material properties like SiC, but GaN has some disadvantages compared to SiC. The first one is that the thermal conductivity of GaN is almost one third of that in SiC. This property is especially important for high power, high frequency operation because the heat generated inside the device needs to be dissipated as quickly as possible. Growing GaN on SiC wafers increases the overall thermal conductivity but still does not reach the performance of SiC. The second important prob-

† Corresponding author. Email: mm_drdo@yahoo.com
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lem is that pure GaN wafer is not available commercially; instead, GaN wafers are grown on sapphire or SiC. Even then, thick GaN substrates are not commercially available. As a consequence, GaN wafers are more expensive than SiC wafers.

As discussed earlier, the high breakdown field and high thermal conductivity of all the polytypes of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized in SiC devices. Among all the polytypes of SiC, from the technological point of view, cubic (β)-SiC has certain advantages over hexagonal (α)-SiC. Though the small area SiC wafers are commercially available for 4H-SiC and 6H-SiC hexagonal polytypes, their cost is 1000 times higher than that of 6Si substrates. Moreover, device quality 4H-SiC and 6H-SiC wafers are produced mainly by bulk-crystallization, including a process involving a high substrate temperature (> 2000 ℃). This high temperature growth forms high density channeled defects, known as micropipes, in α-SiC. The presence of such high density defects in α-SiC is a major problem as it greatly degrades the device quality.

On the other hand, β-SiC appears as a potential candidate since it can be grown at a lower temperature. As there is no suitable substrate for the growth of β-SiC crystals, the alternative is to use Si wafers which exist with good surface crystalline quality and with large surface area free from defects. Hetero-epitaxial growth of β-SiC on Si is a possible solution to overcome the problem of micropipes present in α-SiC polytypes. Moreover, the growth of good-quality 3C-SiC epilayers on Si would make it a cheaper alternative to costly 6H-SiC and 4H-SiC commercial epilayers and also makes it compatible with present Si technology. Additionally, the β-SiC/Si heterostructures hold the promise of developing novel SiC/Si heterojunction devices and monolithic circuits combining SiC and Si devices. Also, the temperature coefficient of the breakdown voltage of a p–n junction formed in 3C-SiC shows a positive value. A positive temperature coefficient is highly desirable to prevent runaway if devices reach the breakdown point. This indicates that IMPATT diodes can possibly be made with β-SiC, because the positive temperature coefficient is the direct result of an impact ionization process, which is required for the IMPATT diodes.

Despite all of its advantages, the prospect of 3C-SiC as a base material for IMPATT fabrication has still not been explored. For the first time, the authors have simulated a 3C-SiC based single drift flat profile (p^+nn^+) IMPATT diode and the corresponding DC and terahertz characteristics of the device are also reported here. The authors have deposited p and n type 3C-SiC epilayers on a Si substrate by a rapid thermal processing chemical vapour deposition (RTPCVD) technique at a growth temperature as low as 800 ℃. A p–n junction has been grown successfully and the characterization of the grown 3C-SiC film has been completed. The corresponding results are reported here.

2. Simulation methodololy

A single drift (p^+nn^+) 3C-SiC diode is designed for operation in the THz regime. Poisson's equation, the carrier continuity equation and the space charge determining equation[2] for the diode are used for the DC analysis. A modified double iterative computer method, initiated from the position of field maximum, has been used to solve simultaneously the diode equations under the condition of DC avalanche breakdown[2, 3]. When the usual boundary conditions are satisfied at the edges of the depletion layer through the computing process, the final solution for the DC electric field profile and carrier current profile are obtained. The present analysis is made accurate by incorporating realistic field dependent material parameters in β-SiC, i.e. field dependent carrier ionization rate data, saturated drift velocities and mobilities of charge carriers in 3C-SiC[4], in the simulation program. The junction temperature is kept fixed at 300 K. The doping profile at the nn^+ interface is considered to be complimentary error function profiles and the doping profile near the metallurgical junction is taken to be an exponential function[2, 3]. The effects of diffusion and mobile space charge have been incorporated into the analysis.

Table 1. Design parameters of a 3C-SiC IMPATT at 0.3 THz.

Diode type	Flat epilayer doping conc. (n region)	Width of the flat epilayer (n region)	Current density
$p^+n\,n^+$	4.0×10^{24} m^{-3}	0.25 μm	2.0×10^9 A/m^2

The above mentioned DC method of simulation analysis is used to optimize the diode structure for the particular design frequency. The width and background doping concentration of the n-region have been designed to obtain the optimum punch-through factor and a narrow avalanche region of the diode which would lead to high conversion efficiency. The device dimensions, doping and current densities for the diode (see Table 1) are optimized for operation at around 0.3 THz, after several computer runs.

The DC data obtained from the final solution of the optimized diode are taken as input for the high-frequency (THz) AC analysis. A highly generalized and modified double iterative computer method[5], which is free from any numerical instability, has been used to solve two second order partial differential equations involving diode resistivity ($R(x)$) and reactance ($X(x)$) per unit length, simultaneously, subject to appropriate boundary conditions[2, 3] at the edges of the depletion layer. The edges of the depletion layer of the diode are accurately pre-determined by corresponding DC analysis. Iteration over the initial choice of the $R(x,\omega)$ and $X(x,\omega)$ at the left edge of the depletion layer are carried out through the process of computation until the boundary conditions are satisfied at the right edge of the depletion layer of the diode. The spatial variation of $R(x)$ and $X(x)$ in the depletion region are obtained from the final solution. The diode resistance $Z_{\rm R}$ and reactance ($Z_{\rm X}$) are obtained by integrating $R(x)$ and $X(x)$ profiles over the depletion layer width. The diode impedance Z is given by

$$Z(\omega)=\int_0^{W_{\rm n}} X(x,\omega){\rm d}x=-Z_{\rm R}+{\rm j}Z_{\rm X}. \tag{1}$$

The diode admittance is expressed as

$$\begin{cases} Y=1/Z=-G+{\rm j}B=1/(-Z_{\rm R}+{\rm j}Z_{\rm X}),\\ -G=-Z_{\rm R}/[(Z_{\rm R})^2+(Z_{\rm X})^2],\\ B=-Z_{\rm X}/[(Z_{\rm R})^2+(Z_{\rm X})^2]. \end{cases} \tag{2}$$

where $-G$ and B are functions of RF voltage (V_{RF}) and frequency (ω) such that the steady state condition for oscillation is given by[6]

$$g(\omega) = -G(\omega) - [B(\omega)]^2 R_S(\omega), \quad (3)$$

where g is load conductance. $-G$, B, g are normalized to the area of the diode. The relation provides minimum uncertainty in g at low power oscillation threshold. The authors have evaluated R_S from the admittance characteristics using the realistic analysis of Gummel–Blue[7] and Alderstein *et al*.[6] without any drastic assumption. V_{RF} (amplitude of the RF swing) is taken as $V_B/2$, assuming a 50% modulation of the breakdown voltage V_B. For such a small value of V_{RF}, R_S can be calculated by considering the value of g nearly equal to the diode conductance (G) at resonance.

At a given bias current density, the peak frequency (f_P) is the frequency at which the negative conductance of the diode is a maximum and the quality factor is a minimum. At f_P, the maximum RF power (P_{RF}) from the device is obtained as[8]

$$P_{RF} = (V_{RF}^2 G_P) A/2. \quad (4)$$

The peak negative conductance at the optimum frequency ($-G_p$) is normalized to the area of the diode. The diode area is assumed to be 10^{-10} m^2 for the present analysis. The effect of series resistance (R_S) on P_{RF} is also considered. The space-step for the present simulation technique has been taken as $\sim 10^{-10}$ m. The validity of this simulation method was found to be quite satisfactory for hexagonal SiC and GaN, as well as InP based millimeter wave and sub-millimeter wave (THz) IMPATTs[2, 3, 9–11].

3. Experimental technique

Due to a lack of suitable 3C-SiC substrates, 3C-SiC has been grown on Si (100) 1–10 Ω· cm, p^+-type substrates (diameter 100 mm). A common method to grow a hetero-epitaxial 3C-SiC (β-SiC) layer on a Si substrate is to mix together a carbon based precursor with a Si based gas in a chemical vapor deposition reactor (CVD). This method requires a high growth temperature (> 1300 ℃). Thus this process requires control of very high temperature. Moreover, it is often difficult to control two separate precursors for silicon and carbon. In addition, the use of a separate precursor in the growth of SiC thin film may results in a small departure from stoichiometry in the films, leading to point defects, which degrade the device characteristics. The rapid thermal processing chemical vapor deposition (RTCVD/RTPCVD) technique is an alternative to conventional CVD for the growth of hetero-structures. SiC epilayers are deposited onto Si substrates by the RTPCVD technique at a growth temperature as low as 800 ℃. A single gas precursor, "methylsilane" ($SiCH_3H_3$), with a Si : C ratio of 1 : 1 has been used for SiC deposition. Boron has been used to obtain p-type β-SiC, while phosphorus is used as an n-type dopant in β-SiC. The boron and phosphorus incorporation are accomplished by introducing diborane and phosphine precursors, respectively. The substrates are cleaned thoroughly by adopting the PIRANHA cleaning method. The substrates are then dipped in dilute HF for 30 s, followed by rinsing in DI water, before they are transferred to the deposition chamber. The chamber pressure has been pumped down to 10^{-4} Torr. The temperature is ramped-up to a growth temperature of 50 ℃/s. *In situ* cleaning of the Si substrate has been carried out at 800 ℃ with flowing H_2 (flow rate: 1 lpm) in the growth chamber of the RTPCVD system. This is done to remove any residual surface oxide. Growth of p-type 3C-SiC film is carried out for 2 h at growth temperature with 6 sccm MMS, 1 sccm of diborane and 1 lpm H_2 at a pressure of 1 Torr. Growth of n-type 3C-SiC film is carried out for 2 h at growth temperature with 6 sccm MMS, 5 sccm of phosphine and 1 lpm H_2 at a pressure of 1 Torr.

Due to the large lattice mismatch ($\approx$ 20%) and the large difference in the thermal expansion coefficient ($\approx$ 8%), it has been difficult to obtain a coherent interface between the two cubic (3C-SiC and Si) materials. A significant part of the 20% mismatch in the lattice constants can be released by the formation of a dislocation network. However, the mismatch in the thermal expansion coefficients of SiC and Si introduces an additional strain in the system during the cooling process after growth. This strain results in a strong degradation of the layer properties and a wafer warp age, limiting the use of SiC/Si hetero-structures for device applications and as a pseudo-substrate for the deposition of group III-nitrides[12]. All of these defects could generate high leakage currents in the p–n junction.

Carbonization of Si is the most common method for improving the quality of SiC/Si interfaces before subsequent epitaxial growth. However, in these "carbon-modified" surfaces, the misfit strain relieved by the formed misfit dislocation network is not able to achieve a fully relaxed 3C-SiC thin layer (normally in tension)[13]. The other approach is the use of modified Si substrates. A theory of misfit-induced structural defects at semiconductor interfaces suggests that in hetero-structures, where a large misfit exists, the insertion of a transition layer aiming to obtain high-quality hetero-structures might be useful[14]. The use of germanium (Ge) during CVD growth of SiC (at 1000 ℃) on Si was reported by Mitchell *et al*.[15], and he observed that SiC films grown on Si with the presence of Ge resulted in changes in surface morphology. Adding Ge in the form of GeH_4 to the reactant gases in a MOCVD reactor allows the crystalline growth of 3C-SiC on Si substrates for a low growth temperature of 1000 ℃[16]. In order to improve the crystal quality and to reduce the high leakage currents, the authors have carried out growth of 3C-SiC p–n junctions on a Ge-modified Si (100) substrate. Germane (GeH_4) gas was introduced into the chamber at temperatures varying from 550 to 400 ℃ and was flowed for times varying from 50 to 20 min with flowing H_2 (flow rate: 1 lpm) in the growth chamber of the RTPCVD system. As a result, Ge layers (thickness 30–100 nm, determined by ellipsometry measurement) were formed on the Si substrate. Doped SiC layers were grown on the Ge layer following the same recipe as described earlier.

4. Results and discussions

4.1. Simulation results

The design parameters of a 3C-SiC based IMPATT diode are summarized in Table 1. The diode has been optimized for low punch-through conditions. Figure 1 shows the electric field profiles within the depletion layer of the p^+nn^+ terahertz IMPATT diode for the same bias current density (2×10^9 A/m^2)

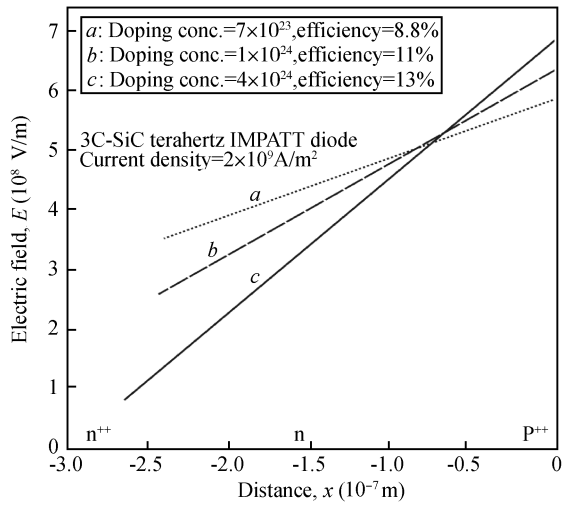


Fig. 1. Electric field profiles of β-SiC IMPATTs for various doping concentrations. A negative sign indicates the n-region of the diode.

Table 2. MM-wave properties of 3C-SiC SDR IMPATT diode at 0.3 THz.

Parameter	Value
E_m	6.5×10^8 V/m
V_B	120.0 V
H	13.0%
f_a	0.220 THz
f_p	0.330 THz
$-G_p$	350.0×10^6 S/m^2
$-Q_p$	0.96
P_{RF}	63.0 W

and a different active layer background doping concentration ranging from 0.7×10^{24} to 4×10^{24} m^{-3}. The figure clearly indicates that the decrease in n-layer doping concentration increases the punch-through and decreases the maximum breakdown filed. The corresponding efficiencies of the diodes at different doping densities are also shown in Figure 1. The efficiency (13%) is found to be higher for the diode structure showing lower punch through (background doping density = 4×10^{24} m^{-3}). The low punch through diode is found to be most efficient in the THz region. Thus, the DC and high frequency properties of the optimized low punch through diode are further simulated and the corresponding results are summarized in Table 2. The diode admittance plots, with and without R_S, are shown in Fig. 2 and they indicate that the diode negative conductance at 0.33 THz (peak operating frequency) will be 353.0×10^6 S/m^2. It is also observed in Fig. 2 that in the presence of R_S, the device negative conductance decreases significantly. The RF power output for the optimized device is calculated from Eq. (3) and is found to be 63.0 W at 0.33 THz.

The parasitic series resistance for the 3C-SiC SDR diode is determined from Eq. (3) and its effect on the RF power is shown in Fig. 3. The values of load conductance (g), negative resistance and positive series resistance are summarized in Table 3. It is evident from Fig. 3 as well as from Table 3 that due to the presence of R_S, the CW power decreases by ~9%. The value of total negative resistance ($-Z_R$) is found to be much higher than R_S at 0.3 THz (Table 3), which is an essential condition for diode oscillation.

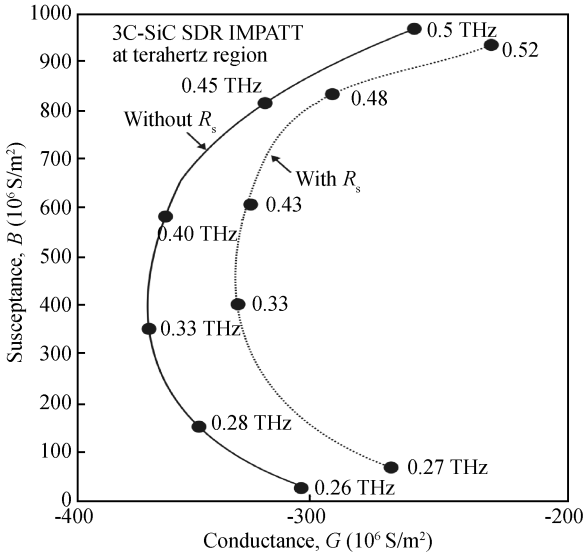


Fig. 2. Admittance characteristic of a β-SiC IMPATT in the THz region.

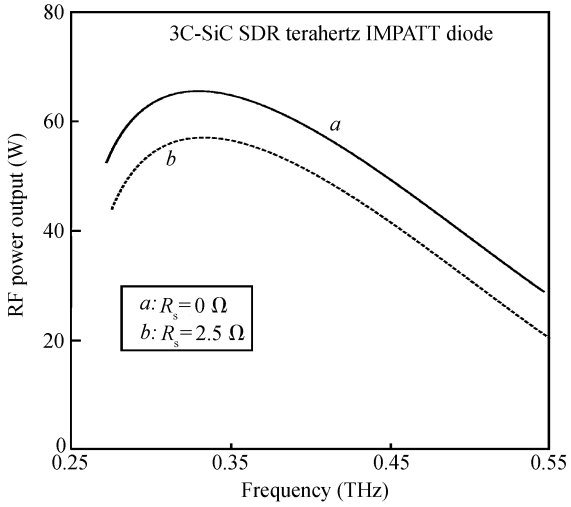


Fig. 3. Effect of parasitic resistance on RF power output of a β-SiC IMPATT.

Table 3. Parasitic series resistance (R_S) at oscillation threshold (frequency = 0.300 THz) of 3C-SiC SDR THz IMPATT. Current density = 2.0×10^9 A/m^2.

Parameter	Value
Diode conductance, $-G$	340.0×10^6 S/m^2
Diode susceptance, B	200.0×10^6 S/m^2
Diode total negative resistance, Z_R	21.85 Ω
Parasitic series resistance, R_S	2.5 Ω
Expected load conductance, g	330.0×10^6 S/m^2

Figure 4 shows the negative resistivity profile at the peak frequency for the optimized 3C-SiC SDR IMPATT device, with and without R_S. Negative resistivity profiles give a physical insight into the region of the depletion layer that contributes to the RF power. These figures show that for both the diode structures, the profiles exhibit negative resistivity peaks in the

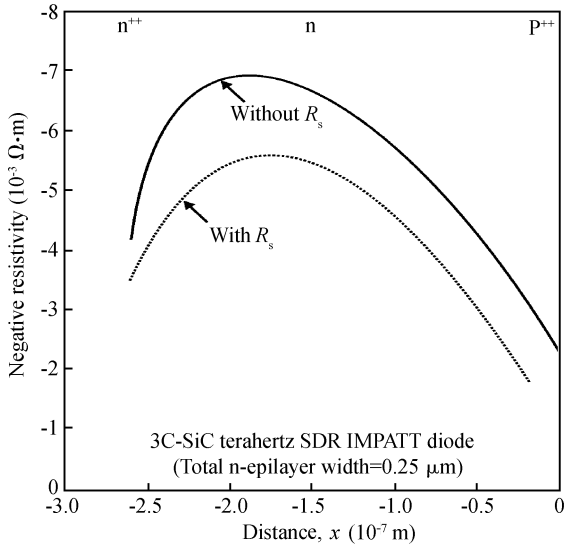


Fig. 4. Resistivity profile of a β-SiC IMPATT in the THz region.

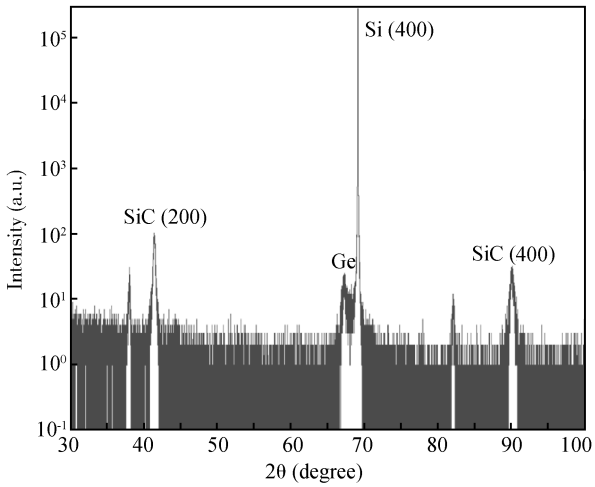


Fig. 5. XRD spectrum of a β-SiC grown on a Ge-modified Si ⟨100⟩ substrate.

middle of the drift layer with dips in the avalanche layer close to the junction. The peak of the profile indicates that the drift region contributes a major role to the higher negative resistance of the diode.

4.2. Characterization of grown (doped) β-SiC p–n junction

Ellipsometry measurement reveals that a Ge layer of thickness 300–1000 Å is formed on the Si substrate. The thickness of the SiC layer, as measured by an ellipsometer, is found to vary from 0.72 to 0.80 μm. The crystallinity of the doped films, studied by X-ray diffraction (XRD), reveals that the SiC layers are perfectly crystalline (Fig. 5). The peaks represent reflections from (left to right) Si (200), SiC (200), Si (400) and SiC (400) crystal planes. A Ge peak close to the SiC (400) peak is also observed. The angular positions of SiC (200), Si (400) and SiC (400) planes, as shown in the XRD spectrum, match closely the corresponding angular position found by other researchers. The AFM pictures of the samples are shown in Figs. 6(a) and 6(b). Figure 6(a) reveals that there are large

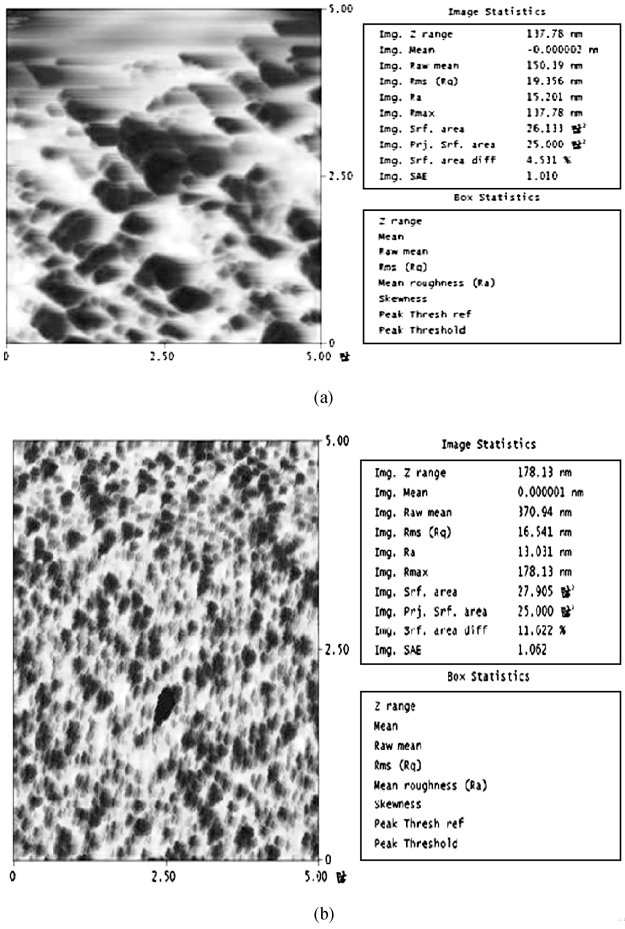
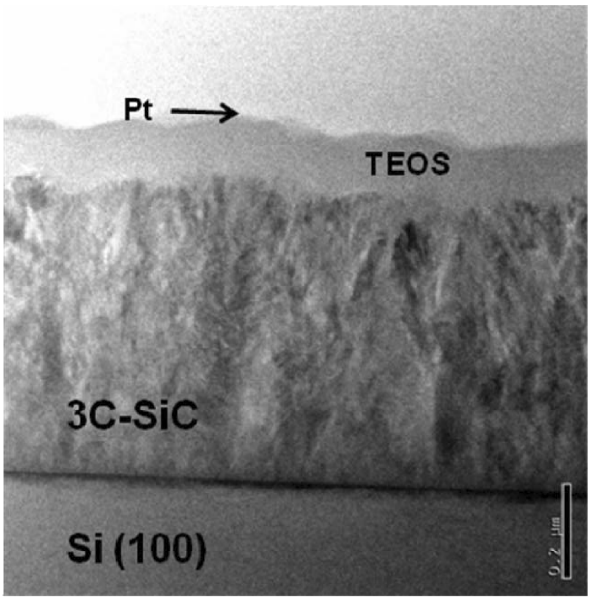
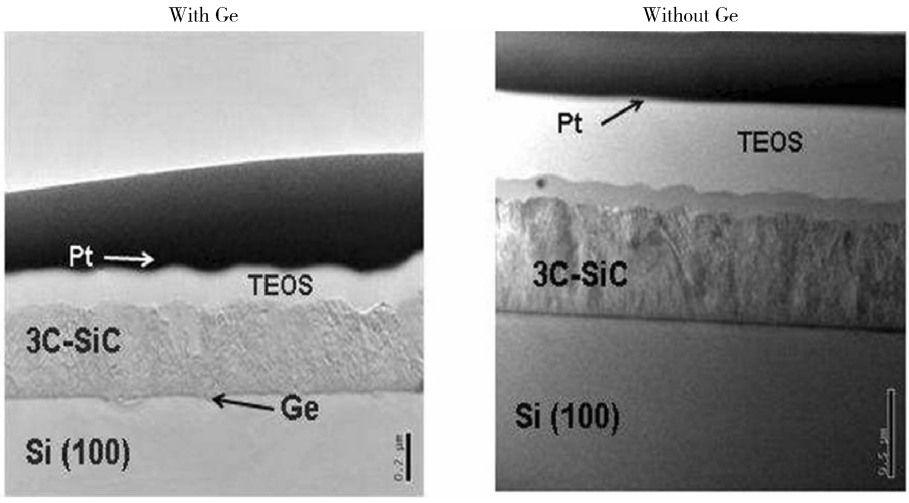


Fig. 6. AFM picture taken from a sample (a) without or (b) with Ge pre-deposition.

spots that are not visible, but these regions are visible for an SiC layer grown on a Ge modified Si substrate (Fig. 6(b)). Such large spots are indicative for holes or deeper lying parts on the SiC surface. Such features are connected with voids beneath the SiC layers. Therefore, in the case of Ge pre-deposition, void formation is suppressed. Consequently, the surface roughness of doped SiC film is found to be 16.0 nm, which is lower than the surface roughness of the film grown on a Si surface without Ge pre-deposition. Transmission electron microscopy (TEM) measurement of the sample without Ge incorporation is shown in Fig. 7(a). To improve the contrast of the TEM picture, the scale of the same sample in TEM mode is changed and shown in Fig. 7(b). In Fig. 7(b), a comparison is made between TEM measurements of samples with and without Ge incorporation. It is found that there is a noticeable improvement in the quality of the SiC layer (Fig. 7(b)). Scanning TEM of samples with Ge and without Ge is shown in Fig. 8. It can be observed that the Ge layer displaces a better contrast under STEM mode, as shown in Fig. 8. Hence, it is expected that the Ge layer acts as a barrier between the Si/SiC interfaces and prevents out-diffusion of the substrate Si into the SiC films. These improvements are likely to reduce the leakage current flowing through the p–n junction. From Fig. 9 it is observed that the Ge-layer displays a better contrast under STEM mode (b). Figure 10 shows the SIMS profiling of doped 3C-SiC film on Si. It is evident that a clear p–n junction with a doping con-

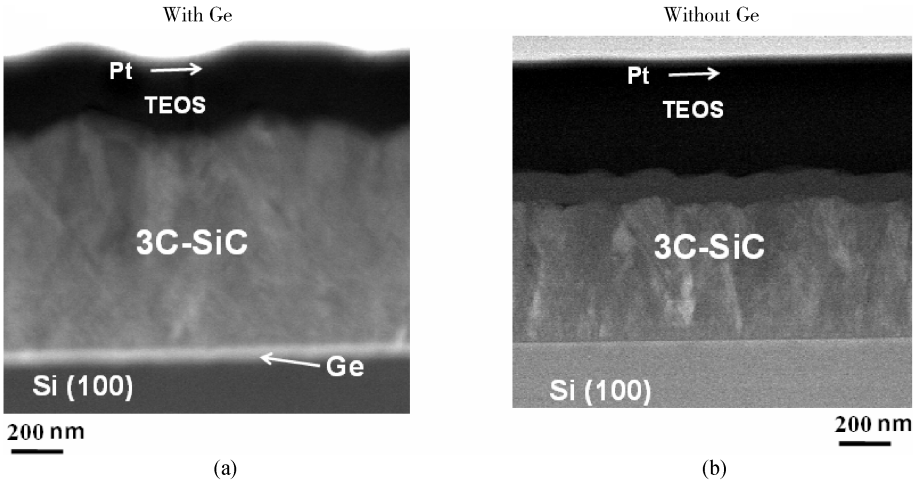


(a)



(b)

Fig. 7. (a) TEM micrograph of a sample without Ge. (b) TEM micrographs of samples with Ge and without Ge.



(a) (b)

Fig. 8. Scanning TEM of samples (a) with Ge and (b) without Ge. The arrow in Fig. 8(a) indicates a Ge layer formed at the interface between Si and 3C-SiC.

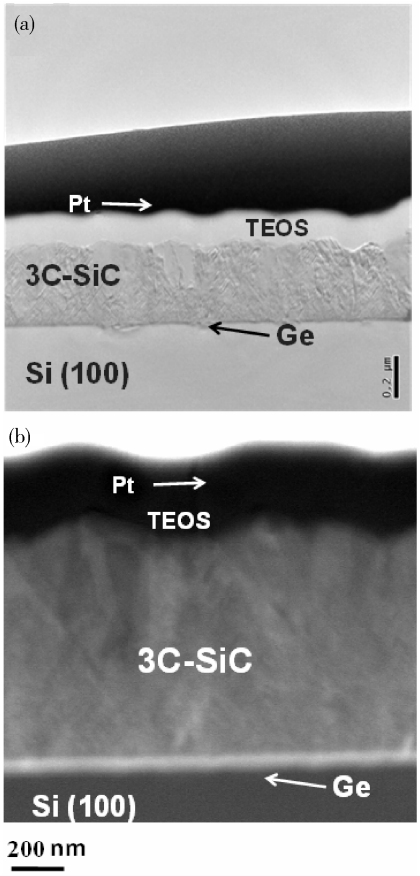


Fig. 9. 3C-SiC on Ge-modified Si. (a) TEM and (b) scanning TEM analysis. The Ge layer displays better contrast under STEM mode (Fig. 9 (b)).

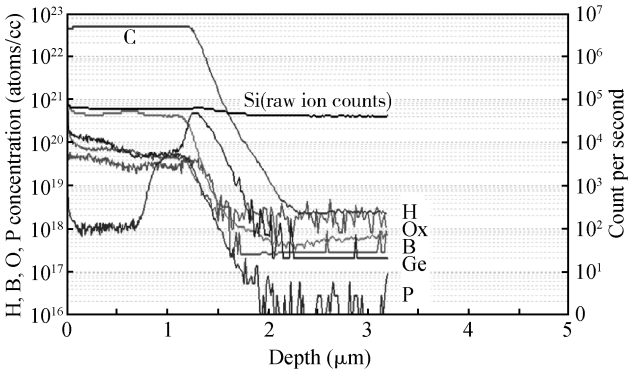


Fig. 10. SIMS profile of a β-SiC grown on a Ge-modified Si ⟨100⟩ substrate.

centration of 4.5×10^{24} atoms/m^3 is formed, which is very close to the simulation data. The p- and n-layer thicknesses are (in μm) 1.38 and 0.472, respectively. The location of the p–n junction is found to be 0.99 μm. The location of the Ge layer is 1.28 μm.

5. Conclusion

To the best of our knowledge, this is the first report on simulation studies of a β-SiC THz IMPATT diode. It may be concluded that the simulation results reported here reveal the potential of β-SiC IMPATT as a high-power THz source, and the design may be used for experimental realization of a 3C-SiC THz IMPATT. Based on the design, the authors have also successfully grown a β-SiC p–n junction on Ge modified Si ⟨100⟩ substrate. Efforts have been made to reduce the lattice mismatch at the Si/SiC interface by incorporating Ge. The preliminary results are encouraging and need further improvement to obtain 3C-SiC based IMPATTs with minimum reverse leakage current. Additional results will be the subject of another paper.

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References

[1] Siegel P H. Terahertz technology. IEEE Trans Microw Theory Tech, 2002, 50: 910
[2] Mukherjee M, Mazumder N, Roy S K, et al. GaN IMPATT diode: a photosensitive high power terahertz source. Semicond Sci Technol, 2007, 22: 1258
[3] Mukherjee M, Mazumder N, Roy S K. Photosensitivity analysis of gallium nitride and silicon carbide terahertz IMPATT oscillators: comparison on theoretical reliability and study on experimental feasibility. IEEE Trans Device Mater Reliab, 2008, 8: 608
[4] http://www.ioffe.ru/SVA/NSM/Semicond/SiC
[5] Roy S K, Banerjee J P, Pati S P. A computer analysis of the distribution of high frequency negative resistance in the depletion layer of IMPATT diodes. Proc 4th Conf Num Anal Semiconductor Devices, Dublin, Boole, 1985: 494
[6] Adlerstein M G, Holway L H, Chu S L. Measurement of series resistance in IMPATT diodes. IEEE Trans Electron Devices, 1983, ED-30: 179
[7] Gummel H K, Blue J L. A small signal theory of avalanche noise in IMPATT diodes. IEEE Trans Electron Devices, 1967,14: 569
[8] Eisele H, Haddad G I. Active microwave devices. In: Sze S M, ed. Microwave semiconductor device physics. New York: Wiley, 1997: 343
[9] Mukherjee M, Mazumder N, Dasgupta A. Radiation effects on a high efficiency double drift region 4H-SiC terahertz IMPATT diode. Proc IEEE International Conference on Microwave and Millimeterwave Techniques, 2007: 655
[10] Mukherjee M, Mazumder N, Dasgupta A. Simulation experiment on optical modulation of 4H-SiC millimeter-wave high power IMPATT oscillator. Jr of European Microwave Association, 2008, 4: 276
[11] Mukherjee M, Mazumder N, Roy S K, et al. Terahertz frequency performance of double drift IMPATT diodes based on opto-sensitive semiconductors. Proc IEEE MTTs Asia Pacific Microwave Conference, Bangkok, Thailand, December 2007: 1077

[12] Nishiguchi T, Nakamura M, Nishio K, et al. Heteroepitaxial growth of (111) 3C-SiC on well-lattice-matched (110) Si substrates by chemical vapor deposition. Appl Phys Lett, 2004, 84: 3082
[13] Morales F M, Molina S I, D Araújo, et al. SiC voids, mosaic microstructure and dislocations distribution in Si carbonized layers. Diamond and Rel Mater, 2003, 12: 1227
[14] Masri P. Elasticity-based theory of misfit-induced structural defects at semiconductor interfaces. Phys Rev B, 1995, 52 : 16627
[15] Mitchell S, Spencer M G, Wongchotigul K. Germanium as a possible surfactant for growth of beta silicon carbide on silicon substrates. Mater Sci Forum, 1998, 264–268: 231
[16] Sarney W L, Salamanca-Riba S, Zhou P, et al. Role of Ge on film quality of SiC grown on Si. J Appl Phys, 2002, 91: 668