A thick SOI UVLD LIGBT on partial membrane*

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Abstract: A thick SOI LIGBT structure with a combination of uniform and variation in lateral doping profiles (UVLD) on partial membrane (UVLD PM LIGBT) is proposed. The silicon substrate under the drift region is selectively etched to remove the charge beneath the buried oxide so that the potential lines can release below the membrane, resulting in an enhanced breakdown voltage. Moreover, the thick SOI LIGBT with the advantage of a large current flowing and a thermal diffusing area achieves a strong current carrying capability and a low junction temperature. The current carrying capability ($V_{\rm Anode}$ = 6 V, $V_{\rm Gate}$ = 15 V) increases by 16% and the maximal junction temperature (1 mW/μm) decreases by 30 K in comparison with that of a conventional thin SOI structure.

Key words: SOI LIGBT; UVLD; partial membrane; current carrying capability; junction temperature
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1. Introduction

Silicon-on-insulator (SOI) technology offers tremendous advantages over bulk Si technology, such as fast speed, superior isolation, high integration density and low loss. However, SOI devices suffer from low breakdown voltage and have an intrinsic self-heating effect (SHE), which constrains its application. In order to overcome these issues, scholars have done much research[1−6]; a thick silicon membrane LIGBT PowerBrane™ device was proposed by Trajkovic *et al*.[7]; a UVLD PSOI LDMOS was proposed by Tadikonda *et al*.[8]; a 3D-Resurf (super-junction) bipolar device in membrane was proposed by Udrea *et al*.[9]; and a double gate LIGBT on partial membrane was proposed by Luo *et al*.[10].

In this paper, a thick SOI UVLD PM LIGBT structure with an alleviated self-heating effect and enhanced current carrying capability is proposed, and then on-state and thermal characteristics are analyzed.

2. Device structure and on-state characteristics

A cross-section of the UVLD PM LIGBT structure and doping profile of the drift region are shown in Fig. 1, where the Si substrate under the drift region is selectively etched, and a buried oxide layer is used for supporting the high voltage and also used as an effective etch-stop during deep reactive ion etch. $L_{\rm v}$ and $L_{\rm u}$ are the length of the drift region with variation doping and uniform doping profile, respectively. $T_{\rm I}$ and $T_{\rm S}$ represent the thickness of the buried and SOI layer. $L_{\rm sub}$ represents the length of the Si substrate. For the thin SOI UVLD PM LIGBT, the doping profile increases from the starting concentration ($N_{\rm S}$) to the ending concentration ($N_{\rm E0}$) with a concentration gradient (ΔN) of 3×10^{15} in the VLD section, and it keeps the same value ($N_{\rm u0}$) in the uniform section. In contrast, the doping profile increases from the starting concentration ($N_{\rm S}$) to the ending concentration ($N_{\rm E1}$) with a concentration gradient (ΔN) of 1×10^{15} in the VLD section and keeps the same value ($N_{\rm u1}$) in the uniform section for the thick SOI structure. Apparently, the thin SOI structure has a three times larger concentration gradient than the thick SOI counterpart, whilst a larger uniform doping profile in the uniform section ($N_{\rm u0} > N_{\rm u1}$) is adopted. The simulation results in this paper are obtained by MEDICI and the key structure parameters used in the simulation are listed in Table 1.

Table 1. Key structure parameters in the simulation.

Parameter	Thick SOI	Thin SOI
$L_{\rm d}$ (μm)	20	20
$T_{\rm S}$ (μm)	1.5	0.5
$T_{\rm I}$ (μm)	3	3
$T_{\rm sub}$ (μm)	10	10
$G_{\rm ox}$ (nm)	100	100
$L_{\rm sub}$ (μm)	13	13
$L_{\rm v}$ (μm)	10	10
$L_{\rm u}$ (μm)	10	10

From Fig. 2, we can see that the thick SOI structure has a higher on-state current density than the thin SOI structure because the current flowing area becomes wider and can accommodate more drift charge, which performs better current character with increasing the thickness of SOI layer. Figure 3 gives the flow line distribution.

3. Blocking and thermal characteristics

The surface field distribution of thick SOI UVLD PM LIGBT is compared with the thin SOI counterpart (Fig. 4). It

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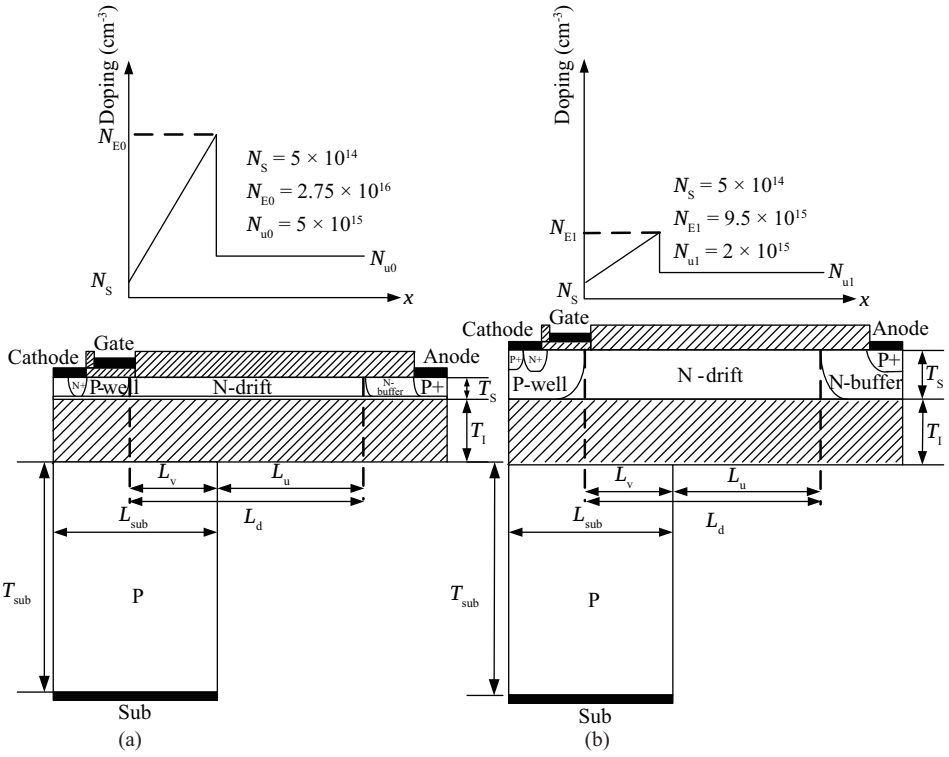

Fig. 1. (a) Thin SOI and (b) thick SOI UVLD PM LIGBT structure and doping profile of the drift region.

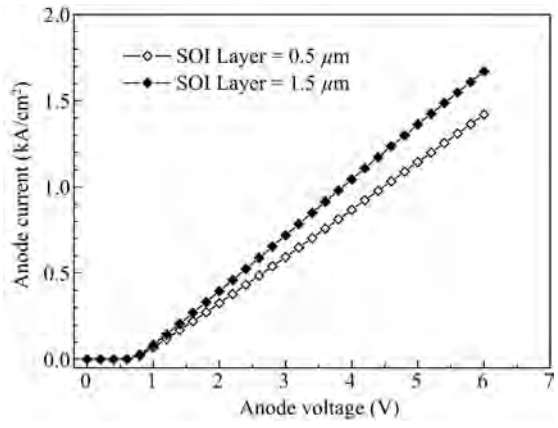

Fig. 2. On-state performances of thin and thick SOI UVLD PM LIGBT with L_v = 10 μm, V_{Gate} = 15 V.

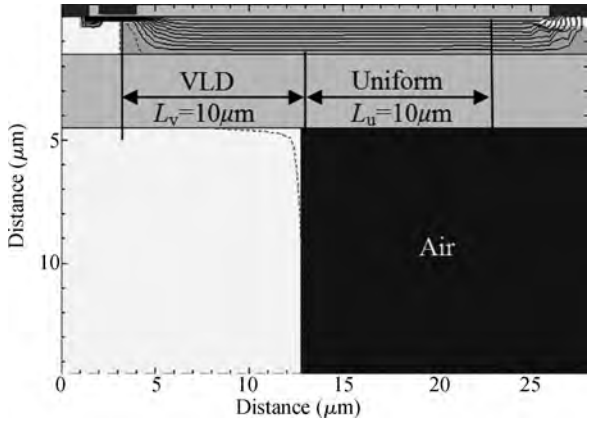

Fig. 3. Flow line distribution (V_{Anode} = 6 V, V_{Gate} = 15 V, I_{Anode} = 2.5 $\times 10^{-5}$ A/μm).

can be clearly seen that the thick SOI structure enhanced the electric field of the anode side and weakened the cathode side because of a milder doping profile. The surface field is uniformly distributed due to the linear doping profile portion in the drift region, which increases the avalanche breakdown voltage (BV) and reduces the specific on-resistance ($R_{on,sp}$). The influence of L_v on BV as well as $R_{on,sp}$ for thin and thick SOI UVLD PM LIGBT is explored and the results are plotted in Fig. 5. It can be concluded from Fig. 5 that with the increase in L_v, the breakdown voltage and specific on-resistance demonstrate an approximately linear increase phenomenon both for thin and thick SOI structures.

The thermal characteristics of thick SOI UVLD PM LIGBT were explored and compared with the thin SOI structure and its uniform doped drift region counterpart. The thermal flow is directed away from the membrane area through a silicon pillar, to which the package heat-sink is attached. The bottom of the substrate is held at 300 K for all simulations. The self-heating effect is drastically reduced, as shown in Fig. 6, as the thickness of the membrane is two times larger than the thin SOI. The temperature increases from cathode to anode because the thermal conductivity of silicon is better than that of air. The temperature increases from 378 to 448 K, 403 to 425 K, and 373 to 400 K, respectively, in Figs. 6(a), 6(b) and 6(d), from which we can draw the conclusion that the thickness of the SOI layer (T_S) and length of the silicon pillar (L_v) have a significant influence on the thermal characteristics of the UVLD PM LIGBT. The temperature of the thick SOI is lower than that of the thin SOI structure due to the longer silicon pillar and the thicker SOI layer. The curves of the junction temperature versus the power for three devices are illustrated in Fig.

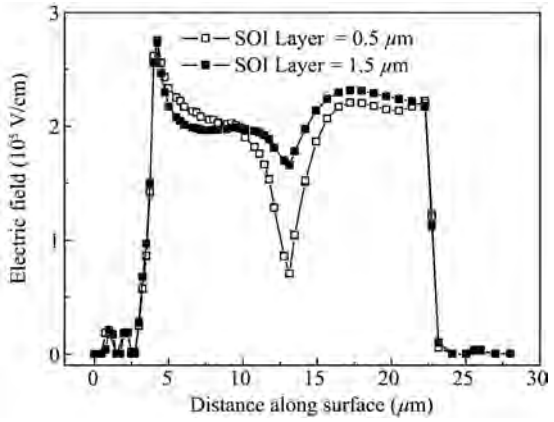

Fig. 4. Optimized surface electric field distribution of thin and thick SOI UVLD PM LIGBT.

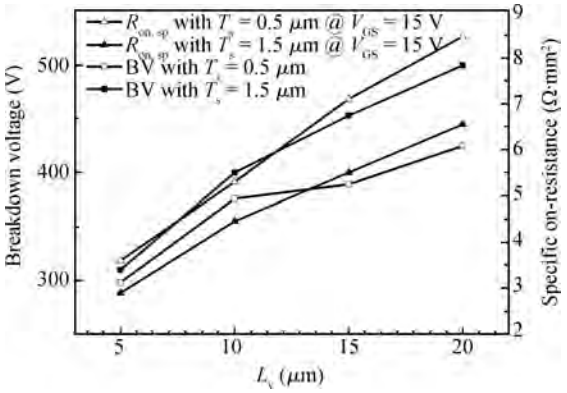

Fig. 5. Influences of $L_{\rm V}$ on BV and $R_{\rm on,sp}$ for thin and thick SOI UVLD PM LIGBT (keeping other parameters unchanged).

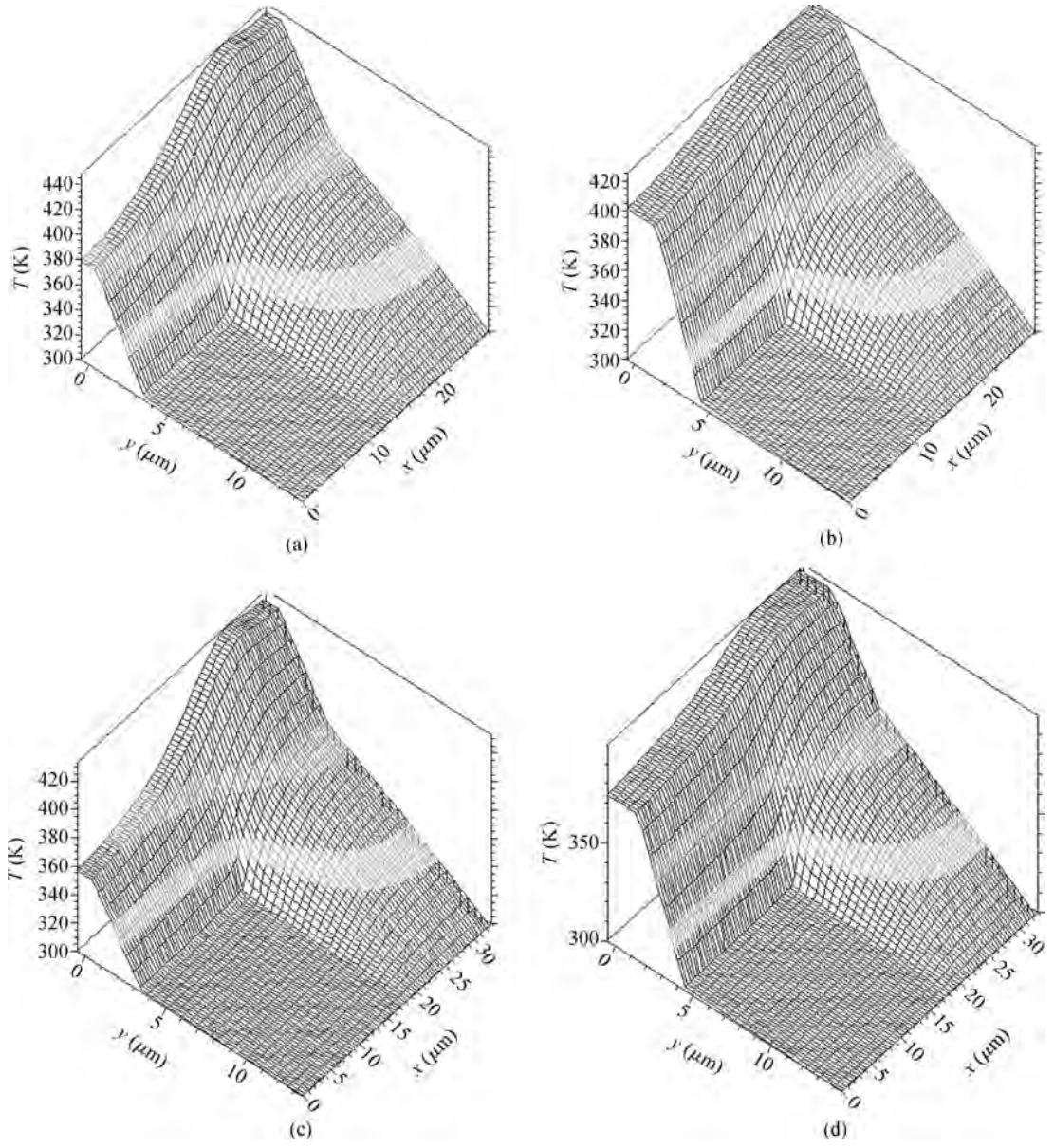

Fig. 6. Thermal characteristics of thin and thick SOI UVLD PM LIGBT with varied $L_{\rm V}$. (a), (c) $T_{\rm S} = 0.5\ \mu$m, $L_{\rm V} = 10, 15\ \mu$m. (b), (d) $T_{\rm S} = 1.5\ \mu$m, $L_{\rm V} = 10, 15\ \mu$m.

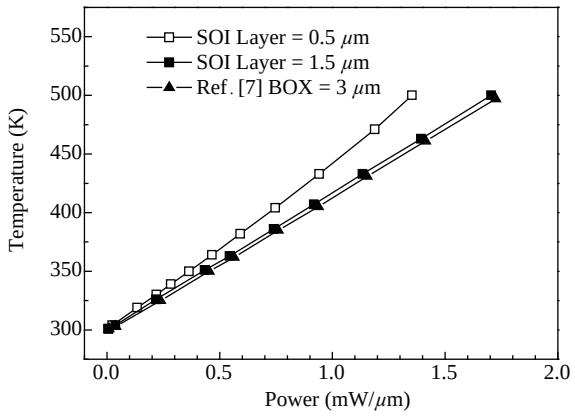

Fig. 7. Junction temperature versus power of the thin and thick SOI UVLD PM LIGBT.

Table 2. BV and $R_{on,sp}$ comparison.

Parameter	Ref. [7]	This paper	Percent
BV	319 V	400 V	↑ 25%
$R_{on,sp}$	25 Ω·mm^2	4.35 Ω·mm^2	↓ 82.6%

7. It can be clearly seen that the maximal junction temperature for the thick and thin SOI structures increases from 300 to 460, 500 K while power increases from 0 to 1.42 mW/μm and 1.35 mW/μm, respectively, decreases by 30 K at a power of 1 mW/μm. A comparison of BV and $R_{on,sp}$ is given in Table 2. The BV improves from 319 to 400 V and $R_{on,sp}$ decreases from 25 to 4.35 Ω·mm^2, improving by 25.4% and 82.6%, respectively, in comparison with Ref. [7] while not clearly deteriorating the thermal characteristics.

4. Conclusion

In this paper, a thick SOI UVLD PM LIGBT structure with increased current density and enhanced power density is proposed. The simulation results indicate that the current density ($V_{Anode} = 6$ V, $V_{Gate} = 15$ V) increases by 16% and the maximal junction temperature (1 mW/μm) decreases by 30 K in comparison with that of the thin SOI structure. The excellent device performances make the proposed UVLD PM LIGBT a promising candidate for power electronic applications.

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