An InGaAs/InP 40 GHz CML static frequency divider

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Abstract: Static frequency dividers are widely used as a circuit performance benchmark or figure-of-merit indicator to gauge a particular device technology's ability to implement high speed digital and integrated high performance mixed-signal circuits. We report a 2 : 1 static frequency divider in InGaAs/InP heterojunction bipolar transistor technology. This is the first InP based digital integrated circuit ever reported on the mainland of China. The divider is implemented in differential current mode logic (CML) with 30 transistors. The circuit operated at a peak clock frequency of 40 GHz and dissipated 650 mW from a single –5 V supply.

Key words: InP; DHBT; static frequency divider
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1. Introduction

In recent years, InP based double heterojunction bipolar transistors (DHBT) have been aggressively pursued because of their superior material properties[1]. Efforts to aggressively scale InP HBTs to submicron features vertically and laterally has resulted in processes intended to produce high-yield circuits. Applications for these devices include mixed signal ICs for digital radar and advanced communication systems[2]. This is demonstrated by the increased value of small signal unity current gain f_t and unity power gain f_{max} that InP devices possess at a given scaling generation[3, 4]. They are of limited value in predicting the speed of logic, mixed-signal, or optical transmission ICs. Static frequency dividers are critical functional elements in a variety of digital and microwave systems. These circuits are often used as benchmarks to evaluate the speed of a digital technology[5, 6]. Up to now, the highest frequency divider is fabricated by Northrop Grumman Aerospace Systems[7] and UCSB[8]. The circuit's excellent performance is due to its perfect device process and the elaborate design of the interconnect.

In this paper, we report a 2 : 1 static frequency divider in our own InGaAs/InP heterojunction bipolar transistor process. The divider employs current-mode logic (CML) and its operation is fully static, operating from 500 MHz to 40 GHz while dissipating 650 mW of power in the circuit core from a –5 V supply.

2. Design and fabrication

The transistors in the circuit are formed from an MBE layer structure with a highly doped 65 nm InGaAs base and they are fabricated in a triple-mesa process with both active junctions defined by a chemistry selective wet etch. The layer structure is given in Fig. 1. The epitaxial layer design and radio frequency (RF) characteristics of the InGaAs/InP HBT used in CML circuits have been discussed in Refs.[9–12].

Benzocyclobutene (BCB) passivates devices and planarizes the wafer after device formation. The ensuing level of metal deposition is used for circuit interconnects and making electrical contacts to the transistors and resistors. Coplanar waveguide wiring is employed for its predictable characteristics, controlled impedance, and ability to maintain signal integrity at very high frequencies within dense mixed-signal ICs.

The HBT device model used in the circuit was established based on our InGaAs/InP DHBT process. The detail of the model is discussed in Refs. [13–15]. The divider architecture consists of several CML circuit stages which were highly optimized to obtain peak performance. The circuit stages shown in Fig. 2 consist of an input buffer, a frequency divider core, and an output buffer. The total power dissipation was 650 mW with the chip area of 1240 × 890 μm^2.

2.1. Input buffer

The input buffer of the divider is shown in Fig. 3. The input terminal is internally connected to ground via a 50 Ω resistor which results in a simple broadband 50 Ω-termination. We used a cascaded emitter followers as the input buffer be-

InGaAs:Si	200 nm	2×10^{19} cm^{-3}
InP:Si	130 nm	1.2×10^{19} cm^{-3}
InP:Si	40 nm	2×10^{17} cm^{-3}
InGaAs:C	65 nm	3×10^{19} cm^{-3}
InGaAs:Si	50 nm	1×10^{16} cm^{-3}
InGaAsP:Si (λ = 1.29 μm)	20 nm	1×10^{17} cm^{-3}
InGaAsP:Si (λ = 1.05 μm)	20 nm	1×10^{17} cm^{-3}
InP:Si	200 nm	1×10^{16} cm^{-3}
InP:Si	200 nm	1.2×10^{19} cm^{-3}
InGaAs:Si	50 nm	2×10^{19} cm^{-3}
InP:Si	400 nm	1.2×10^{19} cm^{-3}
InGaAs:UD	10 nm	
InP substrate		

Fig. 1. Device epitaxial layer structure.

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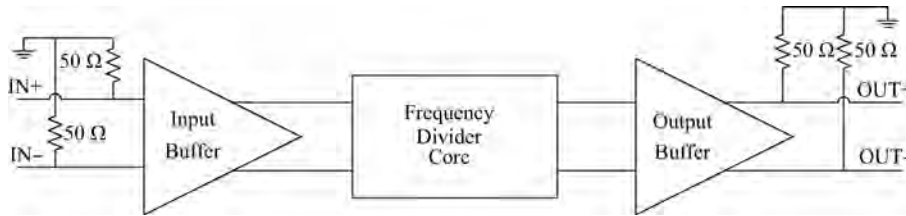

Fig. 2. Block diagram of the frequency divider circuit.

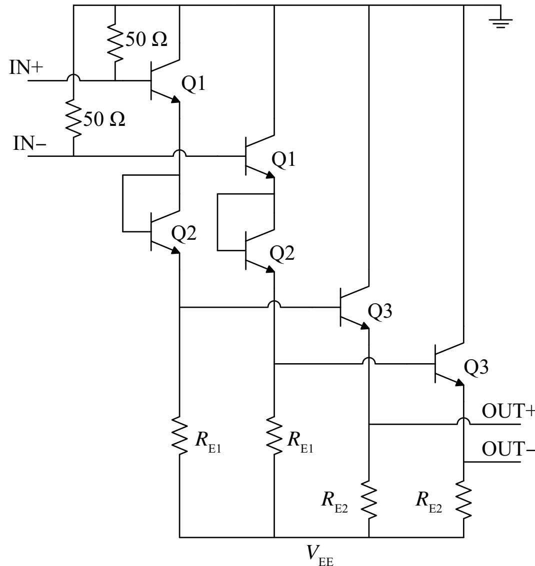

Fig. 3. Input buffer for the frequency divider circuits.

cause the capability of a single emitter follower to act as an impedance transformer degrades at high frequency. The level shifters were indispensable for the frequency divider circuit. They avoided saturation of the differential pairs by shifting the input signal level before connecting the signal to the input terminals of the clock pair. For the biasing of the level shifters, resistors were used instead of current mirrors. To bias each of the four emitter followers at a current of 10 mA, the values for the emitter resistors were set as follows: R_{E1} = 300 Ω, R_{E2} = 250 Ω.

2.2. Frequency divider core

Our frequency divider core was implemented using a master–slave (M–S) flip-flop consisting of two series connected latches that were clocked out of phase 180° (shown in Fig. 4). To generate the $f_{clock}/2$ frequency division, the differential output of the flip-flop was inverted and connected to the input such that the circuit changed state on the falling edge of the clock cycle. The M–S flip-flops were utilized as retiming elements for data synchronization. The circuit was fabricated with 1.4 × 15 μm^2 emitter HBT devices biased to ∼10 mA with a –5 V supply. We used a controlled current source for our frequency divider circuits because it was less sensitive to variations in power supply and temperature than a single resistor. Furthermore, the peak clock frequency of the static frequency divider was sensitive to the work current of the core. Considering the instability of our device process, we used the control voltage V_{c1} to adjust the work current of the core.

It was important to construct the divider layout compactly to reduce parasitic capacitance and inductance which ultimately slow down the divider. In order to minimize the difference in the signal propagation delays, both transmission lines had to have the same length. So the frequency divider core was symmetrically laid out and the transistors in the latches were oriented to minimize the critical feedback path of the M–S latches as well as other less critical signal paths.

2.3. Output buffer

A simple way of matching the circuit output to 50 Ω is the use of a differential pair with collector-load resistors of 50 Ω. This configuration was used in the output buffer shown in Fig. 4. Two pairs of transistors Q7 and Q8 served as level shifters for the subsequent differential pair. The voltage level of the input signal was shifted by $2V_{be,on}$ = 1.72 V. Simulations have shown that a cascade of two emitter followers tends to ring if its input lead lengths exceed approximately 200 μm. So we used single emitter followers for the output buffer. To bias the level shifters with a current of 10 mA, R_{E4} was set to 300 Ω. A second control voltage V_{c2} = –1 V was used to bias the differential pair in order to adjust the output swing independently of the internal logic swing of the frequency divider.

2.4. Layout

Figure 6 shows the static frequency divider layout and chip photograph. After the isolation of the device thin-film, TaN resistors were made by a sputtering process with a sheet resistance of ∼50 Ω/□. BCB was planarized using a dry etch to expose the electrical contacts to the three terminals of the transistor. And the BCB layer was used as the dielectric for the MIM capacitors. Many filtering capacitances and a large area ground reference was used to ensure the stability of the DC power supply.

3. Circuit measurements and results

Divide-by-2 circuit measurements for clock frequencies ranging from 0.5 to 40 GHz were performed at room temperature, 25 ℃. We used Agilent PNA E8363B to directly drive the clock input and Agilent E4440A spectrum analyzer to detect the output spectrum. The output signal spectra are shown in Fig. 7.

The input signal power in Figs. 7(a) and 7(b) is –5 dBm. The input signal power was 0 dBm when the input frequency was 40 GHz. The clock signal attenuation was more than 10 dB when the frequency was above 20 GHz. The main reasons for

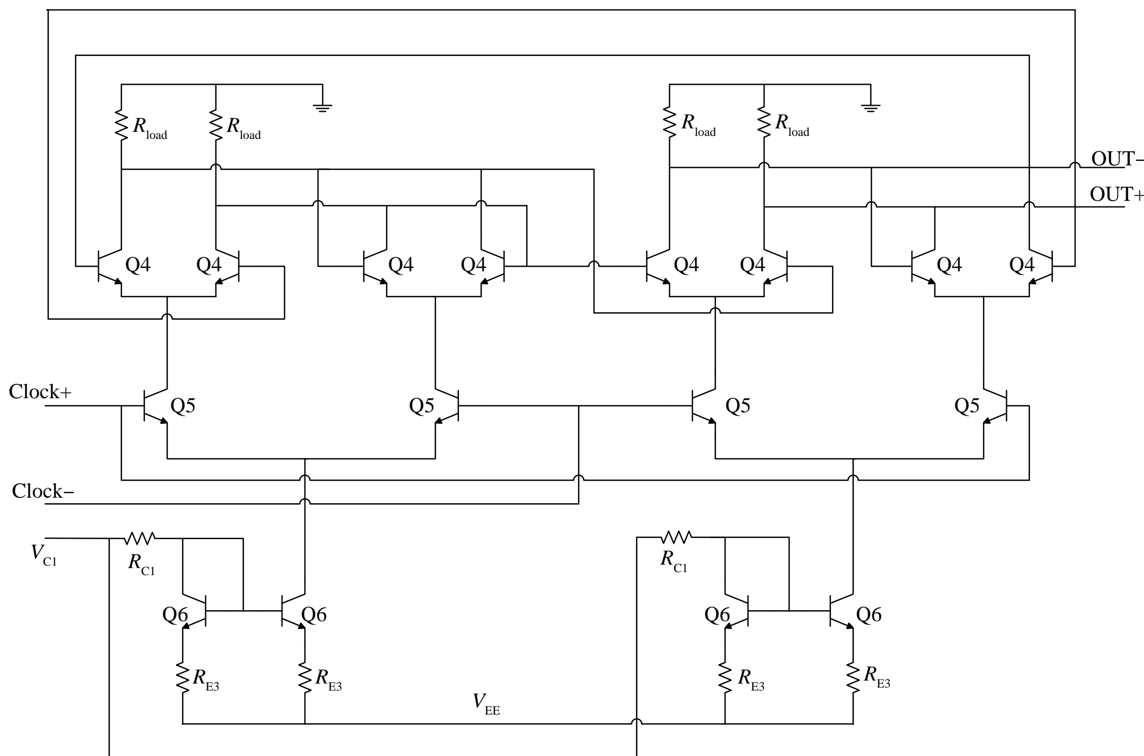

Fig. 4. Schematic of the frequency divider core.

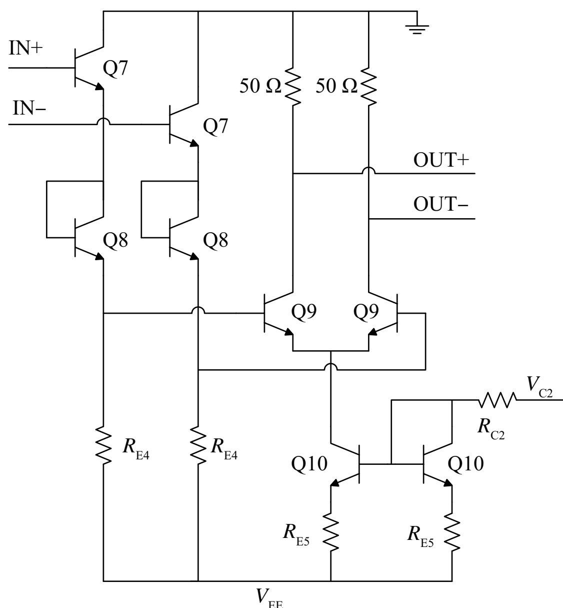

Fig. 5. Output buffer for the frequency divider circuits.

the loss are as follows. First, in our device process, we used a comparatively large scale device to ensure the high yield, and we had only two layers of gold interconnect. So the interconnect of the devices and the three stages of the divider was long. This caused a certain degree of losses. Second, in the process, we did not have a ground layer for the interconnect. There are more losses compared with the microstrip wiring. Finally, we paid less attention to the impedance matching between the input buffer and the core of the divider.

4. Conclusions

We have demonstrated a static frequency divider using InP/InGaAs DHBT technology in a standard three-mesa process. The divider was implemented in differential CML with 30 transistors using a self-aligned process and the BCB passivation and planarization process techniques. The circuit operated at a peak clock frequency of 40 GHz and dissipated 650 mW from a single –5 V supply. This divider was part of introductory research into the InP ultra-high frequency circuit based on our circuit process and device model. Although the performance of the circuit was limited by the interconnect, the process and our test equipment, the circuit represents the first exploration of InP ultra-high frequency circuits in China and it has provided valuable experience for our circuit design.

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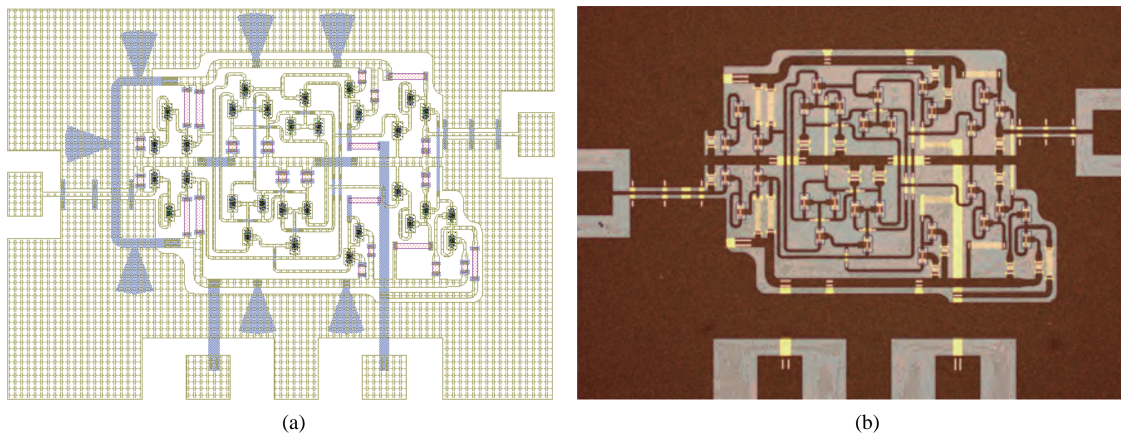
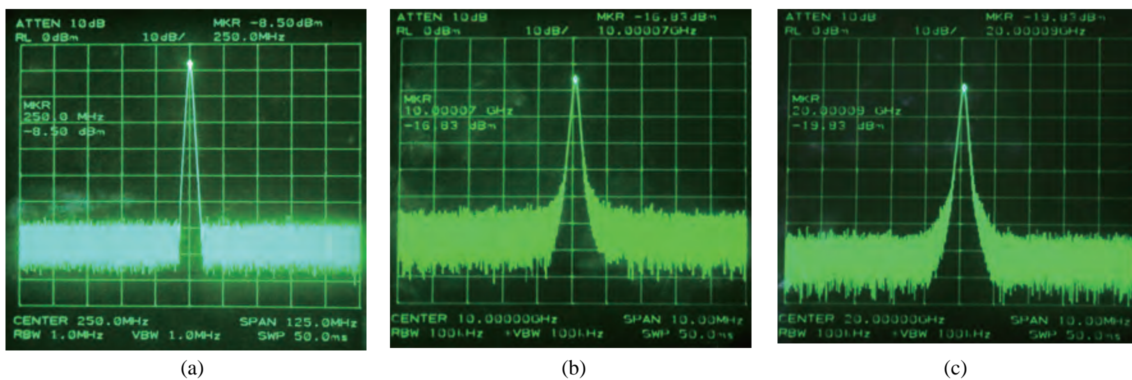


(a) (b)

Fig. 6. (a) Layout and (b) chip photo of the frequency divider circuit.



(a) (b) (c)

Fig. 7. Output signal spectrum of the divider. (a) $f_{\rm in}$ = 500 MHz, $f_{\rm out}$ = 250 MHz. (b) $f_{\rm in}$ = 20 GHz, $f_{\rm out}$ = 10 GHz. (c) $f_{\rm in}$ = 40 GHz, $f_{\rm out}$ = 20 GHz.

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