A low power 12-bit 30 MSPS CMOS pipeline ADC with on-chip voltage reference buffer*

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Abstract: A 12-bit 30 MSPS pipeline analog-to-digital converter (ADC) implemented in 0.13-μm 1P8M CMOS technology is presented. Low power design with the front-end sample-and-hold amplifier removed is proposed. Except for the first stage, two-stage cascode-compensated operational amplifiers with dual inputs are shared between successive stages to further reduce power consumption. The ADC presents 65.3 dB SNR, 75.8 dB SFDR and 64.6 dB SNDR at 5 MHz analog input with 30.7 MHz sampling rate. The chip dissipates 33.6 mW from 1.2 V power supply. FOM is 0.79 pJ/conv step.

Key words: analog-to-digital converter; pipeline; SHA removing; opamp; on-chip reference buffer
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1. Introduction

Analog-to-digital converter (ADC) is an important block in many applications such as video signal processing, medical imaging and wireless receivers. As in wireless receivers, 12-bit ADC with several tens of MHz sampling rate is enjoyed for the easy design of receivers systems[1]. On the other hand, the scaling down of CMOS technology reduces the supply voltage and the effective signal swing range, while noise keeps the same. This poses great challenges on the design of high accuracy ADC.

Power consumption is always one of the key issues for high performance ADCs, especially in portable applications. One effective way is to remove the front-end SHA[2, 3], but it is hard to match the sampling networks between the MDAC and subADC of the first stage in the level of circuit design while using low-offset auto-zeroed comparators in subADC. This work proposes a new kind of sampling network in the first stage for both sampling matching and comparator offset reducing. Another way is the opamp-sharing technique[4] with additional switches which may reduce the effective settling time of the operational amplifier (opamp) and introduce more distortion. A modified dual input opamp is adopted in this work as to cancel the additional switches. What's more, a low power on-chip voltage reference buffer is also integrated in the pipeline ADC without the need of external decoupling capacitors. Hence, the number of pads may be reduced, resulting in cost reduction.

A 12-bit 30 MSPS pipeline ADC is implemented in 1.2 V 0.13-μm 1P8M CMOS technology in this paper. Two-stage cascode-compensated opamps are adopted to enlarge the effective signal swing range. For power consumption reduction, the front-end sample-and-hold amplifier (SHA) is removed and opamps are shared in the backend stages.

2. Proposed ADC architecture

For medium or high resolution ADC and tens of MHz speed analog-to-digital conversion, the pipeline architecture is always the favorite for its good trade-off between speed, resolution, area and power consumption. By carefully choosing the stage resolution, pipeline ADC can achieve good power efficiency. For resolution less than 10-bit, 1.5 bit/stage is used for both low power and good tolerance on comparator offset[5]. However, as resolution goes to 12-bit or higher, multi-bit per stage will save more power and space[6]. In this paper, the pipeline ADC architecture with 2.5 bit/stage is adopted as shown in Fig. 1. The front-end SHA used in the conventional pipeline ADC is removed since it not only consumes a lot of power but also introduces extra distortion and noise. Every pipeline stage consists of an MDAC block and a subADC block, and all of them work at two phases. In the sampling phase, the analog input of pipeline stage is sampled into the sampling capacitors of MDAC, while it is also quantified by the subADC. Then in the holding phase, the MDAC outputs and holds the residue voltage according to the sampled analog input and quantification results. Note that the two successive stages do not work at the same phase simultaneously. When one of them works at the sampling phase, the other works at the holding phase. It is known that the opamp only works at the holding phase, so it can be shared between the two successive stages as to reduce power consumption. This is the so-called opamp-sharing technique, which can reduce power consumption effectively. There are only 3 opamps used since every two successive stages in the backend share one opamp.

Except for the five 2.5-bit stages and a final 3-bit flash, it also includes a clock generator, a voltage reference buffer and a serial control interface (SCI) block as shown in Fig. 1. Non-overlapping clocks are generated by the clock generator as to control the operation of pipeline ADC, and the clock wave-

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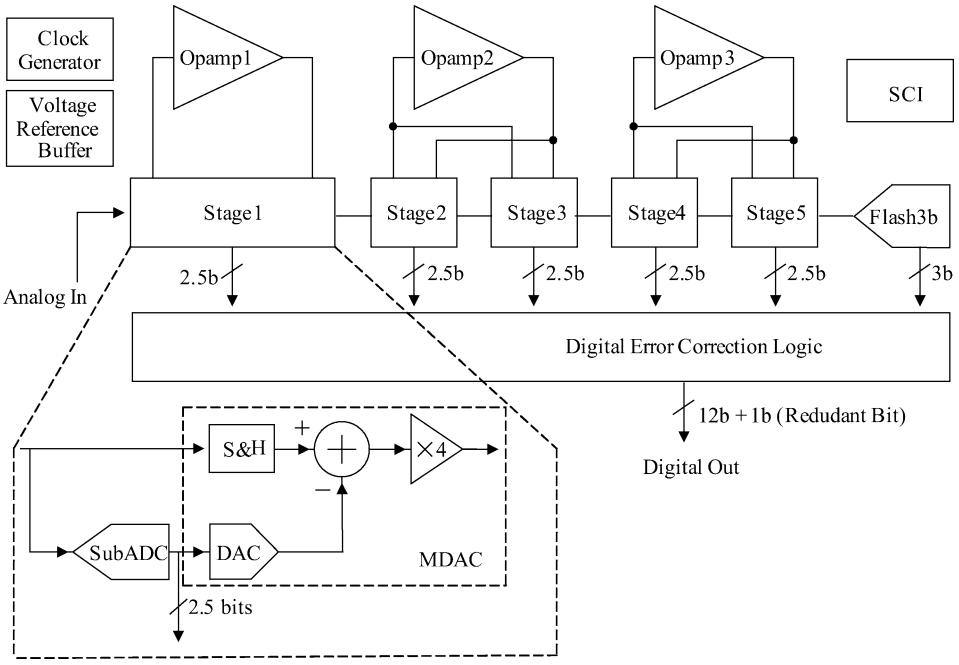

Fig. 1. Block diagram of the proposed pipeline ADC.

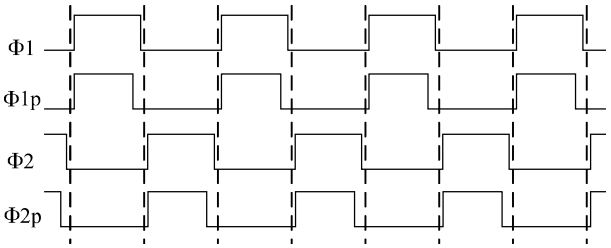

Fig. 2. Clock waveforms for the pipeline operation.

forms are shown in Fig. 2. For the odd numbered stages, $\Phi 1$ is the sampling phase and $\Phi 2$ is the holding phase. However, for the even numbered stages, $\Phi 1$ is the holding phase and $\Phi 2$ is the sampling phase. $\Phi 1$p and $\Phi 2$p have the same rising edges as those of $\Phi 1$ and $\Phi 2$, but their falling edges are in front of those of $\Phi 1$ and $\Phi 2$ respectively. They are used to turn off the sampling switches before the end of the sampling phase. Otherwise charge injection effect of switches will degrade the accuracy of samples badly. Except for the clock generator, an on-chip voltage reference buffer is also integrated in the pipeline ADC. It drives capacitor loads during residue amplification of MDACs without the need of external decoupling capacitors. Controlled through SCI, all bias-currents and most reference voltages are made programmable to accommodate unexpected parameter skews.

3. Circuit design

3.1. Proposed front-end SHA removing technique

An effective solution to realize low power pipeline ADC is to remove the front-end SHA[2]. However, sampling matching between the MDAC and subADC of the first stage is critical. In the conventional SHA-less pipeline ADC[2], as sampling network shown in Fig. 3(a), the sampling switches and capacitors should be carefully designed and adjusted according to post-layout simulation results, which makes circuit design more complex. Another way is to drop the auto-zeroed method in comparator[3] and just keep the sizes of sampling switches and capacitors between the MDAC and subADC in ratio, as shown in Fig. 3(b). However, the offset of comparator without auto-zero will also limit the accuracy of the whole pipeline ADC, especially for multi-bit/stage architecture.

To overcome both sampling mismatch and comparator offset, a new sampling network in the first stage is proposed here, as shown in Fig. 3(c). Unlike the conventional auto-zeroed comparator as shown in Fig. 3(a), another capacitor $C_{\mathrm{S,offset}}$ is between the input of preamplifier and the bottom plate of sampling capacitor $C_{\mathrm{S,signal}}$. So the bottom plate of $C_{\mathrm{S,signal}}$ can be pulled down to V_{cmi} during the sampling phase, like that in Fig. 3(b). Meanwhile, the offset of preamplifier is also sampled into $C_{\mathrm{S,offset}}$, and then subtracted from the input signal during the comparing phase so that the offset of preamplifier will be counteracted. Since the preamplifier has some gain, the equivalent input offset of comparator is very small. This is the so-called auto-zeroed method. And the proposed sampling network in Fig. 3(c) makes it possible while keeping sampling matching between the MDAC path and subADC path in the first stage. Moreover, sampling switches in the MDAC and subADC of the first stage are both bootstrap switches which have small resistance and good linearity.

3.2. Dual input opamp for opamp-sharing

Opamp-sharing technique is also an effective way to improve the power efficiency of pipeline ADCs. Figure 4 shows the conventional opamp-sharing technique for 2.5-bit stages, in which C_{SA1}–C_{SA4} and C_{SB1}–C_{SB4} are the sampling capacitors for the two successive stages respectively. As the clock waveforms shown in Fig. 2, in Φ_1, C_{SA1}–C_{SA4} sample the ana-

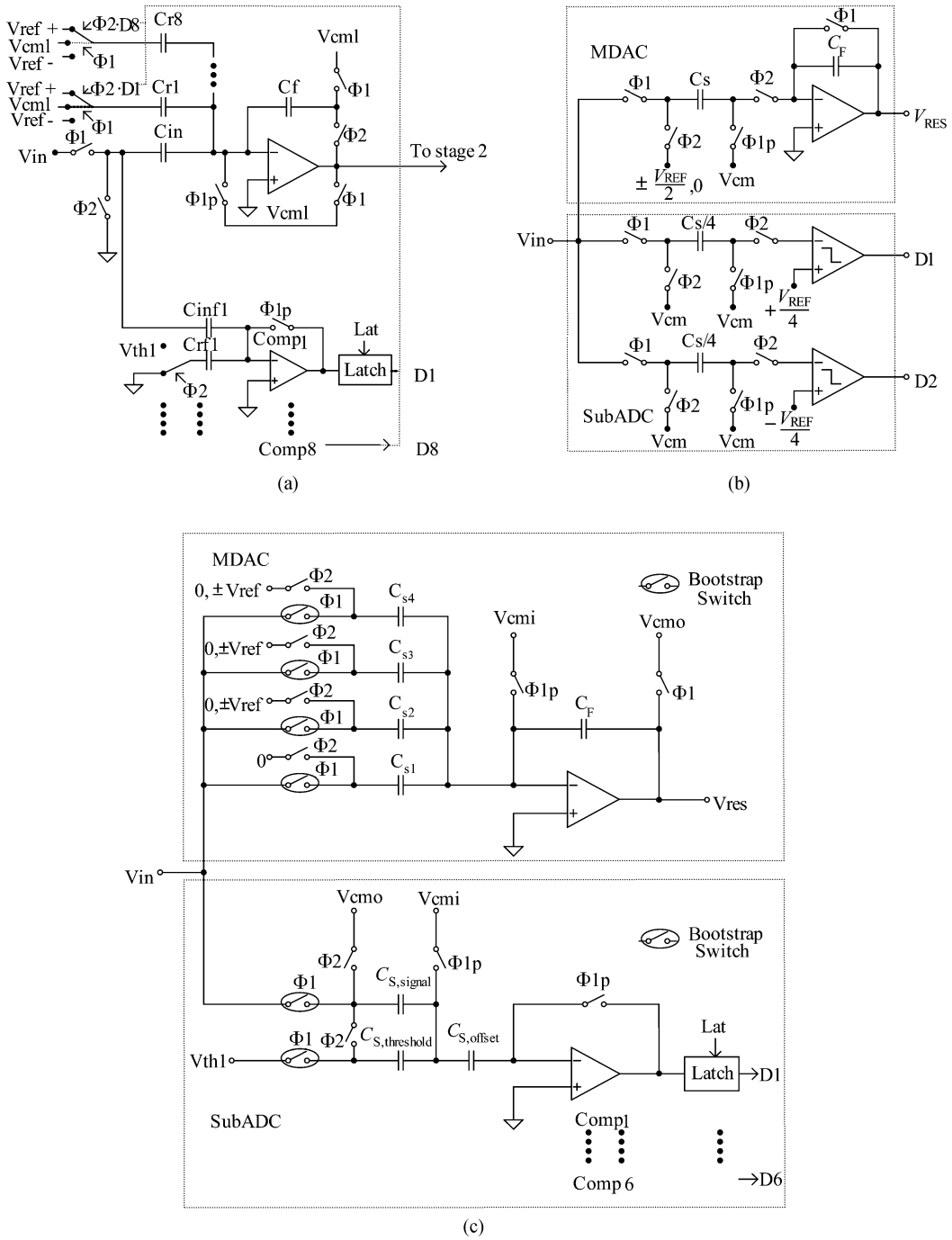

Fig. 3. (a) Sampling matching network I[2]. (b) Sampling matching network II[3]. (c) Proposed sampling matching network.

log input, while the opamp amplifies the residue voltage on C_{SB1}–C_{SB4}; in $\Phi 2$, the opamp amplifies the residue voltage on C_{SA1}–C_{SA4}, which is also sampled into C_{SB1}–C_{SB4}. The opamp works continuously without reset, so its power efficiency is improved greatly. The switches SW1–SW4 are added to isolate the switch-capacitor (SC) networks of the two successive stages. However, due to the on-resistance of switches and charge injection effect, these additional switches not only reduce the effective settling time of the opamp but also introduce nonlinearity[4]. Comparatively, the opamp with dual inputs as shown in Fig. 5 is a better choice to avoid the additional switches SW1–SW4[7]. The two successive stages are isolated by the two input pairs instead, which would not introduce other error sources and degrade the ADC's performance.

The schematic of the modified dual input opamp used in the proposed pipeline ADC is shown in Fig. 6. It uses two stages including a class-A output stage to enlarge the output voltage swing. Two compensated capacitors connected from the sources of the cascode NMOS and PMOS transistors to the output nodes make the settling speed of this opamp faster than that of the miller-compensated one. Though it consumes a little more power consumption without turning off one of the two folded-cascode input pairs[7], there is no turn-on delay when switching the input pairs. Moreover, it's more stable since there is no great change on the current flowing through either of the two input pairs. The modified opamp is shared between the two

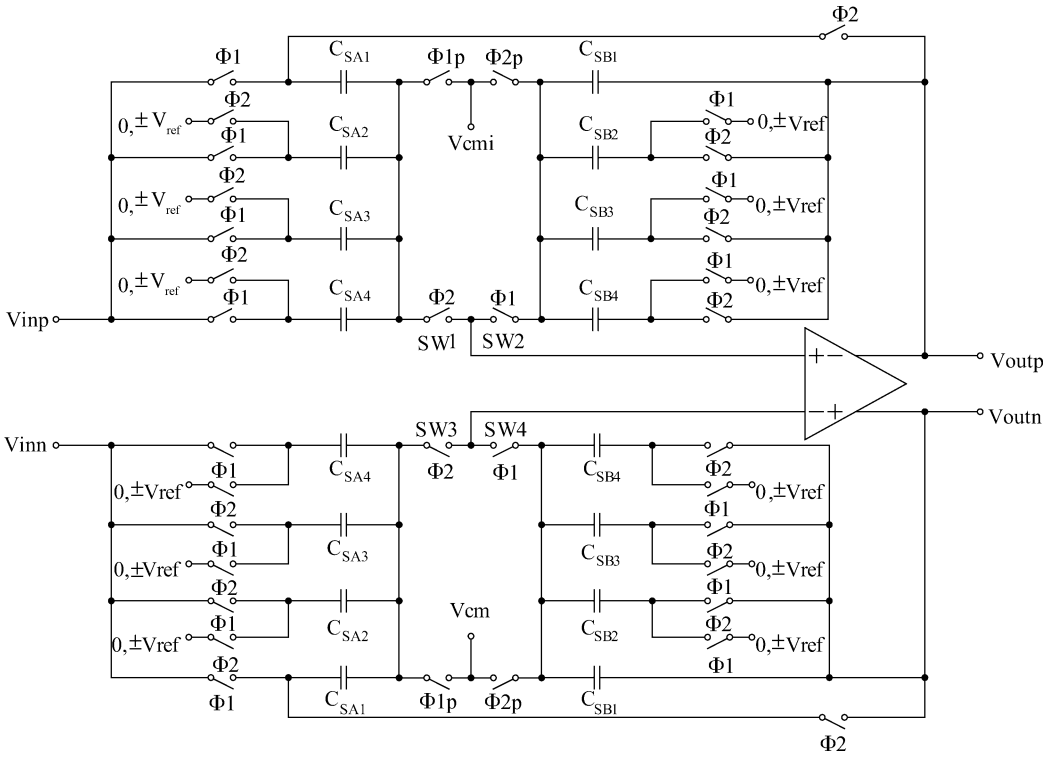

Fig. 4. Conventional opamp-sharing technique using additional switches.

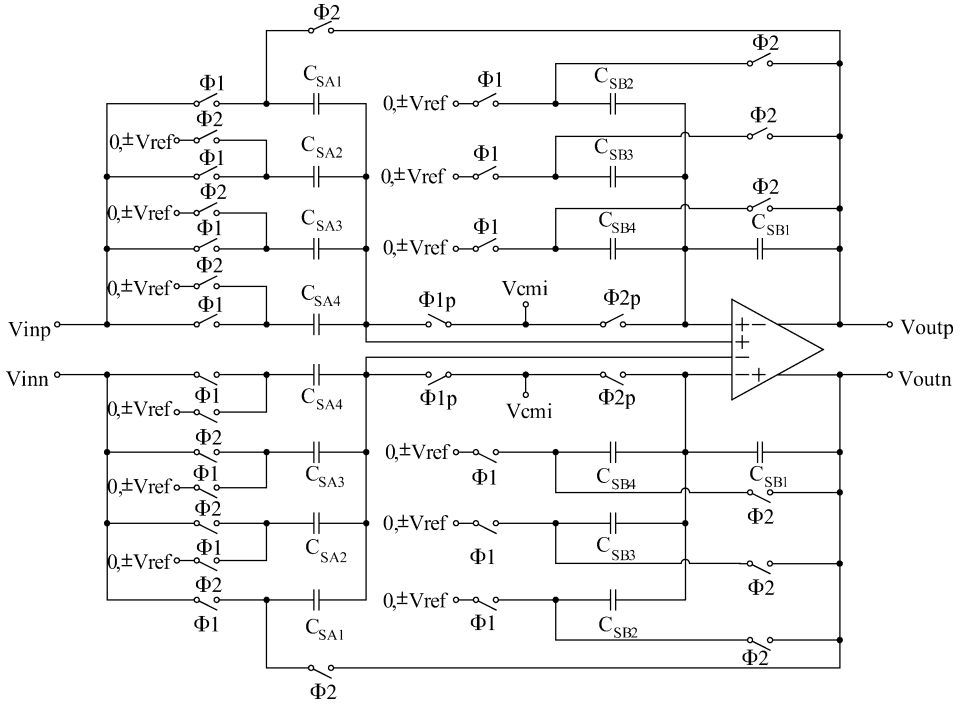

Fig. 5. Opamp-sharing technique using dual input opamp.

successive 2.5-bit stages in the proposed pipeline ADC, so the two input pairs have the same sizes. It can also be shared between stages with different stage resolutions since their sizes can be different.

The common mode feedback circuit (CMFB) consists of an SC network and a voltage-to-current converter composed by Mfb1 and Mfb2. The change of output common mode voltage will be feedback into the input through Mfb1, which is fast and stable at the cost of some extra power consumption. One of the two input pairs will receive the feedback current when it's connected to input common mode voltage at its idle phase. Without the dual input pairs, the CMFB has the risk that the feedback loop may be cut off from the input, since one input pair may firstly work at the cut-off region.

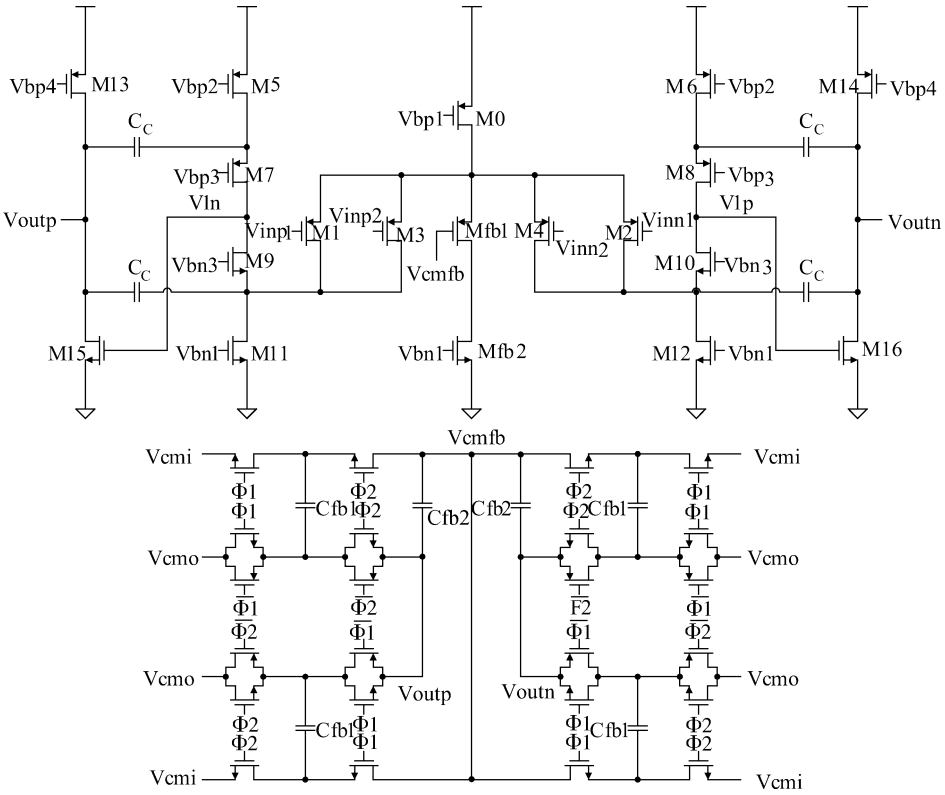

Fig. 6. Two-stage cascode-compensated opamp.

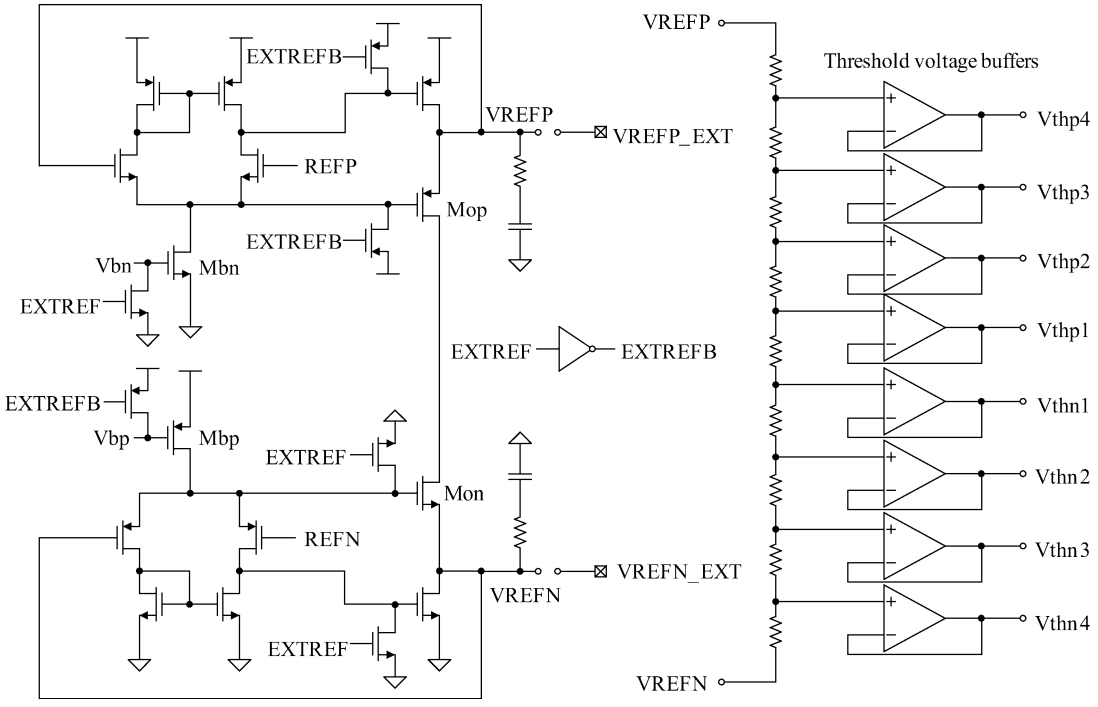

Fig. 7. On-chip voltage reference buffer.

3.3. On-chip voltage reference buffer

In the SC pipeline ADC, voltage reference buffer is needed though it consumes power. There are two purposes for its application in the pipeline ADC. First, sampling capacitors should be charged or discharged to reference levels during the residue amplification of MDACs. Second, it also provides threshold voltages for comparators in SubADCs. To satisfy the settling requirement for large capacitive load, the bandwidth of the buffer should be large, which can be only achieved by sacrificing a large amount of power. It's estimated that the power of the voltage reference buffer takes about 20%–30% of the overall power consumption of the pipeline ADC[8]. For this reason, external reference with decoupling capacitors is preferred in

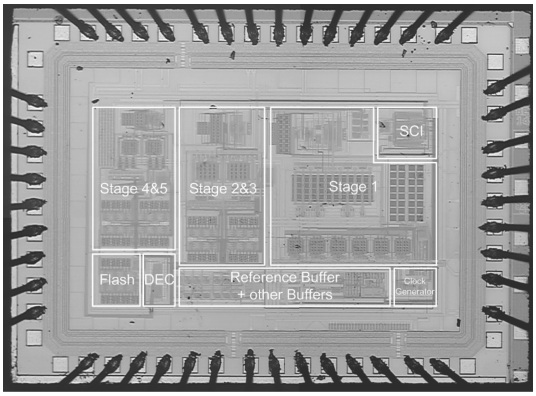

Fig. 8. Die photograph of the prototype ADC.

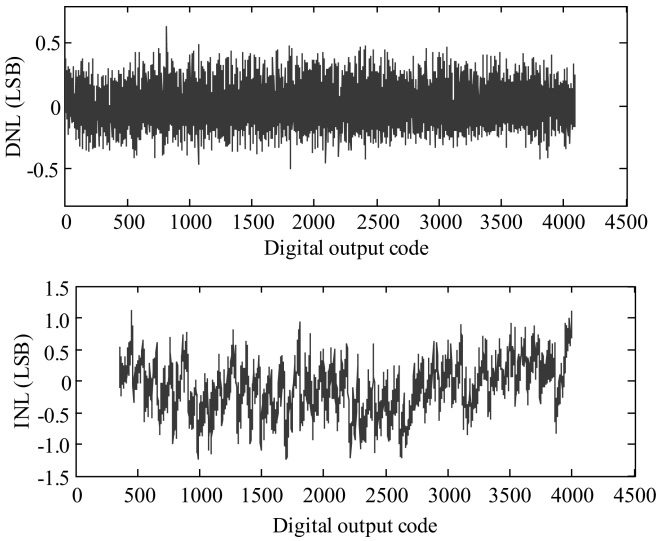

Fig. 9. Measured DNL and INL @ f_{in} = 5 MHz, f_S = 30.7 MHz.

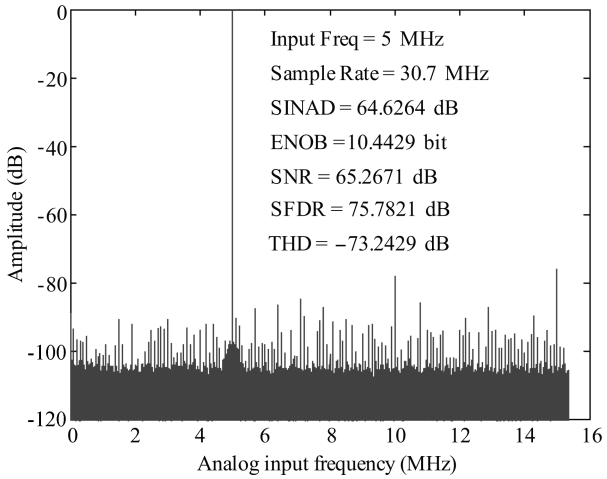

Fig. 10. Measured FFT spectrum @ f_{in} = 5 MHz, f_S = 30.7 MHz.

Table 1. Summary of ADC performance @ f_{in}= 5 MHz.

Parameter	Value
Technology	0.13-μm 1P8M CMOS technology
Power supply	1.2 V
Resolution	12-bit
Conversion rate	30.7 MHz
Input signal range	1.2 Vpp
DNL	–0.51 LSB to +0.64 LSB
INL	–1.18 LSB to +0.98 LSB
SNR	65.3 dB
SFDR	75.8 dB
SNDR/ENOB	64.6 dB/10.44 bit
Area	2.7 mm^2
Power consumption	33.6 mW 30 mW (Excluding on-chip reference buffer)
FOM [Power/($f_S \times 2^{ENOB}$)]	0.79 pJ/conv step 0.70 pJ/conv step (Excluding on-chip reference buffer)

the conventional design, but it increases the pads of the chip, the count of external components and the overall system cost. So an on-chip voltage reference buffer is integrated in the proposed pipeline ADC.

In Fig. 7, the two-stage opamp is used as buffer, and the output stages of the positive and negative reference buffers are combined together to save power consumption. Moreover, the two cascode transistors Mop and Mon in the output stage are biased by the drain voltages of the tail transistors of two input stages without the need of some extra bias circuits. The dominant pole is seen at the output stage which has a large driving ability, so the miller capacitor is removed here.

Some switches are added to power off the voltage reference buffer when EXTREF is high, and it provides two external reference levels instead. So the performance of the proposed pipeline ADC with on-chip reference buffer can be compared with that using external reference buffer. A simple on-chip low pass capacitor-resistor filter which is added at the output reference node will further improve the settling speed of the reference buffer.

4. Experimental results

The prototype ADC has been fabricated in 0.13-μm 1P8M CMOS technology with MIM capacitors. Figure 8 shows the die photograph and it occupies an area of 1.40 × 1.92 mm^2. The DNL and INL are measured at 30.7 MHz sampling rate with 5 MHz analog input. As shown in Fig. 9, the measured DNL is −0.51/0.64 LSB and INL is −1.18/0.98 LSB. Figure 10 indicates the measured FFT spectrum of the pipeline ADC with on-chip voltage reference buffer. It shows that the measured SNR, SFDR and SNDR are 65.3 dB, 75.8 dB and 64.6 dB, respectively. With power consumption of 33.6 mW, the figure of merit (FOM) of this work is about 0.79 pJ/conv step. Table 1 summarizes the whole performance of this ADC. Table 2 compares this work with some similar ADCs and it shows that the FOM of this work is comparable with these outstanding ADCs.

5. Conclusion

This paper presents a 1.2 V 0.13-μm 12-bit 30 MSPS pipeline ADC. Power consumption is reduced by removing the

Table 2. Performance comparison with similar ADCs.

Reference	Bit	MSPS	Technology	With on-chip reference buffer	Input (MHz)	SNDR (dB)	Power (mW)	FOM (pJ/conv step)
JSSC07[9]	13	40	0.18-μm	No	1	67	268	3.7
CICC08[10]	12	30	65-nm	No	4.7	65.1	18	0.41
AD9629[11]	12	20	—	Yes	9.7	71.4	45	0.74
This work	12	30	0.13-μm	Yes	5	65.6	33.6	0.79

front-end SHA and sharing opamps between successive stages in the backend. It also integrates a low power on-chip voltage reference buffer without the need of external decoupling capacitors. The measured SNDR is 64.6 dB at the analog input of 5 MHz with 30.7 MHz sampling rate. The chip occupies an area of 2.7 mm^2 and consumes 33.6 mW from 1.2 V power supply. FOM is 0.79 pJ/conv step. This ADC will be integrated in an SDR system.

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