A 2.5-V 56-mW baseband chain in a multistandard TV tuner for mobile and multimedia applications*

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Abstract: This paper presents post-layout simulated results of an analog baseband chain for mobile and multimedia applications in a 0.13-μm SiGe BiCMOS process. A programmable 7th-order Chebyshev low pass filter with a calibration circuit is used in the analog baseband chain, and the programmable bandwidth is 1.8/2.5/3/3.5/4 MHz with an attenuation of 26/62 dB at offsets of 1.25/4 MHz. The baseband programmable gain amplifier can achieve a linear 40-dB gain range with 0.5-dB steps. Design trade-offs are carefully considered in designing the baseband circuit, and an automatic calibration circuit is used to achieve the bandwidth accuracy of 2%. A DC offset cancellation loop is also introduced to remove the offset from the layout and self-mixing, and the remaining offset voltage is only 1.87 mV. Implemented in a 0.13-μm SiGe technology with a 0.6-mm^2 die size, this baseband achieves IIP3 of 23.16 dBm and dissipates 22.4 mA under a 2.5-V supply.

Key words: multimedia; baseband; low pass filter; leapfrog; programmable gain amplifier; frequency calibration; DC negative feedback loop

DOI: 10.1088/1674-4926/32/3/035003 **EEACC:** 1270E; 2570F; 6420D

1. Introduction

As a variety of digital mobile TV standards are being deployed and applied in more and more countries, the concept of multi-functional mobile entertainment platforms is gradually increasing. Using multimedia-rich handheld devices to watch satellite TV has become the latest trend, and mobile TV reception systems are in great demand. In order to increase user flexibility and create considerable economic benefits for multimedia terminal equipment manufacturers, the research and development of multi-standard receivers, supporting both mobile and broadcast digital TV, will be the next hot spot. The main mobile TV standards expected to co-exist are DVB-H in Europe, T-DMB in South Korea, S-DMB in Japan and South Korea, Qualcomm's MediaFLO, and the CMMB standard with independent intellectual property rights in China. In addition to multi-standard operation, low-cost, low-power and small physical size required by cellular phones and other mobile terminals necessitate moving into smaller geometries and integrating more functionality into a single piece of silicon. The structure of a direct-conversion tuner has successfully resolved these problems. But the direct-conversion architecture has many unavoidable weaknesses, such as DC offset, I/Q mismatch and even-distortion, which bring many challenges to the analog baseband design.

First, the analog baseband chain in the direct-conversion tuner must meet many stringent specifications, such as precise cut-off frequency, sharp transition zone, sufficiently large stopband attenuation, and a high linearity and dynamic range. Therefore, a 7th-order Chebyshev LPF is selected to meet the frequency response specification. The filter's programmable cutoff frequency is set to 1.8/2.5/3/3.5/4 MHz. In order to compensate for the device's constant drift caused by process variation, an on-chip frequency automatic calibration system is using to make the cutoff frequency to maintain the desired frequency point.

Second, a direct-conversion tuner may result in a large DC offset component in the down-conversion process, so the DC offset may saturate the baseband output and degrade the dynamic range. A multi-level DC negative feedback circuit can effectively reduce DC offset component.

2. Analog baseband design

In this section, the active low-pass filter, programmable gain amplifier, DC offset cancellation and automatic frequency calibration circuit will be discussed in detail.

The baseband consists of a filter, a programmable gain amplifier (PGA), a buffer and a DC offset cancellation (DCOC)

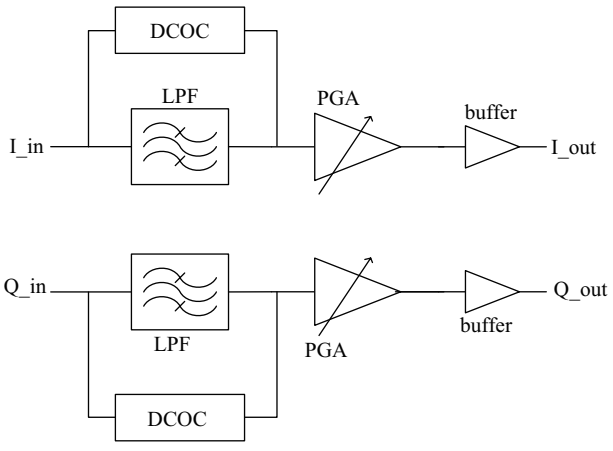

Fig. 1. Block diagram of baseband chain.

* Project supported by the Provincial and Ministerial Industry-Academia Cooperation Project of China (No. 2009A090100019).

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Received 13 July 2010, revised manuscript received 5 October 2010

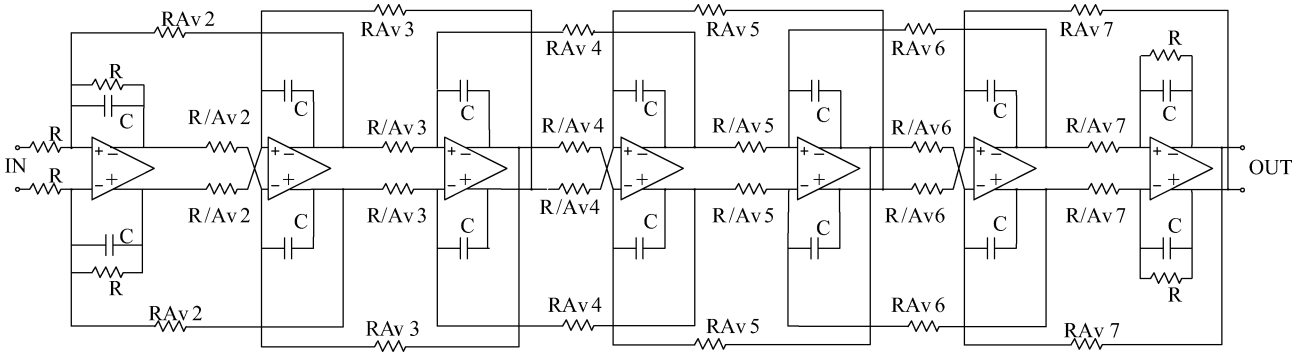

Fig. 2. Schematic diagram of the 7th-order Chebyshev filter. The variable gain of the filter is obtained by switched resistor matrices, and the Av2 to Av7 are the resistor scaling factors.

loop, as shown in Fig. 1. The baseband PGA is designed to provide a gain range of 40 dB with 0.5-dB steps. The 7th-order Chebyshev LPF filter with an on-chip frequency automatic calibration is accomplished using a capacitor switching technique over all temperatures, and process variation. The multi-level DC negative feedback circuit is used to remove DC offsets introduced from the mixer and layout.

In order to meet the high linearity requirement and suppress common mode noise, the analog baseband is designed to a fully differential structure.

2.1. Variable gain channel filter

There are two major issues when we design a baseband LPF. One is the selection of the filter LCR prototype, that is, Butterworth or Chebyshev. The other is the selection between G_m–C and active-RC[1].

The filter rejection response is the main concern for the selection of the LCR prototype. Regarding the stringent adjacent-channel rejection specifications of digital mobile TV standards, Chebyshev filters are more suitable and require fewer orders than Butterworth filters do.

For the selection between G_m–C and active-RC, G_m–C filters are generally used for applications of this kind since G_m amplifiers have a high bandwidth. So G_m–C filters are more suitable for the applications of transmitters, because of their better high frequency performance. On the other hand, the op-amp of active-RC filters is used to working in the closed-loop state, so active-RC filters have a higher linearity and wider dynamic range than G_m–C filters.

As a consequence, a Chebyshev active-RC structure is chosen for this baseband filter. In addition, compared with a cascade of biquard to constitute a high order filter, the leapfrog structure has lower sensitivity against the component variations, in order to decrease the passband sensitivity that results from components, the leapfrog technique is chosen to synthesize the filter, the resistance and capacitance value of filter obtained from the RLC ladder prototype.

The structure of the baseband filter is shown in Fig. 2. Switching resistor and capacitance arrays controlled by digital means are used to achieve a programmable cut-off frequency and a 40-dB filter gain.

The design of the op-amp is critical to active-RC filters. Here, we'll analyze the Q increase problem which depends on

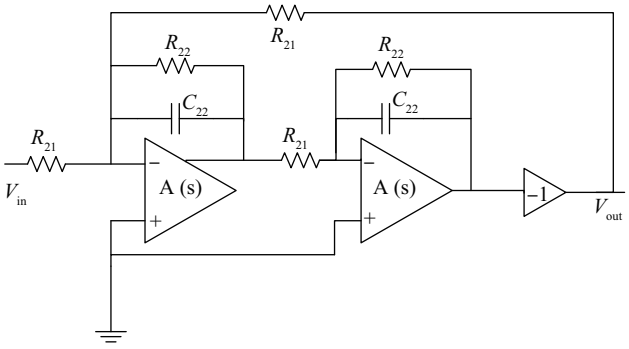

Fig. 3. Block diagram of 2nd-order filter.

the bandwidth of filter. There are two reasons why the Q of an active-RC filter is different from that of an LCR prototype. One reason is that a nonideal amplifier may introduce poles which lead to a change in the frequency characteristics of the filter. The second reason is that different LCR prototypes require different powers, for example, Chebyshev filters need more power than Butterworth filters, so as the GBW decreases, the Q of the Chebyshev filters increases more abruptly from that of the LCR prototype than Butterworth filters. In order to analytically solve the Q increase dependence on the bandwidth and the Q of an LCR prototype, a second-order filter is analyzed here, as shown in Fig. 3.

The transfer function of a nonideal amplifier is expressed as

$$A(s) = \frac{A_{\text{amp}}\omega_{\text{amp}}}{s + \omega_{\text{amp}}}, \tag{1}$$

where A_{amp} and ω_{amp} are DC gain and the dominant pole frequency of the amplifier, respectively. We can suppose that this nonideal amplifier is used in a lossy integrator, as shown in Fig. 3, then its transfer function is derived as

$$H_{\text{lossy}}(s) \approx \frac{1/R_{21}}{\left(\dfrac{1}{R_{22}} - \dfrac{\omega^2 C_{22}}{A_{\text{amp}}\omega_{\text{amp}}}\right) + sC_{22}}. \tag{2}$$

Now that the denominator is a first-order polynomial in terms of s, the Q of the filter is expressed as

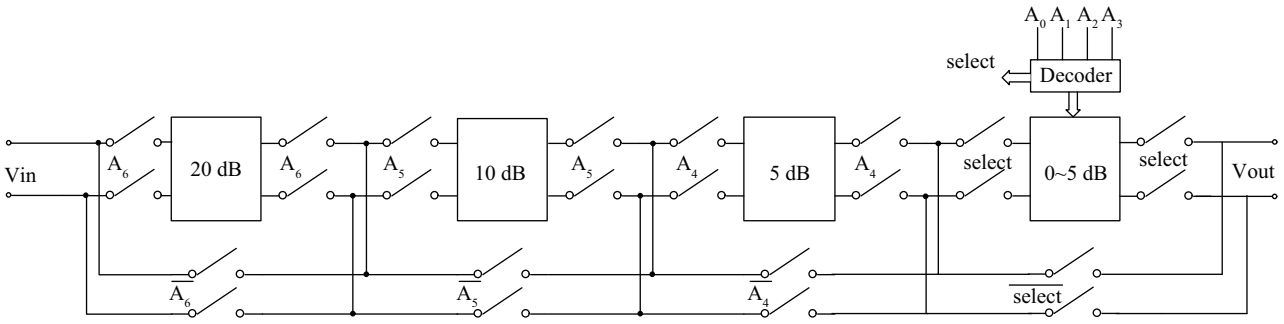

Fig. 4. Basic block diagram of the PGA.

$$Q_{\text{lossy}} \approx \frac{1}{2R_{21}} \frac{1}{\left(\dfrac{1}{R_{22}} - \dfrac{\omega^2 C_{22}}{A_{\text{amp}}\omega_{\text{amp}}}\right)}. \tag{3}$$

We can derive the Q increase in the filter due to its amplifier's nonideality. We define ΔQ as

$$\Delta Q = \frac{Q_{\text{lossy}} - Q_{\text{I}}}{Q_{\text{I}}} \approx \frac{2\omega_{\text{I}} Q_{\text{I}}}{A_{\text{amp}}\omega_{\text{amp}}}, \tag{4}$$

Q_{lossy} is the Q factor of the lossy integrator, which has a nonideal amplifier; Q_{I} is the Q factor of integrator with an ideal amplifier; ω_{I} is the bandwidth of the filter.

According to Eq. (4), the required GBW for the Chebyshev filter is twice as high as the GBW for the Butterworth filter. As for the 7th-order Chebyshev, which can be divided into 3 second- and a first-order filter, to keep the increase in the Q smaller than 2%, the GBW of 3 second-order filters must be 249, 72.2 and 33.9 ($Q_{3,2,1} = 6.2$, 1.81 and 0.85) times as large as the cutoff frequency of 4 MHz, respectively. So the GBW of the amplifiers are 6.26, 1.81 and 0.85 Grad/s, respectively. Then, we design different amplifiers to satisfy the above requirement of the GBW, and it benefits from reducing the baseband power consumption.

The implementation of the op-amp is a typical two-stage miller-compensation op-amp with a common feedback circuit. The simulation shows that the op-amps can achieve a GBW of 6.26, 1.81 and 0.85 Grad/s, phase margins of more than 60°, DC gains of 65, 70 and 71 dB, and power consumption are 5.7, 3.7 and 2.5 mW with the load capacitor of 0.5 pF and the load resistor of 10 kΩ, respectively.

2.2. Programmable gain amplifier

The form of the PGA's gain control can be divided into two categories. One is to change the parameters of the open-loop amplifier, and the other one is to change the closed-loop amplifier's feedback factor. The former usually has relatively poor linearity that can't meet the strict linearity requirements of mobile digital TV standards. The latter adjusts gain by changing the feedback resistor, so it has very good linearity and relatively simple implementation, but its disadvantage is that it consumes more power and needs a higher load capacity of the op-amp. As the analog baseband circuit is divided into several cascade sub-modules, the selection of a common-mode voltage level is also important to the PGA's design.

In order to match the PGA's common-mode voltage level with the filter and meet the high linearity requirement, we choose the latter one to achieve the precision gain control. The above disadvantages can be overcome by an appropriate design.

Figure 4 shows the PGA block diagram. This consists of 4 stages, and their gains are set to 20 dB, 10 dB, 5 dB and 0–5dB, respectively, where the former three are fixed gain stages and the last one is the variable gain stage with a 0.5-dB gain step. There's a digital signal in each stage to access or bypass the baseband chain, and accordingly the gain of each stage is selected to its rating or 0 dB. By different combinations of the 4 stages, it can achieve a linear 40-dB gain range with a 0.4-dB resolution.

The above structure has the advantage that when a certain stage's gain is 0 dB, the input signal is added directly to the input of the next stage, which avoids the introduction of that stage's gain error.

2.3. DC offset cancellation

DC-offset cancellation is indispensable in a direct conversion receiver because DC offset may saturate the baseband output and degrade the dynamic range. Currently, the main methods of elimination of DC offset are a DC negative feedback loop, AC-coupled, digital elimination and feedforward elimination, etc. AC coupled will use a large capacitor that occupies a large chip area, digital elimination is very complex, and feedforward elimination has very strict requirements of the circuit's matching. Therefore, a DC negative feedback loop is used to eliminate the DC offset. The basic concept of a DC negative feedback loop is to detect the DC offset component of the output, then convert it into a voltage or current signal to be subtracted from the input and adjust the final output.

Featuring a high-pass response in the signal chain, the DCOC has a cutoff frequency of less than 1 kHz to ensure that sub-carriers around DC are not affected too much. However, such a low cutoff frequency will demand large loop capacitors if a single feedback loop cancellation is utilized in the baseband signal path, inevitably implemented in off-chip components at the expense of extra package pins. Since the high-pass corner frequency is proportional to the signal processing gain, but inverse to the loop capacitance, multi-loop cancellation can effectively reduce the required loop capacitances. As the signal chain is uniformly divided into M segments in cascade, the ratio of the total required loop capacitance in single-loop calibra-

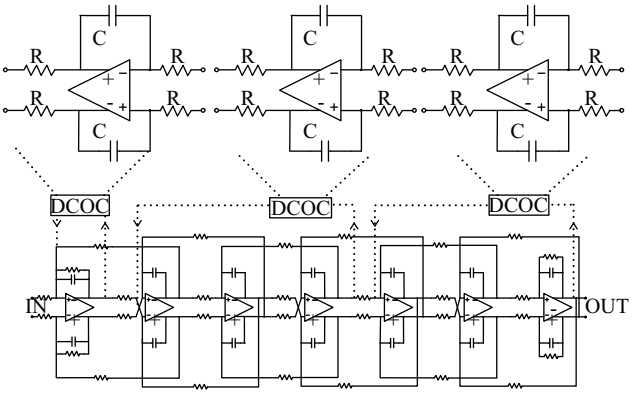

Fig. 5. DCOC schematic diagram.

tion to that in multi-loop can be approximated can be induced as

$$\frac{C_{\mathrm{sl}}}{C_{\mathrm{ml}}} = \frac{A^{1-1/M}}{M}, \tag{5}$$

where A is the DC gain of amplifier, C_{sl} and C_{ml} are the total capacitance required in single-loop and multi-loop cancellation, respectively[2]. In addition, the loop feedback resistors can be instead for PMOS active resistance. The width to length ratio of PMOS is set to as small as possible. The equivalent resistances are about 4 MΩ.

As is shown in Fig. 5, three independent servo-loops are utilized to reject DC offset in this design, in total using 12 pF capacitance, which is much easier to integrate on chip since 83 times less total capacitance is required compared with a single loop implementation.

2.4. Automatic frequency calibration circuit

On-chip automatic frequency calibration circuit activated at power-up accurately sets the channel bandwidth from 1.8 to 4 MHz against PVT variations. The architecture and the timing diagram are depicted in Fig. 6[2]. An RC integrator compares the RC time constant with a reference clock. The detailed calibration procedure is described as follows.

Firstly, the $\mathrm{CLK_B}$ is set to high. The integrator is configured as a resistive feedback amplifier with gain attenuation. As a result, both integrator outputs, V_{op} and V_{on}, are reset to the op-amp's common-mode voltage. Secondly, the $\mathrm{CLK_B}$ is low.

The integrator is configured as a lossless integrator, which forces its positive output V_{op} to charge toward VDD and its negative output V_{on} to discharge to ground. Once V_{on} becomes smaller than the reference voltage, the digital comparator will generate a STOP signal to interrupt the counter. Then the counter's present code is subtracted from the bandwidth code. If the residue is zero, it means that the present value of the RC time constant is equal to the default value, the channel bandwidth is correct and the calibration system is power off. If the residue is not zero, the subtracted output code is sent to update the capacitor-code used to control the capacitor banks. The calibration will continue until the capacitor code remains constant for several consecutive iterations. Finally, a 5-bit control word is provided to adjust the capacitors in the filter within 2% bandwidth accuracy.

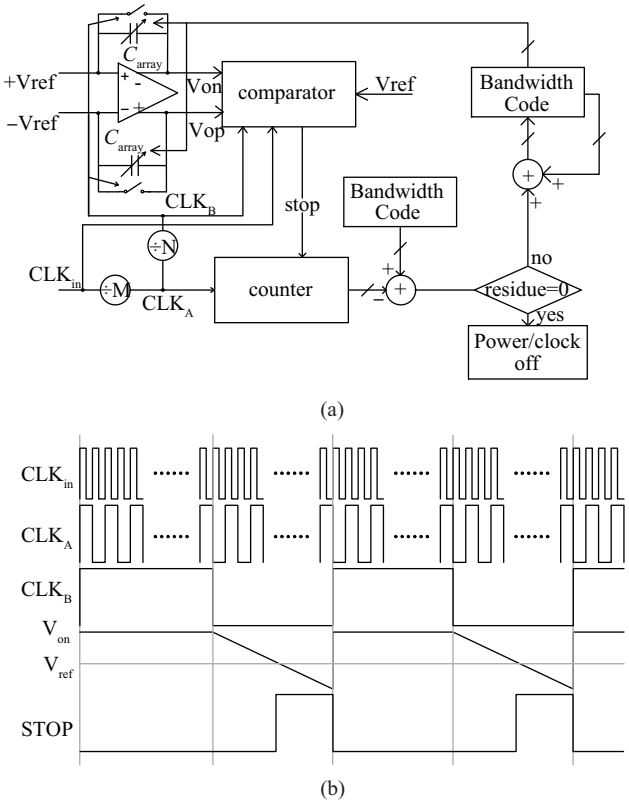

Fig. 6. (a) Architecture of the frequency calibration circuit. (b) Timing diagram of the calibration circuit.

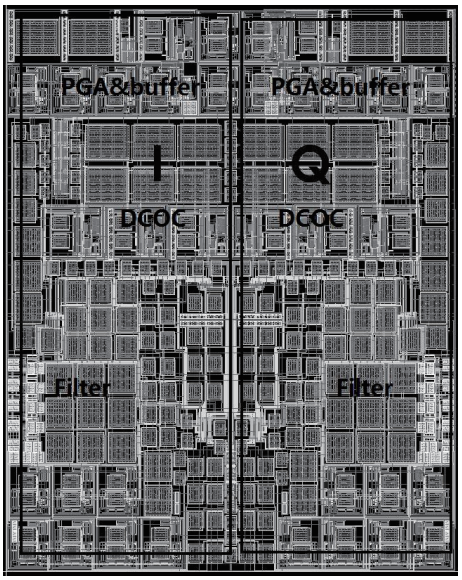

Fig. 7. Baseband layout.

2.5. Simulation results

Figure 7 gives the baseband layout in a DTV tuner. The baseband is implemented in a 0.13-μm SiGe BiCMOS technology, which occupies 0.6 $\mathrm{mm^2}$.

Figures 8 and 9 give the simulated frequency characteristics and attenuation at offsets of 1.25/4 MHz of the filter, respectively. The filter shows a programmable cutoff frequency of 1.78/2.38/2.88/3.41/3.92 MHz with automatic calibration,

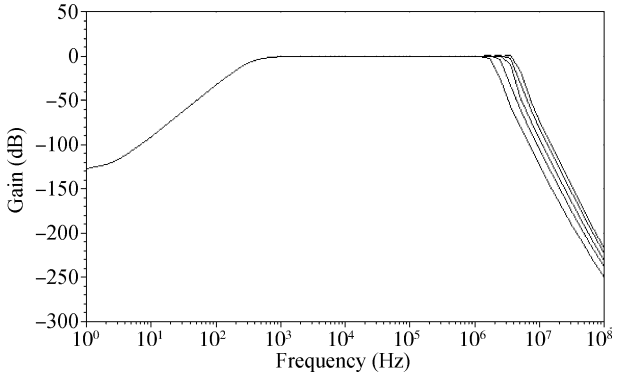

Fig. 8. Simulated frequency characteristics of the filter.

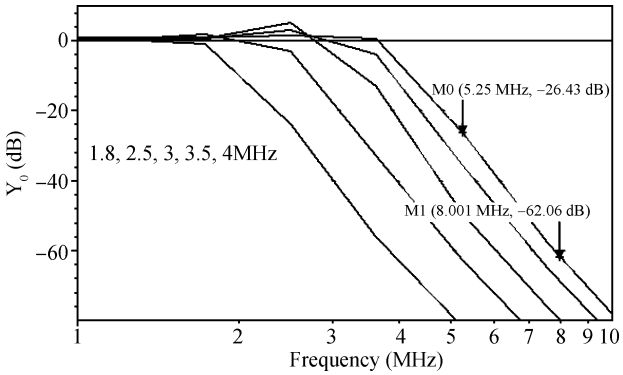

Fig. 9. Simulated filter's attenuation at offsets of 1.25/4 MHz.

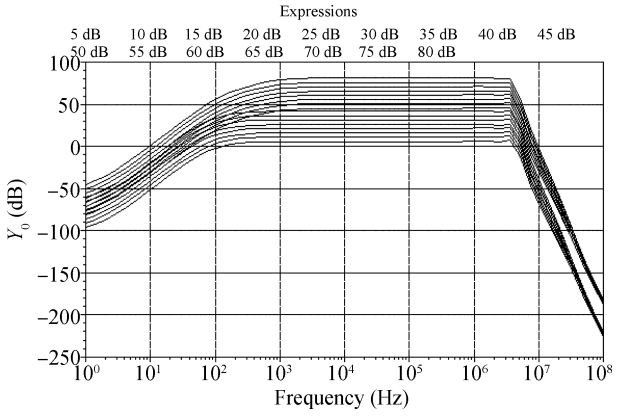

Fig. 10. Simulated baseband gain at 2.5 V.

and the stopband attenuation is more than 26/62 dB at offsets of 1.25/4 MHz.

Figures 10 and 11 give the simulated frequency characteristics of the baseband and the featured high-pass filter's cutoff frequency, respectively. The baseband shows a gain range of 0–80 dB, and the featured HPF's cutoff frequency is about 0.807 kHz.

Figure 12 gives the transient simulation results of the baseband at the maximum gain settings. It shows that when the input signal with a DC offset value of 10 mV, the DC offset component of output signal is less than 1.87 mV.

Figure 13 gives the DC offset cancellation when the DC negative feedback loop turns from on to off. The input DC offset voltage is set to 10 mV.

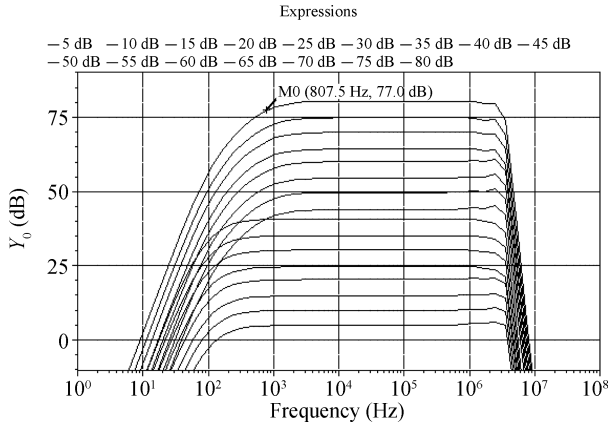

Fig. 11. Simulated featured HPF's cutoff frequency.

Table 1. Summarized performance of the baseband chain.

Parameter	Simulated value
Gain range/Step	0–80 dB/0.5 dB
Max gain/Step error	1 dB/0.1 dB
I/Q gain/Bandwidth imbalance	0.1 dB/0.7%
Input referred noise	45 nV/$\sqrt{\text{Hz}}$
3dB bandwidth	1.78/2.38/2.88/3.41/3.92 MHz
In-band IIP3	23.16 dBm
Attenuation	26/62 dB @ 5.25/8 MHz
DCOC cutoff frequency	$<$ 0.85 kHz @ all gain settings
DCOC remaining voltage	1.87 mV @ max gain
Supply voltage	2.5 V
Current consumption	22.4 mA
Area	0.58 $\times$ 0.6 mm^2

Figure 14 gives the simulated noise figure. The in-band noise figure of baseband chain is less than 36 dB.

Figure 15 gives the simulation result of in-band IIP3. When the input power is 0 dBm, the in-band IIP3 is 23.16 dBm. The baseband performance is summarized in Table 1.

3. Conclusion

This paper presents post-layout simulated results of an analog baseband chain for mobile and multimedia applications in a 0.13-μm SiGe BiCMOS process. A programmable 7th-order Chebyshev LPF with a calibration circuit is used in the analog baseband circuit, and the programmable bandwidth is 1.8/2.5/3/3.5/4 MHz with an attenuation of 26/62 dB at offsets of 1.25/4 MHz. The baseband achieves a linear 80-dB gain range in 0.5-dB steps. The automatic calibration circuit achieves the bandwidth accuracy of 2%. A DC offset cancellation loop is introduced to remove the offset, and the remaining offset voltage is only 1.87 mV. Implemented in a 0.13-μm SiGe technology with 0.6 mm^2 layout size, this baseband achieves IIP3 of 23.16 dBm and dissipates 22.4 mA under a 2.5-V supply.

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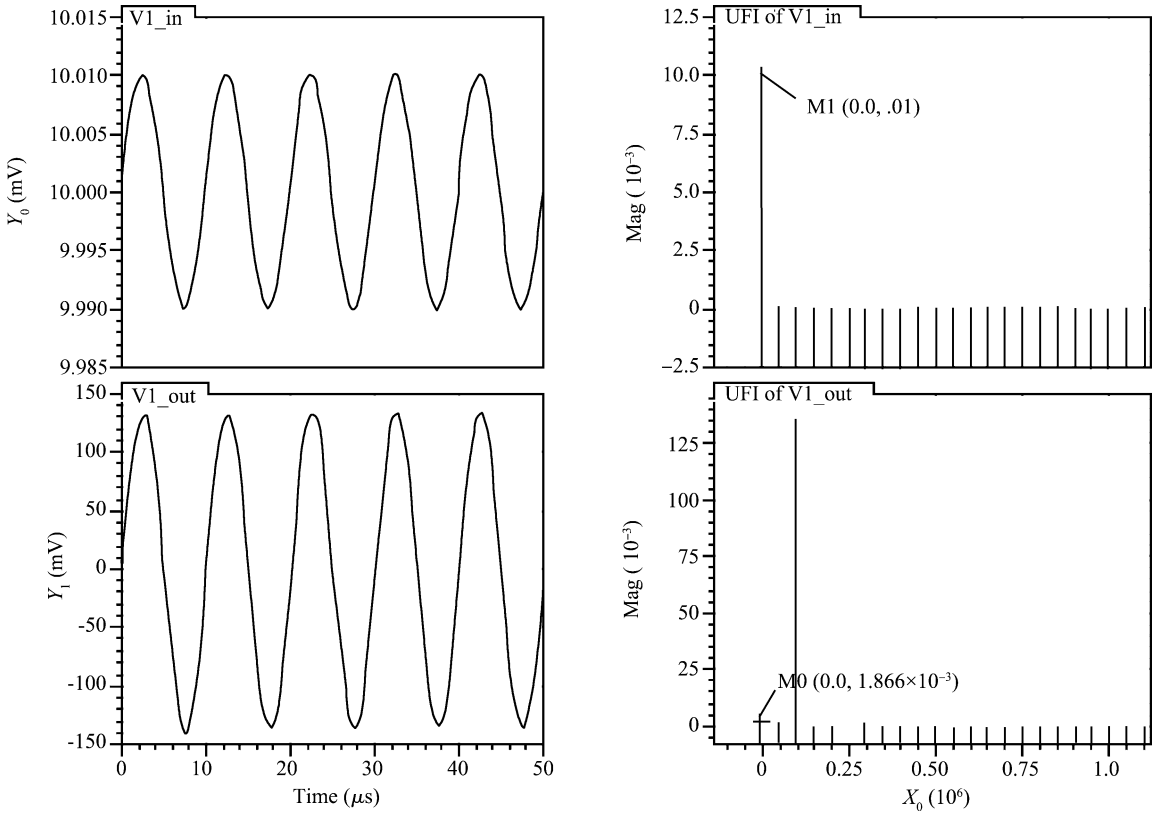

Fig. 12. Simulation results of the remaining DC offset voltage.

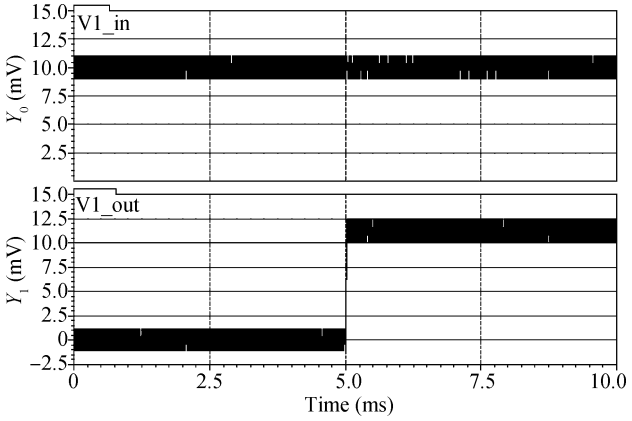

Fig. 13. Simulation results of DC offset cancellation.

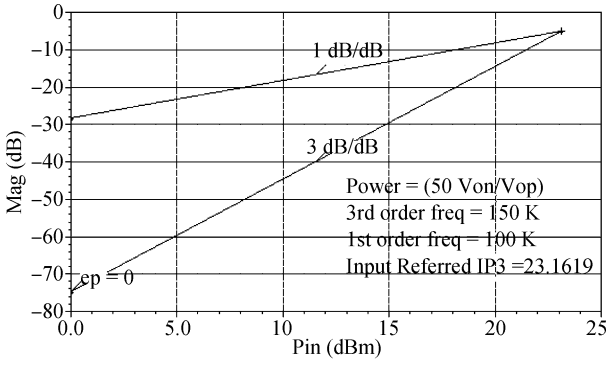

Fig. 15. Simulated in-band IIP3 of 23.16 dBm.

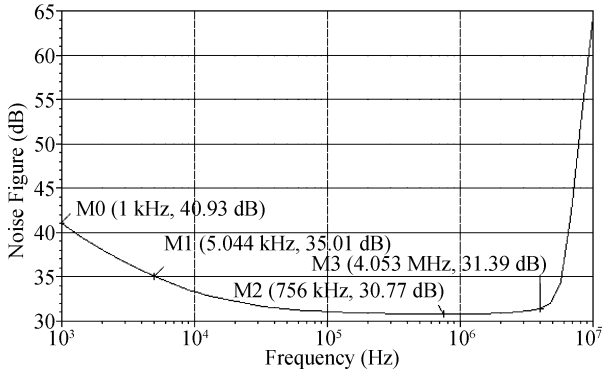

Fig. 14. Simulated noise figure.

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