A 455 nW 220 fJ/conversion-step 12 bits 2 kS/s SAR ADC for portable biopotential acquisition systems*

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Abstract: An ultra-low power 12 bits 2 kS/s successive approximation register analog-to-digital converter (ADC) is presented. For power optimization, the voltage supply of the digital part is lowered, and the offset voltage of the latch is self-calibrated. Targeted for better linearity and lower noise, an improved digital-to-analog converter capacitor array layout strategy is presented, and a low kick-back noise latch is proposed. The chip was fabricated by using 0.18 μm 1P6M CMOS technology. The ADC achieves 61.8 dB SNDR and dissipates 455 nW only, resulting in a figure of merit of 220 fJ/conversion-step. The ADC core occupies an active area of only 674 × 639 μm^2.

Key words: ADC; SAR; low power; biopotential acquisition system

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1. Introduction

In modern clinical practice, the monitoring of biopotential signals (such as ECG and EEG) is a crucial and important part. Commonly, these recordings are uncomfortable for patients, because they will be connected to bulky and main-powered instruments. Therefore, there is a growing demand for portable biopotential acquisition systems[1−3]. Meanwhile, thermoelectric generators, solar cells and even integrated energy-harvesting devices are the optimal power sources for these systems, hence low power consumption should be put primary in the implementation[2, 4]. A typical block diagram of the biopotential acquisition system is shown in Fig. 1. The analog input from the sensor is amplified and filtered at first. Then it will be digitized by the following analog-to-digital converter (ADC), whose clock is generated by the on-chip oscillators. Finally, the digital code will be transmitted outside by the wireless transmitter.

Generally speaking, the power of the biopotential signal centralizes in the bandwidth of lower than 1 kHz[2]. And the SNR will not be higher than 60 dB due to the noise from sensors and amplifiers[5, 6]. Therefore, ADCs with a sampling rate higher than 2 kS/s and a resolution of 12 bits or greater are well suited for this application. In addition, their input range should be large enough to accommodate the voltage swing of the pre-stage, which is 1.8 V in this design. What's more, to achieve power savings, the successive approximation register (SAR) architecture is often adopted because it has been proved to be most power-effective due to minimal active analog circuit requirement[7−12].

This paper presents an ultra-low power 12 bits 2 kS/s successive approximation register analog-to-digital converter (ADC), and describes the systematic considerations in the design and the circuit implementation of the key building blocks in detail.

2. Systematic considerations

2.1. System architecture

There are three types of structures that are widely used in SAR ADC: fully-differential[7−9], pseudo-differential[10], and single-ended[11]. The fully-differential type is most widely used for better common-mode noise rejection and less signal distortion. But it consumes more power and a larger area because there are two DACs connected to the comparator inputs. As an improvement in power reduction, pseudo-differential structure utilizes one DAC only. The other comparator input side is connected to the sampling switch. However, considering both the input voltage and DAC output voltage vary from GND to $V_{\rm DD}$, a comparator with rail-to-rail input range is necessary. What's more, a large sampling capacitor is also needed for suppressing the kT/C noise.

In this design, low-power and small chip area are preferred, so the single-ended architecture is employed. As shown in Fig. 2, one of the two comparator inputs is still connected to DAC, but the other is directly connected to a constant reference voltage $V_{\rm cm}$. The DAC has been separated into a main-DAC and a sub-DAC, both implemented as binary weighted capacitor arrays to save power. No additional sampling capacitor is needed, hence chip area is saved.

2.2. Conversion timing arrangement

As shown in Fig. 3, the ADC conversion starts with a reset phase, during which the charge on the DAC capacitor array is purged and registers are reset. Then, the converter enters into the sampling phase, during which the DAC acts as sampling capacitor and disconnected from the comparator. To save power, the preamplifier is auto-zeroed at the end of sampling phase, and it won't be turned on until the auto-zero phase (AZ_1 and AZ_2) is arriving. It should be noted that the sampling time is

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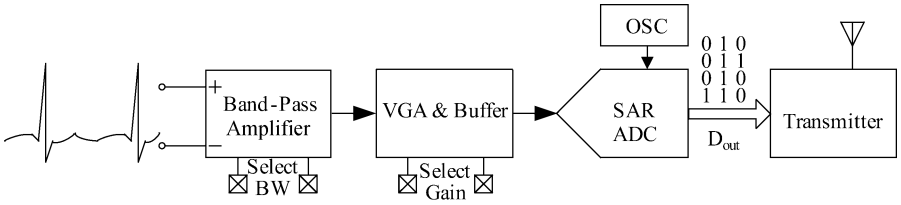

Fig. 1. Block diagram of the biopotential acquisition system.

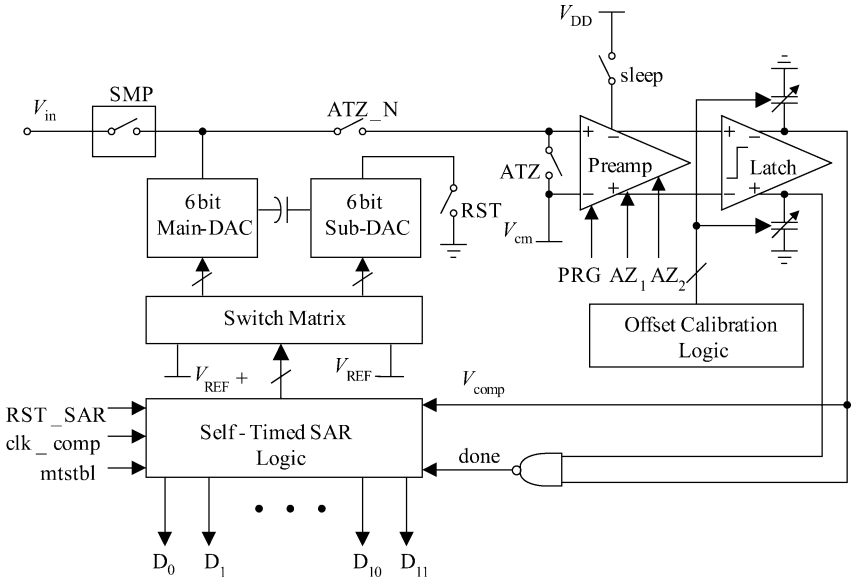

Fig. 2. System architecture of the proposed SAR ADC.

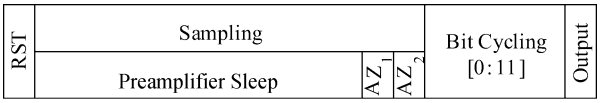

Fig. 3. Simplified timing diagram of the proposed SAR ADC.

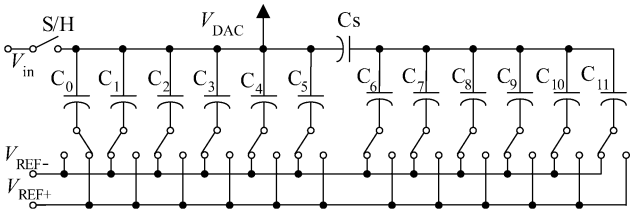

Fig. 4. Schematic of the DAC capacitor array.

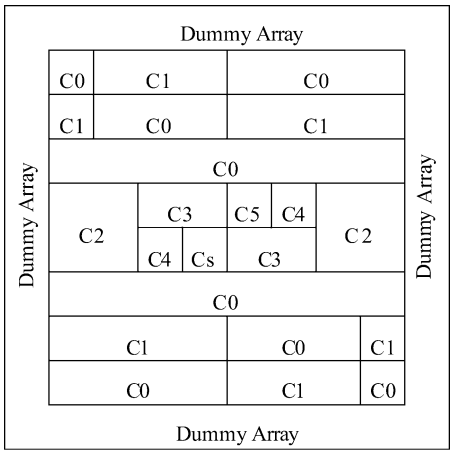

Fig. 5. Layout of the main-DAC capacitor array.

intentionally prolonged to be about 80% of a conversion period. By doing so, there will be more time for voltage settling. Hence the speed requirement for the pre-stage buffer could be relaxed. After the sampling phase, the DAC output voltage approximates V_{cm} using binary search algorithm. In each clock cycle, one bit of ADC output is obtained, and the 12 bits data will be triggered out simultaneously in the output phase.

3. Circuit implementations

3.1. DAC capacitor array

Figure 4 depicts the schematic of the DAC employed in the designed ADC. Compared to conventional architecture, the dummy capacitor is eliminated thus the scaling capacitor C_S is equal to the unit capacitor. By doing so, C_S can scale the sub-DAC better hence a higher accuracy can be achieved[3, 11].

Sizing the unit capacitor plays a crucial role in the DAC designing because that the ADC accuracy is strongly dependent upon the matching and kT/C noise of the DAC capacitor array. Although increasing the value of unit capacitor will improve both matching and noise performance, more power will be dissipated. Therefore, as a tradeoff, the unit capacitor is determined to be 400 fF and implemented as meta–insulator–metal (MIM) capacitors in this design. To achieve a further improvement in capacitor matching, an improved capacitor array layout strategy based on Ref. [7] is pro-

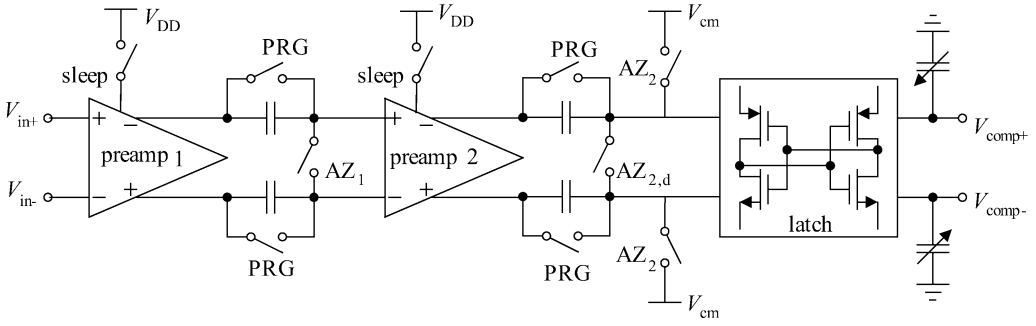

Fig. 6. Schematic of the comparator.

posed, which is shown in Fig. 5. Different from Ref. [7], the location of capacitors is rearranged for better routing[15]. This is important because that the linearity will be deteriorated by the parasitic capacitors from routing line.

As the two reference voltages V_{REF+} and V_{REF-} are set to be V_{DD} and GND, PMOS and NMOS transistors are used as reference switches, respectively. Moreover, the MSB capacitor C_0 is connected to V_{REF+}, and the other capacitors are connected to V_{REF-} during the sampling period. This sampling method achieves rail-to-rail input range without using bootstrapped sampling switch because that V_{DAC} will never be beyond V_{DD}. Therefore, the charge injection error will be significantly reduced.

3.2. Low offset low kick-back noise comparator

The comparator of SAR-ADC is responsible for deciding the polarity between its inputs. As the most power-efficient comparator structure, regenerative latch suffers from large offset voltage and low frequency noise. Therefore, low offset preamplifiers are usually placed before the latch to reduce the input referred offset voltage to smaller than 0.5 LSB. However, the larger offset voltage the latch suffers from, the higher preamplifier gain is required, and more power will be consumed. In this paper, the designed comparator is shown in Fig. 6. To conserve power, the latch is offset-calibrated by adding unbalanced load capacitors[12], yielding a residual offset of about 3 mV. Hence the gain requirement for the preamplifier can be significantly relaxed. Further more, two auto-zeroed preamplifier stages are placed before the latch for further suppression of offset.

Besides offset voltage, the latch also introduces kick-back noise, which will degrade the preamplifier settling[13]. To solve this problem, a low kick-back noise latch is proposed in this paper. Compared with the conventional structure[12], four additional transistors M3, M4, M10, M11 are added, as shown in Fig. 7. First, let's consider the case without these four transistors. When clk is low, the node voltages V_X, V_Y are both pushed to V_{DD} during latch regeneration and they will be pulled to GND when clk jump high. Such a large step of V_X and V_Y will be coupled to the input sides by the gate-drain parasitic capacitor of M1 and M2. Therefore, the preamplifier output will be corrupted due to the mismatch in the parasitic capacitors. Regarding the proposed latch, when clk is low, V_P, V_Q, V_X, V_Y are all pushed to V_{DD}. However, when clk turn high, M3 and M4 turn off and isolate V_P, V_Q from V_X, V_Y. Furthermore, M10

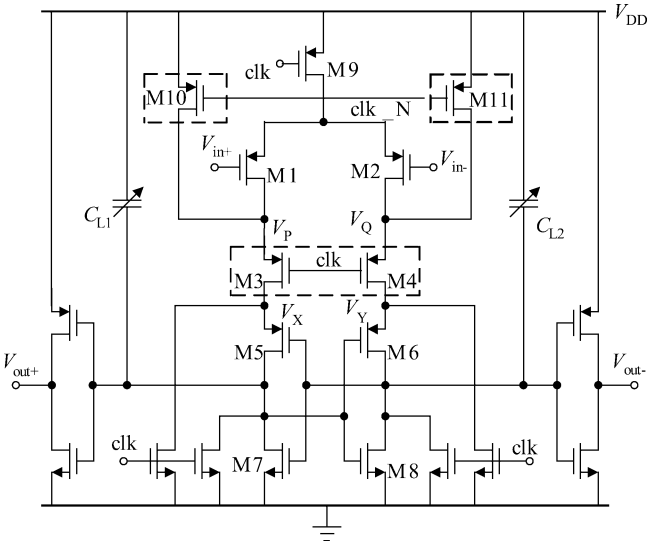

Fig. 7. Schematic of the proposed low kick-back noise latch.

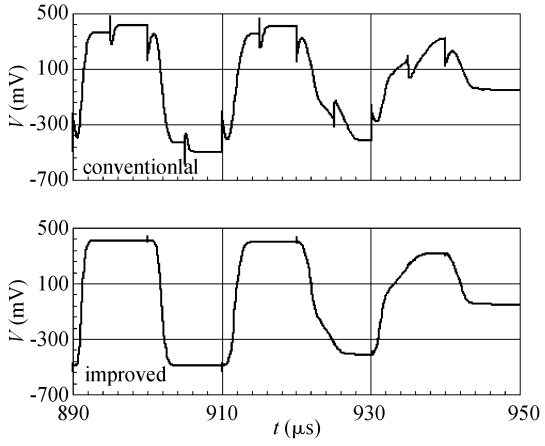

Fig. 8. Simulation result of the latch input signal.

and M11 will turn on and hold V_P, V_Q at V_{DD}. Therefore, there is no voltage change at the drain of M1 and M2, hence no kick-back noise generated. Figure 8 shows the simulation result of the latch input. For conventional structure, it can be clearly seen that there is large glitches, which is caused by the large kick-back noise. As regard to the proposed latch, the input signal is not suffered from kick-back noise and is quite clean.

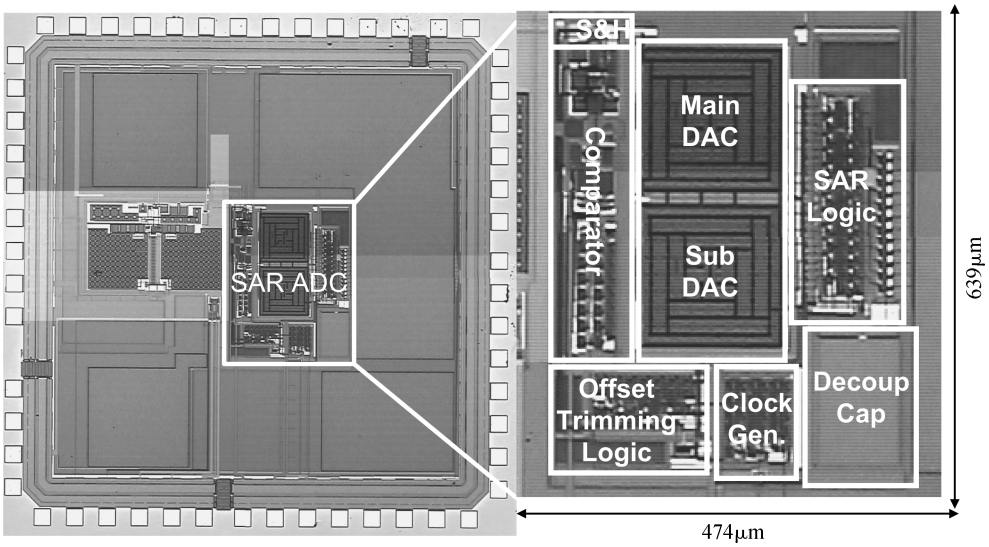

Fig. 9. Chip micrograph.

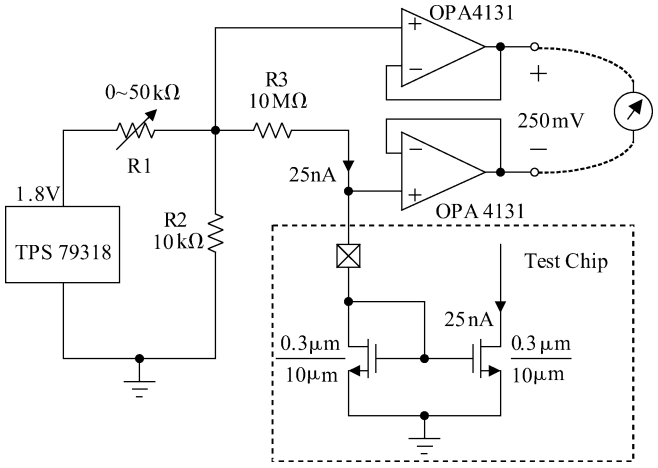

Fig. 10. Bias current generation for the test chip.

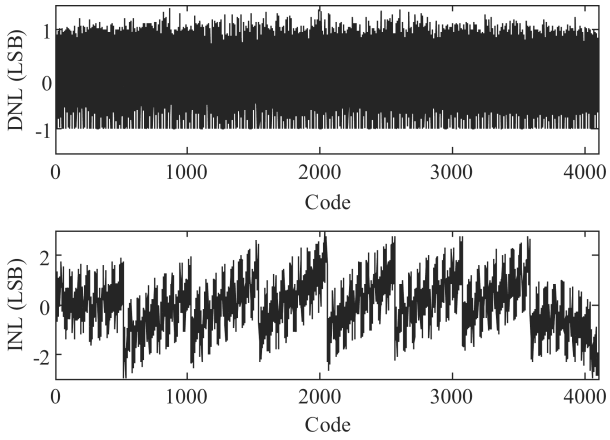

Fig. 11. Measured DNL and INL.

4. Experimental results

The chip was processed in 0.18 μm 1P6M CMOS technology. The microphotograph is shown in Fig. 9. The core size is about 474×639 μm^2.

During the measurement of any ultra-low power chips, the generation of the small bias current is always a hard problem. For example, the bias current of the designed ADC is only 25 nA, which is hard to generate using commercial current source. In this paper, it is generated by biasing the gate voltage of the on-chip current mirror, as shown in Fig. 10. The current flowing into the test chip can be adjusted by R_1, and it can also be measured by detecting the voltage drop across R_3, which is 250 mV in this design. Regarding to the on-chip current mirror, the channel length is designed to be large and W/L is designed to be small for matching considerations.

4.1. Static measurement

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are both shown in Fig. 11. The peak DNL and INL are 1.5/–1 LSB and 3/–3 LSB, respectively. The performance is limited by the parasitic capacitance induced by layout routing. Moreover, the settling speed of comparators in "over-drive" state should also be increased.

4.2. Dynamic measurement

Figure 12 shows the measured output spectrum of the ADC with 1.7 V_{pp}, 47.7 Hz input. The measured SNDR and SFDR are 61.8 dB and 78.7 dB, respectively. It corresponds to an effective number of bit (ENOB) of 10 bits.

Figure 13 illustrates the measurement results of the ADC's SNDR and SFDR versus different input frequencies. The SFDR degrades about 7 dB near the Nyquist frequency. This is mainly because the sampling switch is made small to reduce the charge injection, hence introduces signal distortion at high frequency. However, the SNDR does not degrade too much because that the noise power is much higher than the total harmonic distortions. This also indicates the noise from the DAC and comparator should be reduced.

Table 1. Performance summary and comparison with the state-of-the-art designs.

Specification	This work	JSSC'07[7]	ISSCC'08[11]	JSSC'09[3]	JSSC'10[9]	JOS'10[14]
Technology (μm)	0.18	0.18	0.13	0.35	0.13	0.18
Supply voltage (V)	1.8	1	1	1	1.2	1.8
Sampling rate (kS/s)	2	100	100	1	50000	384
Resolution (bit)	12	12	12	12	10	8
ENOB (bit)	10	10.5	9.4	10.2	9.18	7.4
SFDR (dB)	78.7	71	71.8	74	61.8	51
Power (μW)	0.455	25	3.8	0.233	830	63
FOM (fJ/conv-step)	220	165	56	200	29	970

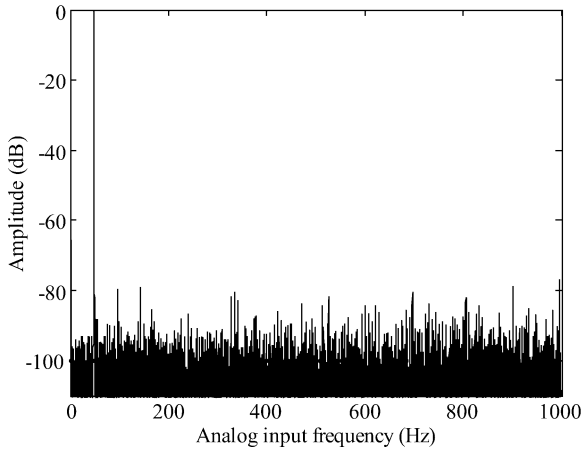

Fig. 12. Measured FFT spectrum with 47.7 Hz input frequency.

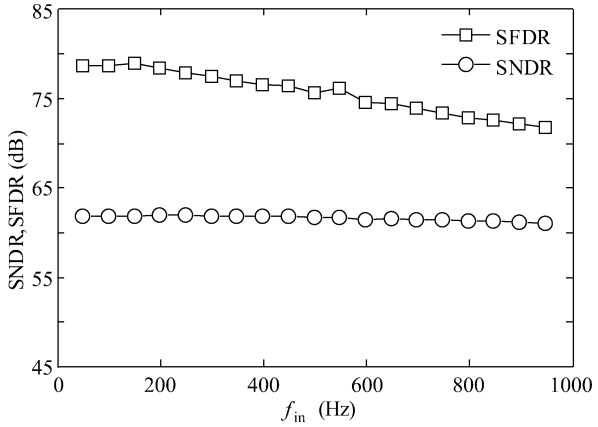

Fig. 13. SNDR and SFDR versus input frequency.

4.3. Power consumption

The current dissipation is so small that it couldn't be detected by the measurement instrumentation. Therefore, the post simulation result that considers the parasitic parameters is presented here. Under a 1.8 V analog supply, the comparator consumes about 100 nW, the DAC capacitor array dissipates 210 nW. The SAR logic and clock manager dissipate 145 nW under a 1 V digital supply. The ADC power distribution among these functional blocks is shown in Fig. 14. For further reduction in power consumption, the digital power consumption must be reduced. This can be done either by lowering the digital supply voltage, or utilizing thick-gate transistors to decrease the parasitic capacitances.

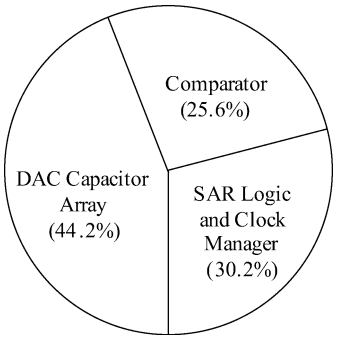

Fig. 14. ADC power distribution.

4.4. Comparison and discussion

To compare the proposed ADC with other designs having different sampling rates and resolutions, the well-known figure-of-merit (FOM) is utilized, which is defined as

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} f_{\text{S}}}. \quad (1)$$

The FOM of the proposed ADC is 220 fJ/conversion-step. Table 1 lists the comparison results. Although a much lower FOM is achieved compared with Ref. [14], but it is still much larger than that reported in Ref. [9], which is only 29 fJ/conversion-step. This is mainly because a much higher reference voltage is utilized in this design to accommodate the large voltage swing of the pre-stage. Besides, the design in Ref. [9] didn't take any precautions against the comparator offset voltage, hence no static power dissipated by the comparator. However, considered that this design is applied in sensor networks, offset cancellation is necessary because several sets of data are gathered at the same time and offset will introduce errors.

5. Conclusions

An energy-effective 12 bits 2 kS/s SAR ADC was presented in this paper. Low power strategies are emphasized throughout the design. An improved DAC capacitor array layout method is presented and a low kick-back noise latch is proposed. The designed ADC achieves a peak SNDR of 61.8 dB and a peak SFDR of 78.7 dB, as well as a rail-to-rail input range. From the energy perspective, the proposed ADC achieves an FOM of 220 fJ/conv-step and dissipated only 455 nW. Although the ADC was designed for use in biopotential acquisition system, it can also be used in other low speed, high resolution applications.

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