A low-power triple-mode sigma–delta DAC for reconfigurable (WCDMA/TD-SCDMA/GSM) transmitters*

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Abstract: A sigma–delta ($\Sigma\Delta$) DAC with channel filtering for multi-standard wireless transmitters used in the software-defined-radio (SDR) system is presented. The conversion frequency, transfer function of the digital filter and the $\Sigma\Delta$ modulator, word-length of the IDAC and cut-off frequency of the analog reconstruction filter can be digitally programmed to satisfy specifications of WCDMA, TD-SCDMA and GSM standards. The $\Sigma\Delta$ DAC fabricated in SMIC 0.13-μm CMOS process occupies a die area of 0.72 mm^2, while consuming 5.52/4.82/3.04 mW in WCDMA/TD-SCDMA/GSM mode from a single 1.2-V supply voltage. The measured SFDR is 62.8/60.1/75.5 dB for WCDMA/TD-SCDMA/GSM mode, respectively.

Key words: $\Sigma\Delta$ digital-to-analog converter; low-power; reconfigurable

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1. Introduction

Wireless communication terminals are demanding longer battery life and more operation modes, which are the two key issues for software-defined-radio (SDR) systems. Generally speaking, utilizing the scaled-down of the state-of-art technologies which provides lower supply voltage and smaller feature size can benefit both power and area cost. In designing DACs used in transmitters, two of the effective ways to save the power consumption are reducing word-length of the DAC and releasing the requirements on the following analog reconstruction filter. Improving the reconstructive ability is the key element to lower the overall cost to meet variety of emerging wireless standards. Reported multi-mode DACs[1, 2] used in transmitters adopt the architecture of traditional current-steering DAC, reducing the DAC word-length by over-sampling techniques and reconfiguring only by adjusting the conversion and filter cut-off frequency.

This paper presents a sigma–delta ($\Sigma\Delta$) architecture with a multi-bit IDAC that has less power consumption due to word-length reduction and can be digitally programmed with great flexibility. The conversion frequency, transfer function of the digital filter and the $\Sigma\Delta$ modulator, word-length of the IDAC and cut-off frequency of the analog reconstruction filter can be digitally programmed to satisfy specifications of WCDMA, TD-SCDMA and GSM standards. By changing the clock rate of the digital part, taps of the digital filter and bias current of analog reconstruction filter, the power consumption is optimized for different operation modes. Besides, since both digital filter and $\Sigma\Delta$ modulator are digital circuits, IDAC and analog construction filter are simpler compared to the traditional ones, this architecture is more suitable to be implemented in an advanced technology.

2. System architecture and reconfigurable method

As indicated by the standard, the quality of the transmitted signal is specified evaluating the error-vector-magnitude (EVM) and its power out of band has to be sufficient low as specified by the emission mask. Therefore, the resolution and linearity performances of the DAC block, mainly determined by SNR and SFDR, are considered in this design.

The theoretical in-band SNR of $\Sigma\Delta$ modulator[3] is:

$$\mathrm{SNR}_{\text{In-Band}} = 6.02L + 1.76 - 10\lg\frac{\pi^{2N}}{2N+1} + 10(2N+1)\lg\mathrm{OSR}, \quad (1)$$

where L is the output word-length of the quantizer, N is the order of the modulator, and OSR is the over-sampling-ratio. From Eq. (1), it can be observed that increasing OSR, L and N can improve the in-band SNR.

The block diagram of the reconfigurable $\Sigma\Delta$ DAC is depicted in Fig. 1. It is mainly composed of four blocks, a digital filter, a $\Sigma\Delta$ modulator, a current-steering DAC (IDAC) and an analog reconstruction filter. Because the digital part is comparatively simple and the power supply is only 1.2 V, the power dissipation of the DAC is mainly composed of the one of the IDAC (P_{IDAC}) and the analog reconstruction filter (P_{Filter}). For a certain SNR, P_{IDAC} is inversely proportional to the OSR and directly proportional to the number of unary current sources, which is determined by L in Eq. (1). While P_{Filter} is proportional to the order and inversely proportional to the cut-off frequency of the analog filter under a given SNR and signal bandwidth. Hence, higher $\mathrm{SNR}_{\text{In-Band}}$ of the $\Sigma\Delta$ modulator, which releases the stress on the transition band steepness and attenuation requirements of the analog reconfigurable filter, can reduce P_{Filter}.

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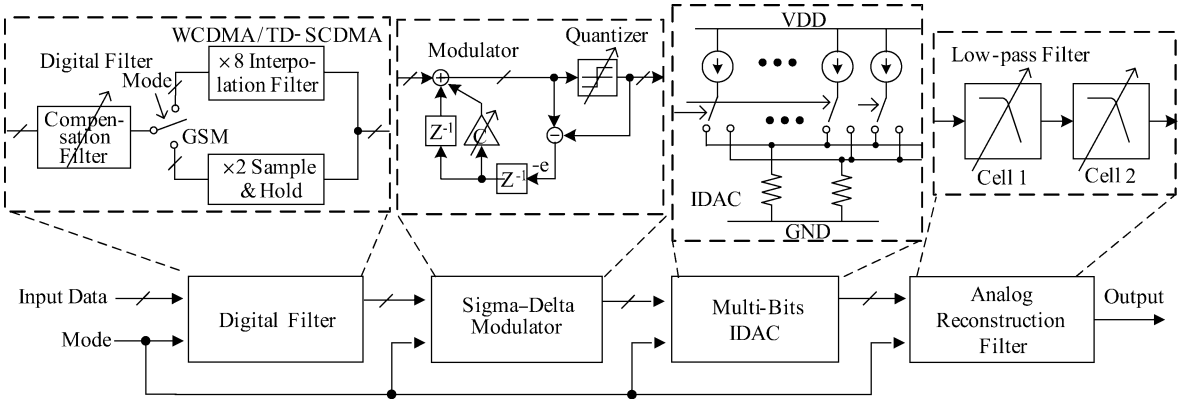

Fig. 1. General block diagram of the ΣΔ DAC.

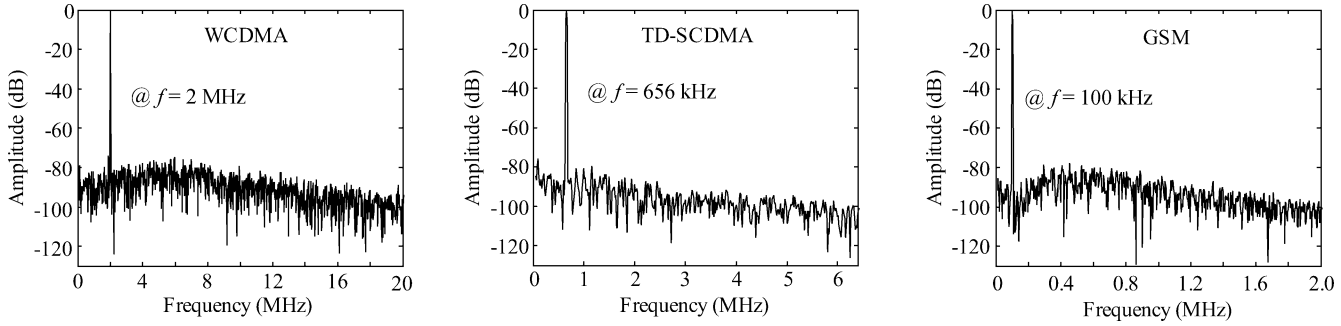

Fig. 2. Spectrum of the behavior-level simulation.

Table 1. Features of the reconfigurable ΣΔ DAC.

Mode	In-band SNR requirement (dB)	Data rate of baseband interface (MHz)	Signal bandwidth (MHz)	Conversion frequency (MHz)	Modulator order	Word-length of the quantizer (bit)
WCDMA	56	15.36	1.92	122.88	2	3
TD-SCDMA	59	15.36	0.64	122.88	2	3
GSM	62	12.8	0.1	25.6	2	1.5

Based on the discussion above, tradeoffs have been made among the conversion frequency (OSR × $2F_S$), the quantizer word-length (L) and the modulator order (N) under a given SNR requirement to minimize the total power.

The features of the reconfigurable ΣΔ DAC are listed in Table 1.

The digital filter in Fig. 1 is used to reduce the total ripples induced by the analog reconstruction filter and the sample-and-hold circuits and suppress the closest images at the frequency of the baseband interface data rate to meet the demand of spectrum emission mask. For different operation modes, the clock rate and taps of this block are adjusted for the sake of power reduction.

The modulator is implemented with a 2nd order error-feedback (EFB) structure, which is free of signal distortion and different phase-delay and can be easily reconstruct for different quantization levels because the comparatively simpler structure and the exactly realized coefficients. It works under a 122.88/122.88/25.6 MHz clock and word-length of the quantizer is 3/3/1.5 for WCDMA/TD-SCDMA/GSM mode, respectively. Since zeros of NTF influence the total noise power in the signal band, the coefficient C is optimized for the best SNR according to different operation modes.

The multi-bits IDAC, constituting with 6 unary current-sources, can be reconfigured from a 3-bit one to a 1.5-bit one according to the word-length of the quantizer by different decoding ways.

The following analog reconstruction filter is designed to filter the out-of-band quantization noise and it can be programmed to adjust the cutoff frequency to meet the requirements of different standards. To save power, the bias current of analog reconstruction filter is optimized for different operation modes.

The single-tone behavior simulation results are depicted in Fig. 2 for all the three modes. The cut-off frequencies of both filter cells are set to 5/2.5/0.45 MHz for WCDMA/TD-SCDMA/GSM mode, respectively.

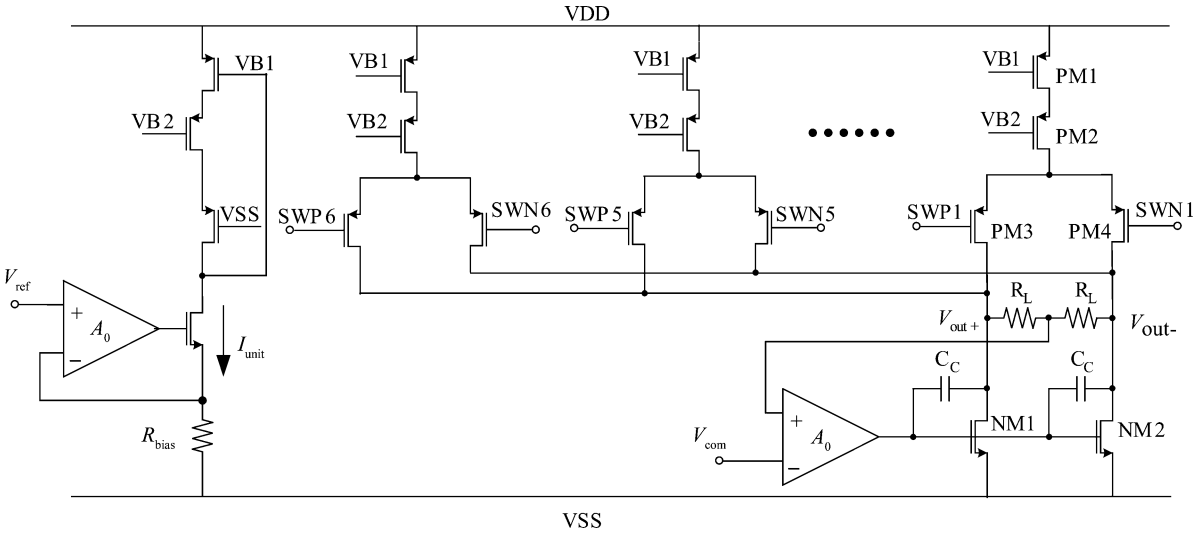

Fig. 3. Schematic of the IDAC.

3. Circuit implementation

3.1. Digital filter and ΣΔ modulator

In the implementation of the digital part, several efforts are taken to save the power and hardware cost, such as placing the compensation filter before the interpolation operations as shown in Fig. 1 to work under a lower frequency, realizing the digital filter in transposed form which can shorten the critical path to reduce the multiplication operations and transferring the filter coefficients to the canonic sign digit (CSD) representations[4] so that the multiplications can be completely substituted by the fewest shift-and-add operations. In the modulator with EFB structure, the digital limiter usually placed in front of the quantizer to avoid the round-off phenomenon is omitted, owing to a safe margin in the hardware circuit has been left.

3.2. IDAC

The IDAC design has been focused on the optimization of dynamic performance and power consumption. The schematic of the IDAC is shown in Fig. 3, including 6 unary current-sources. Each source is implemented with the cascode structure and its current $I_{\text{unit}} = V_{\text{ref}}/R_{\text{bias}}$. The output voltage is:

$$V_{\text{out}} = (2m-6)I_{\text{unit}}R_{\text{L}} = (2m-6)V_{\text{ref}}\frac{R_{\text{L}}}{R_{\text{bias}}}, \qquad (2)$$

where m represents the number of current-sources switched to the positive node. From Eq. (2), it can be observed that the full-scale output amplitude of the IDAC only depends on the match degree between R_{L} and R_{bias}. And the full-scale output voltage of the analog reconstruction filter is:

$$A_{\text{F}} = A_{\text{In}}\beta_{\text{D}}\frac{A_{\text{D}}}{\text{QR}/2}\beta_{\text{A}}, \qquad (3)$$

where A_{F} and A_{D} represent the full-scale output amplitude of the filter and the IDAC, β_{D} and β_{A} is the digital and analog filter attenuation factors, and A_{In} and QR represent the full-scale input amplitude and quantity-range of the modulator, respectively. Therefore, given a DAC output range, the ratio of R_{L} to R_{bias} can be figured out according to Eqs. (2) and (3).

Usually the larger the unit current, the better SNDR can be obtained[6]. The relationship can be expressed as follows when a full-scale sinusoidal signal is applied at the input:

$$\text{SNDR} = \frac{(2nI)^2/\left(2\sqrt{2}\right)^2}{\text{BW}\times\left(\overline{I}_{\text{eq1}}^2+\overline{I}_{\text{eq2}}^2\right)\left(n+\dfrac{n^2}{h}\right)+\dfrac{I^2}{12\times\text{OSR}}+\dfrac{P_{\text{d}}}{\text{OSR}}}, \qquad (4)$$

where n is equal to the number of unary current-sources, BW is the bandwidth in which the SNDR is evaluated, h presents the mirror ratio between unit current generation transistor and unary current source transistor, P_{d} is the mean power of distortion, and $\overline{I}_{\text{eq1}}^2$ and $\overline{I}_{\text{eq2}}^2$ are the integrated thermal and flicker noise density of the current source in the band of interest, respectively. According to Eq. (4), a 64-μA unary current is chosen for WCDMA and TD-SCDMA modes and a 128-μA unary current is chosen for GSM mode by making tradeoffs between the SNDR and the power consumption.

Considering only the output SNR is concerned by the TX chain, the area of the current-source is mainly determined by its affections on the dynamic performance instead of the INL or DNL in ordinary ways. And the behavior simulations indicate that a relative standard deviation σ/I of 0.1% is acceptable, for the deterioration on SNR is smaller than 2 dB. So, according to the Pelgom model[3]:

$$\frac{\sigma^2}{I^2} = \frac{1}{WL}\left(A_\beta^2+\frac{4A_{\text{Vt}}^2}{V_{\text{ov}}^2}\right), \qquad (5)$$

where V_{ov} is the overdrive voltage, A_β, A_{Vt} are technology dependent parameters ($A_\beta = 0.0138$ μm, $A_{\text{Vt}} = 5.19$ mV·μm), and assuming $\sigma/I = 0.1\%$ and $V_{\text{ov}} = 0.2$ V, which is the tradeoff between the low sensitivity to threshold voltage change and the available headroom from 1.2-V power supply, a minimal area (WL) of 2900 μm^2 is obtained.

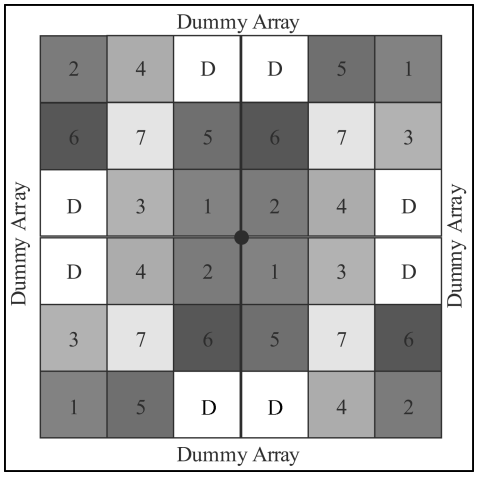

Fig. 4. Floorplan and switching arrangement of the current sources.

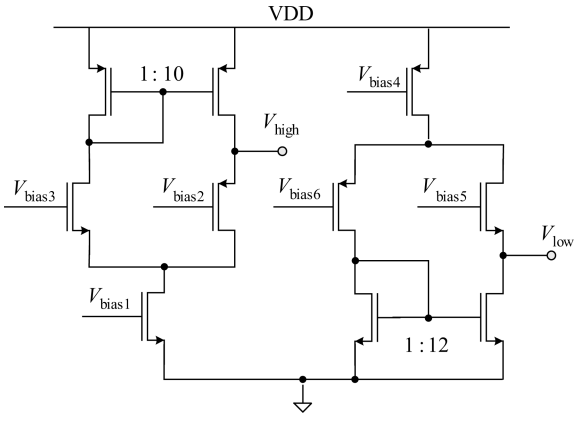

Fig. 5. Schematic of the switch voltage generator.

Based on the discussion above, each current source is implemented with $W = 96 \times 4$ μm and $L = 8$ μm (3072 μm^2).

In GSM mode, two 64-μA current sources constitute one 128-μA unary one and the doubled area ensures less SNR attenuation induced by mismatch for the higher requirement (10-bit).

The floorplan and the switching arrangement are shown in Fig. 4; 'hierarchical switching scheme'[3] has been adopted to cancel both the linear and quadratic errors. Four cells with the same number formed one current source and dummy transistors are placed around the current sources array to ensure that all the source transistors have the same boundary conditions. By this way, the current sources can match with each other better.

Data-dependent interference and switch glitches are two of the main elements that affect the dynamic performance. Therefore, for synchronization, the constant clock latch[8] is adopted here to provide a constant load for the clock. And the glitches are reduced by minimizing the voltage swing of the switch control signals. The switch-on (V_{low}) and switch-off (V_{high}) voltage of the PMOS switches are set to 240 mV and 550 mV, respectively. In order to save the static power of the IDAC, these two voltages are generated by using the circuit shown in Fig. 5, which can produce a large transient current when biased at a small one.

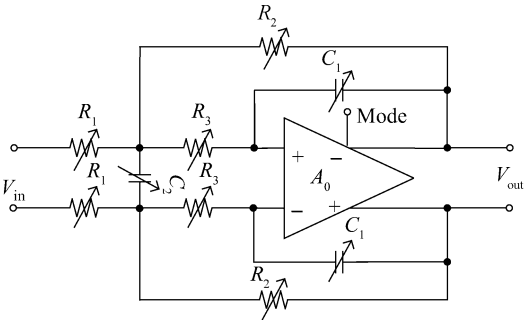

Fig. 6. 2nd order Sallen-key filter

All the circuits of the IDAC are reused for all modes and it consumes 760 μA (0.912 mW) totally.

3.3. Analog reconstruction filter

The analog reconstruction filter in Fig. 1 is realized by cascading two 2nd-order Sallen-key filters. The schematic of filter cell is shown in Fig. 6.

The transfer function of the filter is:

$$H(s) = \frac{-R_2/R_1}{2R_2R_3C_1C_2S^2 + (R_2 + R_3 + R_2R_3/R_1)C_1S + 1}. \quad (6)$$

By setting the parameters as

$$R_1 = R,\ R_2 = AR,\ R_3 = mR,\ C_1 = C,\ C_2 = nC, \quad (7)$$

where A is the gain of the filter. Then quality factor (Q) and the cut-off frequency (f_{cutoff}) are given by

$$Q = \frac{\sqrt{2mn}}{1 + m + Am}, \quad (8)$$

$$f_{cutoff} = \frac{1}{2p\sqrt{2mn}RC}. \quad (9)$$

When A, requirement of SNR, Q and f_{cutoff} are fixed, m, n, R and C can be figured out from Eqs. (8) and (9). For Bessel filter, Q is set to $1/\sqrt{3}$.

In this design, the cutoff frequency is required to be programmable in order to satisfy the bandwidth requirements of the considered standards. According to Eq. (9), the cutoff frequency can be modified by adjusting R or C or both of them. Although the SNR requirement of GSM standard is more stringent than that of WCDMA standard, the narrower bandwidth allows for larger noise floor. And the noise floor of $\Sigma\Delta$ DAC is mainly determined by the noise floor of the analog reconstruction filter, including the thermal noise of the resistors and both the thermal noise & $1/f$ noise of the feedback amplifier. If C_1 and C_2 in Fig. 6 are kept the same for WCDMA mode and GSM mode, the thermal noise contributed by R_1, R_2 and R_3 for WCDMA mode will be far below the desired. So in order to satisfy the SNR requirement for both standards and minimize the power consumption, the cutoff frequency is modified by adjusting R and C at the same time. Both R and C in Eq. (9) for GSM mode are greater than that for WCDMA mode.

It also can be seen from Eq. (9) that the cutoff frequency is dependent on the product of R and C, which are affected by

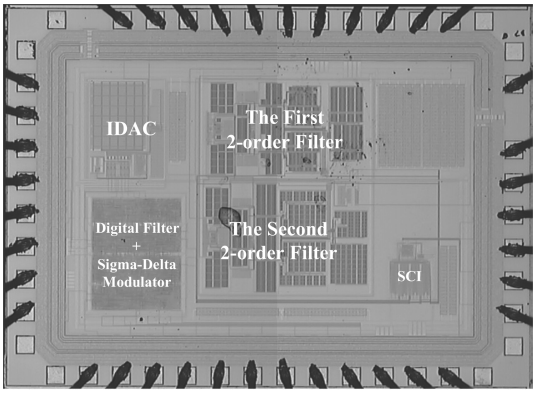

Fig. 7. Die microphotograph.

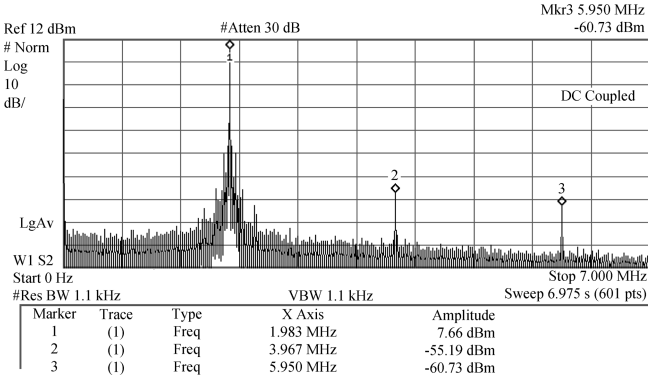

Fig. 8. Measured output spectrum with a 2-MHz F_S sinusoid tone (WCDMA standard).

process fluctuation greatly and varies about ±30% for different technology corners. Therefore, a 4-bit digital control circuit is used to adjust the values of C_1 and C_2 in order to keep the variation of the cutoff frequency less than 10% of the desired value.

Since the cutoff frequency for GSM mode is much smaller than that for WCDMA and TD-SCDMA mode, the UGB of the feedback amplifier in Fig. 6 is adjusted by reducing its bias current for GSM mode. The current consumption of the whole analog reconstruction filter is 2.41 mA and 1.20 mA for WCDMA/TD-SCDMA mode and GSM mode, respectively.

All the reconfigurable switches are placed next to the low impedance nodes (the input nodes and the feedback amplifier outputs) or the virtual ground nodes (the inputs of the feedback amplifier) to reduce the nonlinearity caused by the switch equivalent resistance which varies with the voltage across it.

To minimize the area occupation, the capacitor arrays are reused as much as possible.

4. Experimental results

The proposed triple-mode reconfigurable ΣΔ DAC has been processed in a 0.13-μm CMOS process. The chip core occupies an area of 0.9×0.8 mm^2 (excluding pads and SCI block). The die photo is shown in Fig. 7.

The device operates with a single 1.2-V supply voltage and the DAC clock is set to 128 MHz for WCDMA and TD-SCDMA mode and 26 MHz for GSM mode.

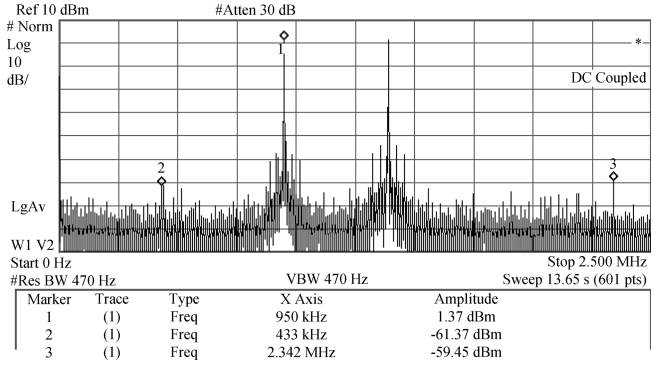

Fig. 9. Measured output spectrum with two –6 dBFS sinusoid tone (WCDMA standard).

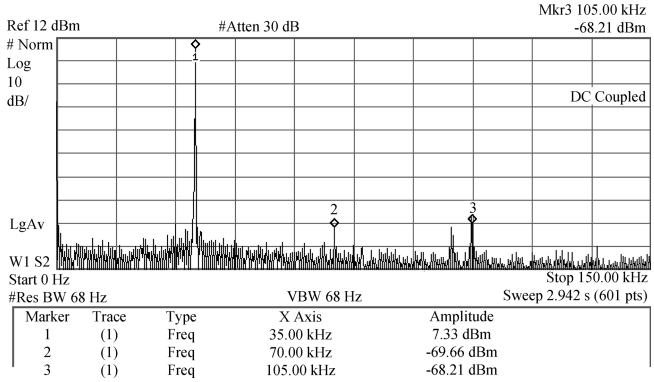

Fig. 10. Measured output spectrum with a 35-kHz F_S sinusoid tone (GSM standard).

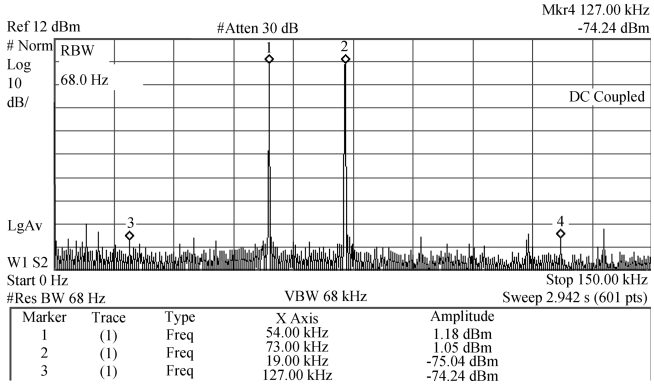

Fig. 11. Measured output spectrum with two –6 dBFS sinusoid tone (GSM standard).

The dynamic performance of the DAC has been verified with single tone tests as well as the intermodulation tests.

For WCDMA setting, a 62.8-dB SFDR has been measured with a full-scale 2-MHz (precisely 1.984375-MHz) single tone as shown in Fig. 8. The measured IMD is 60.8 dB when two –6 dBFS tones centered at 1.2 MHz (1 MHz and 1.4 MHz) are applied at the input as shown in Fig. 9.

For TD-SCDMA setting, a single tone (640-kHz) SFDR of 60.1-dB and an IMD (300-kHz and 500-kHz input tones) of 59.3dB are measured.

While for GSM setting, a single tone (35-kHz) SFDR of

Table 2. Performance summary and comparison.

Parameter	This work			Ref. [1]		Ref. [2]	
Technology	CMOS 0.13 μm			CMOS 0.13 μm		CMOS 0.13 μm	
Supply voltage (V)	1.2			1.2		1.2	
Core area (mm^2)	0.72			0.8		0.9	
Standard	WCDMA	TD-SCDMA	GSM	WLAN	UMTS*	WLAN	UMTS
Differential F_S output swing (mV_{pp})	764	827	735	1800	1800	1400	1400
SFDR @ F_S(dB)	62.8 (@ 2 MHz)	60.07 (@ 640 kHz)	75.5 (@ 35 kHz)	54 (@ 3 MHz)	61 (@ 0.6 MHz)	58 (@ 3 MHz)	60 (@ 0.6 MHz)
IMD @ –6 dBF_S (dB)	60.8	59.27	75.3	52	60	59	N/A
DR @ F_S (dB)	58.1 (9.35 bits)	60.53 (9.76 bits)	65.4 (10.56 bits)	55 (8.8 bits)	58 (9.3 bits)	52 (8.3 bits)	56 (9 bits)
Filter power consumption (mW)	2.89	2.89	1.44	5.6	3	8.4	5.9
Total power consumption (mW)	5.52	4.8	3.0	11	8.4	19.4	16.8

* Here, UMTS and WCDMA represent the same communication standard.

75.5-dB and an IMD (50-kHz and 70-kHz input tones) of 75.3 dB are evaluated from Figs. 10 and 11.

The main performances of this DAC are summarized in Table 2 and compared to two similar reconfigurable ones presented in Refs. [1, 2].

5. Conclusion

A low-power triple-mode sigma–delta DAC for reconfigurable (WCDMA/TD-SCDMA/GSM) transmitters is presented. All the DAC conversion frequency, the transfer function of the digital filter and the sigma–delta modulator, the word-length of the IDAC, the bandwidth and bias current of the analog reconstruction filter can be programmed for different operation modes. Several efforts are made to save the space and power consumption in circuit implementation. The device is implemented in SMIC 0.13-μm CMOS technology with a core area of 0.72 mm^2. It operates from a single 1.2-V power supply and consumes 4.6/4.0/2.5 mA for WCDMA/TD-SCDMA/GSM mode, respectively. The measured SFDR and IMD for WCDMA/TD–SCDMA/GSM are 62.8/60.1/74.6 dB and 60.8/59.3/75.3 dB respectively.

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