A low power 12-bit 200-kS/s SAR ADC with a differential time domain comparator*

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Abstract: A low power 12-bit 200-kS/s SAR ADC is proposed. This features a differential time domain comparator whose offset is cancelled by using a charge pump and a phase frequency detector instead of the preamplifiers usually needed in a high resolution comparator. The proposed ADC is manufactured in 0.18-μm CMOS technology and the measured SNR and SNDR are 62.5 dB and 59.3 dB, respectively, with a power consumption of 72 μW at a 200-kS/s sampling rate. The device operates with a 1.8-V power supply and achieves a FOM of 477 fJ/conversion-step.

Key words: successive approximation register; A/D; differential time domain comparator
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1. Introduction

Low power design has become the main concern for battery-powered portable applications, such as environmental monitoring and biomedical detection[1−3]. SAR ADC (successive approximation register analog-to-digital converter) architecture has proved to be very suitable for these applications because of its high power efficiency.

The comparator, charge/discharge of the capacitive DAC and SAR control logic are primary sources of power consumption in a SAR ADC. Digital power consumption becomes lower with technology scaling-down, while the power consumption of the comparator and capacitor network is limited by mismatch and noise. The power consumption of a capacitive DAC is proportional to the number of unit capacitors and the charge/discharge of the capacitor array by the switching sequence, so power efficiency can be achieved by reducing the total capacitance of the DAC. A conventional comparator used in a high resolution ADC consists of preamplifiers and a latch, and the preamplifiers consume much static power. A time domain comparator is proposed in Ref. [2] to enhance the power efficiency, however, its offset is cancelled by an off-chip method, and the performance of the ADC is limited by the second-order harmonics and common mode error due to the single-ended configuration[2]. To overcome the problem mentioned above, a differential time domain comparator with on-chip offset cancellation is proposed in this paper.

2. Architecture and operation of the proposed ADC

Figure 1 shows the architecture of the proposed ADC. The ADC consists of a charge redistribution DAC, a differential time domain comparator, SAR logic and control logic. Figure 2 shows the architecture of the charge redistribution DAC, which consists of two capacitor arrays and switches controlled by SAR and control logic. A differential DAC structure is adopted to suppress the common mode error and even-order harmonics caused by a single-ended structure[2]. For each capacitor, four switches are connected to the bottom plate, $V_{\rm in}+$ and $V_{\rm in}-$ are differential input signals, the common mode voltage($V_{\rm com}$) is for purging the capacitors, and the positive reference voltage ($V_{\rm refp}$) and the negative reference voltage ($V_{\rm refn}$) are reference voltages for comparison. The differential time domain comparator is composed of a differential voltage to time converter (V2T), a phase and frequency detector (PFD) and a charge pump. The charge pump and the PFD are used for offset cancellation.

As shown in Fig. 1, when the reset signal is high, the offset of the comparator is cancelled and the SAR logic is initialized. The conversion requires 20 clock periods of the main clock: the first for purging capacitors, 2 periods for input sampling, 12 periods for the successive approximation cycles and the last 5 for offset refinement.

The purging phase is for purging all of the charge stored in the capacitors before sampling the signal in order to shorten the settling time of the sampling phase. During the purging phase, the top and bottom plates of the capacitors are shorted to purge all stored charge.

In the sampling phase, the sampling switches are switched on and the input signal is sampled at the bottom plates of the capacitor arrays and the top-plates are shorted, and therefore their voltage stays at the input common mode voltage. In the conversion phase, all of the sampling switches are switched off, and the bottom plates of the capacitors are switched to $V_{\rm refp}$ or $V_{\rm refn}$ controlled by SAR logic.

The waveform of the DAC switching procedure is illustrated in Fig. 3. The comparator determines whether $V_{\rm dacp}$ is higher than $V_{\rm dacn}$ during the conversion phase. If $V_{\rm dacp}$ is higher than $V_{\rm dacn}$, the corresponding bit of SAR is set to "1"; otherwise it is set to "0". The ADC repeats the above mentioned conversion step until the LSB is resolved.

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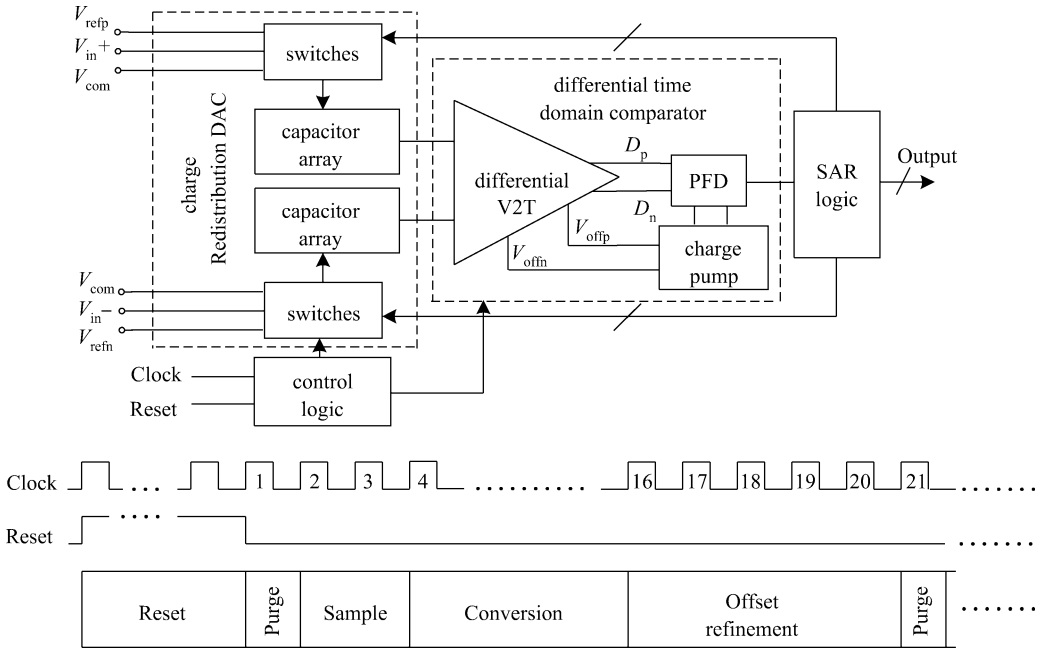

Fig. 1. Proposed SAR ADC architecture.

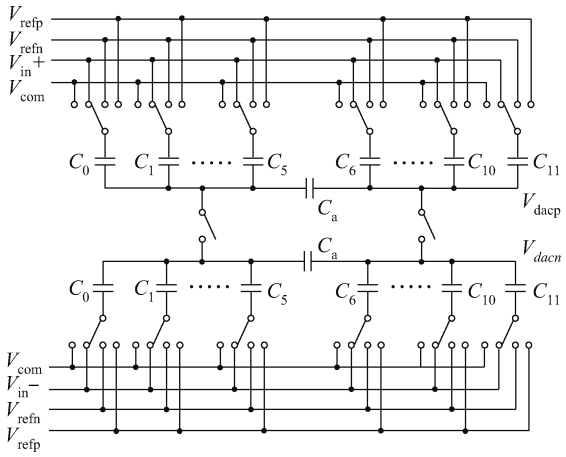

Fig. 2. Charge redistribution DAC.

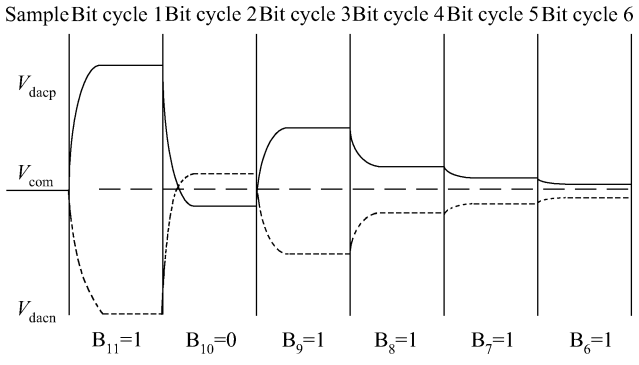

Fig. 3. Waveform of DAC switching procedure.

3. Implementation of key blocks

3.1. Differential time domain comparator

The schematic of the proposed differential voltage to time converter is shown in Fig. 4. When the signal Clk = 0, the nominally equal capacitors C_P and C_N will be charged to V_{DD} through M3 and M8, the parasitic capacitance at node E will be discharged to ground through M11, and $D_p = D_n = 0$.

When Clk rises, M2 and M7 will be switched on and capacitors C_P and C_N will be discharged. The discharging currents depend on the differential input ($V_{dacp} - V_{dacn}$). When the voltage drops at nodes A and B across the threshold voltage of M4 and M10 in Fig. 4, D_p and D_n will rise.

The PFD shown in Fig. 1 will detect which of D_p and D_n rises first and provides the comparator output. Once the comparison result is resolved, signal ctrl will fall and switch off M2 and M7 to reduce the power consumption.

The power consumption of the differential V2T is related to the input signals V_{dacp} and V_{dacn}, and the maximum power consumption in one period, T, can be calculated as

$$P = \frac{2V_{DD}V_{THP}C}{T}, \tag{1}$$

where V_{THP} is the threshold voltage of PMOS, $C_P = C_N = C$, and T is the period of signal Clk. The power consumption of the differential time domain comparator is mainly from the dynamic power of charging and discharging capacitors C_P and C_N, so low power supply voltage, long clock period and small capacitors can reduce power consumption.

When the differential input is 1 LSB of the ADC, the discharging currents of C_P and C_N are nearly the same, and discharge of C_P and C_N should be completed in $T/2$, so the following condition should be satisfied,

$$T > \frac{4CV_{THP}}{I_{R_S}}, \tag{2}$$

where I_{R_S} is the current through R_S and inversely proportional to R_S. According to Eq. (2), small C and R_S can promote the speed of the differential V2T.

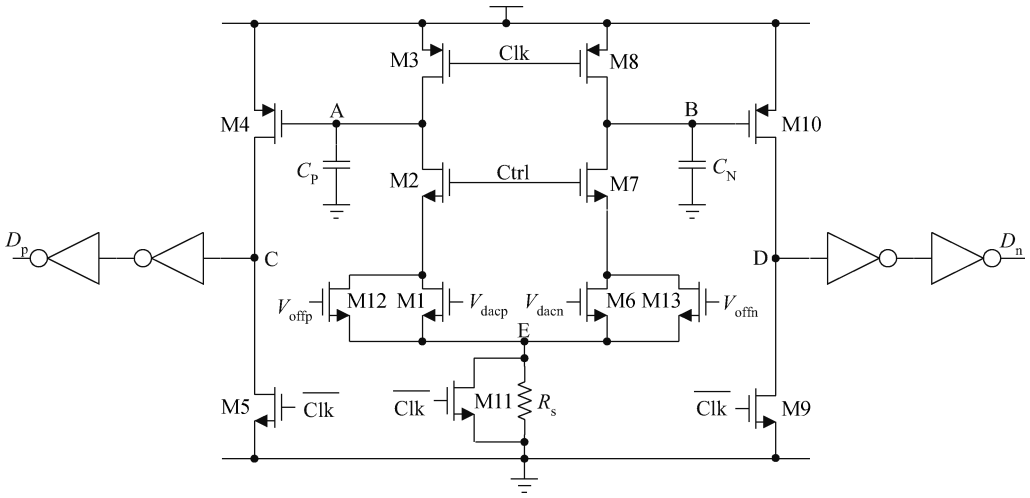

Fig. 4. Schematic of proposed differential voltage to time converter.

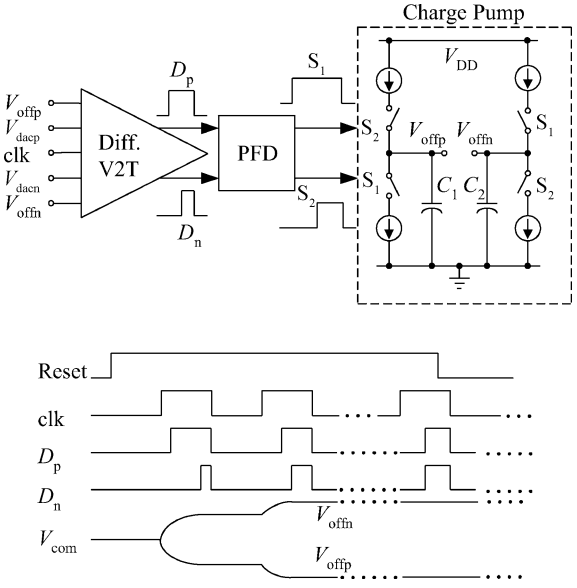

Fig. 5. Offset cancellation procedure.

However, for the minimum differential input, the time between the rise edges of D_p and D_n, Δt, should be larger than the dead-zone of PFD, and this difference can be enlarged by increasing C and R_S.

So compromises should be made among the power, speed and resolution by designing C_P, C_N and R_S properly.

The mismatch between the symmetrical devices in Fig. 4 causes an input-referred offset of about several mVs. It is cancelled by the PFD and the charge pump shown in Fig. 1. Figure 5 illustrates the offset cancellation procedure. V_{offp} and V_{offn} are set to V_{com} to charge C_1 and C_2, and then disconnected. The phase difference of D_p and D_n is directly proportional to the input-referred offset of the comparator and can be reduced by controlling the charge pump to charge or discharge the capacitors C_1 and C_2 to generate an offset compensating voltage ($V_{offp} - V_{offn}$), which is converse to the input-referred offset. To eliminate the performance degradation caused by charge leakage from C_1 and C_2, they are refreshed in the offset refinement phase.

The aspect ratio of transistors M12 and M13 is properly designed to reduce the residue of offset after cancellation. A PFD with dynamic logic DFF[4] is used to reduce its dead-zone and a modification of charge pump in Ref. [5] is adopted for better current matching and greater speed.

3.2. DAC

The total power consumption of the charge redistribution DAC is proportional to the total capacitance and the switching frequency. For a 12 bit SAR ADC, a large unit capacitor is necessary to diminish the nonlinearity caused by the mismatch of the capacitors, and the total capacitance of a conventional binary weighted capacitor array is $2^{11}C_U$ (C_U is the unit capacitor). Since the conventional binary weighted capacitor arrays will consume a large amount of power, a power efficient capacitor array is adopted.

Figure 6 shows the capacitor array. This is implemented with two 6-bit binary weighted capacitor arrays coupled by an attenuation capacitor. A unity capacitor attenuation capacitor is adopted instead of a fractional one, and the dummy capacitor in the LSBs part is removed. This will cause a gain error of DAC, which does not increase the nonlinearity. The area of the proposed capacitor array is just approximately $1/2^5$ of the area of the conventional binary weighted capacitor array.

Figure 7 shows the layout placement of the capacitor array. The equal edge ratio common-centriod layout[6] is adopted for better matching. In a conventional common-centroid layout, as illustrated in Fig. 7(a), the largest capacitors are C_5, C_4 and C_3 and the number of their outside edges is 24, 4 and 2. So they would suffer from disproportional parasitic capacitance between the top plates and the dummy array because of disproportional outside edges. Since the error of the largest capacitors imposes the most impact on the linearity of the DAC, it is necessary to adjust the outside edges of the largest capacitor proportionally. As illustrated in Fig. 7(b), the number of outside edges of C_5, C_4 and C_3 are adjusted to 18, 10 and 4, respectively, which are approximately binary weighted.

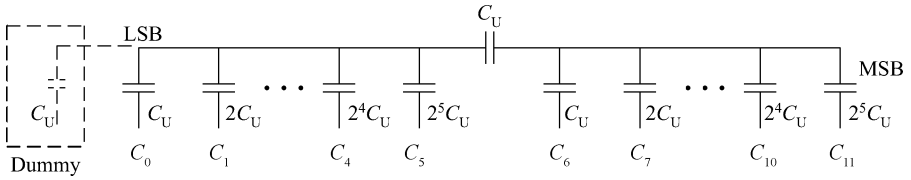

Fig. 6. Proposed capacitor array.

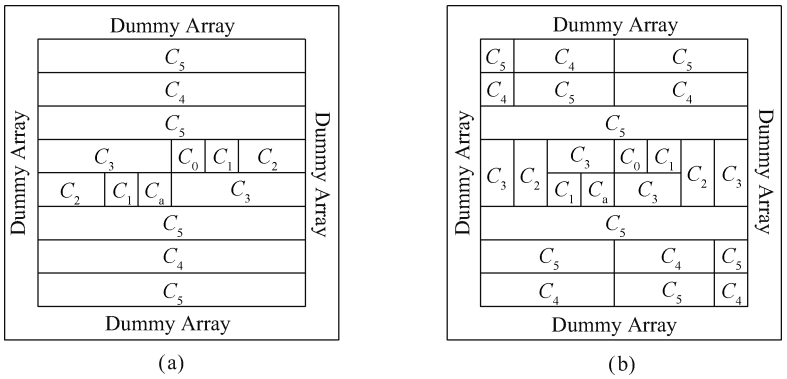

Fig. 7. Layout of capacitor array. (a) Conventional common-centroid. (b) Equal edge ratio common-centroid.

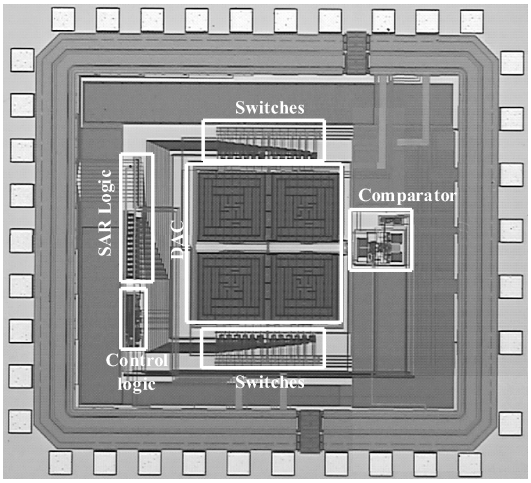

Fig. 8. Photograph of the ADC prototype.

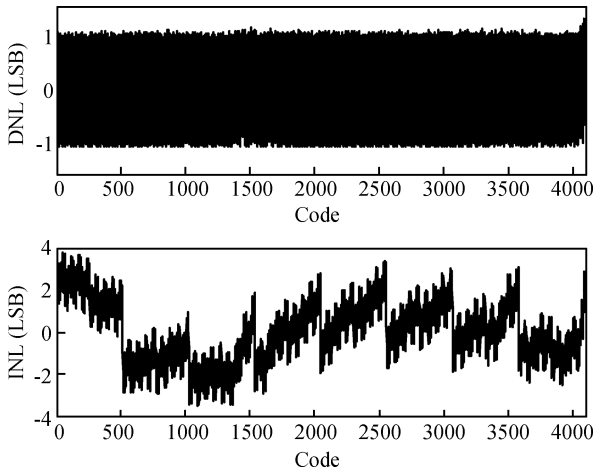

Fig. 9. Measured DNL and INL.

4. Experimental results

The low power ADC is manufactured by 0.18-μm 1P6M CMOS technology. A photomicrograph of the ADC prototype is shown in Fig. 8. The total die area including pads is 2 × 2 mm^2 with a core area of 0.7 × 0.9 mm^2.

The DNL and INL of this converter are measured with the code density method using a full-swing, differential sinusoidal input with an amplitude of 1 V. Figure 9 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) with respect to the output code. The maximum DNL is 1.3/–1.0 LSB, while the maximum INL is 3.5/–3.6 LSB.

The signal-to-noise-plus-distortion ratio (SNDR) of the ADC is derived using tone testing. The output spectrum is measured when a 97 kHz sine wave is fed into the chip at a sampling frequency of 200 kHz. A fast Fourier transform (FFT) of the ADC output is shown in Fig. 10; the SFDR and SNDR of the converter are respectively 62.3 dB and 59.3 dB. The variations in SNR, SNDR with respect to the input frequency are shown in Fig. 11. It is demonstrated in Fig. 11 that SNDR is dominated by the 3rd harmonic, which is caused by the nonlinearity of the input switch resistance. Figure 12 shows the 2nd and 3rd harmonics versus input frequency. It can be seen

Table 1. Summary of performance.

Parameter	Value
Process	SMIC 0.18-μm 1P6M CMOS
Supply voltage	1.8 V
Input range	2 V_{p-p}, differential
Sampling rate	200 kS/s
Power	72 μW
INL	+3.6/–3.45 LSB
DNL	+1.3/–1 LSB
SNR @ 97 kHz	62.5 dB
SNDR @ 97 kHz	59.3 dB
SFDR @ 97 kHz	62.3 dB
ENOB	9.56 bits
FOM	477 fJ/conversion-step

Table 2. Comparison with recently published work.

Parameter	ISIC'07[7]	JSSC'07[2]	ISSCC'08[1]	VLSI'09[8]	JOS'10[9]	This work
Architecture	SAR	SAR	SAR	SAR	SAR	SAR
Technology (μm)	0.18	0.18	0.18	0.13	0.18	0.18
Resolution (bits)	12	12	12	12	8	12
Sampling rate (kS/s)	20	100	100	10000	384	200
Supply voltage (V)	0.9	1	1	1	1.8	1.8
ENOB (bits)	7.11	10.55	9.4	10.07	7.4	9.56
DNL (LSB)	0.33/–0.62	0.19	N/A	0.8/0.8	0.7	1.3/–1
INL (LSB)	0.4/–1.69	0.16	N/A	3.0/3.0	1.2	+3.6/–3.45
Power (μW)	0.099	25	3.8	3570	63	72
FOM (fJ/conversion-step)	358	165	56	311	970	477

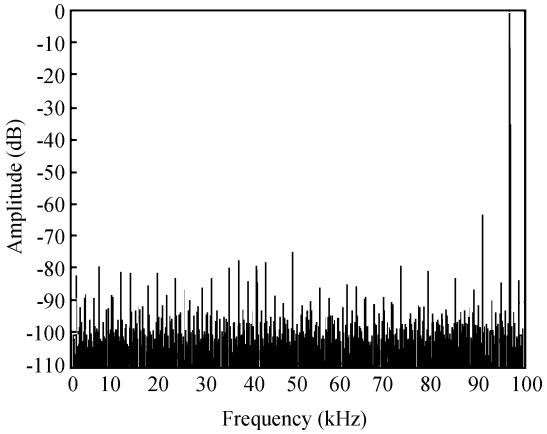

Fig. 10. FFT Plot of the ADC with an input of 97 kHz.

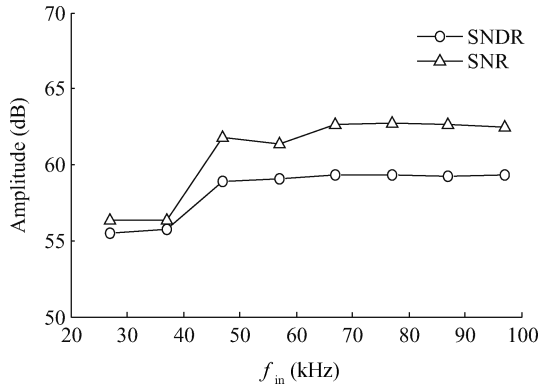

Fig. 11. SNDR and SNR versus input frequency.

that the 2nd harmonic is greatly suppressed compared with the testing results in Ref. [2].

The effective numbers of bits (ENOB) is 9.56 bit at the input frequency of 97 kHz from Eq. (3),

$$\mathrm{ENOB} = \frac{\mathrm{SNDR(dB)} - 1.76}{6.02}. \tag{3}$$

The total power is 72 μW with a power supply of 1.8 V. The figure-of-merit (FOM) is calculated according to Eq. (4), and the ADC achieves a FOM of 477 fJ/ conversion-step,

$$\mathrm{FOM} = \frac{P}{2 \times f_{\mathrm{in}} \times 2^{\mathrm{ENOB}}}. \tag{4}$$

The summary of performance is presented in Table 1. Table 2 compares this work to recently published work on SAR

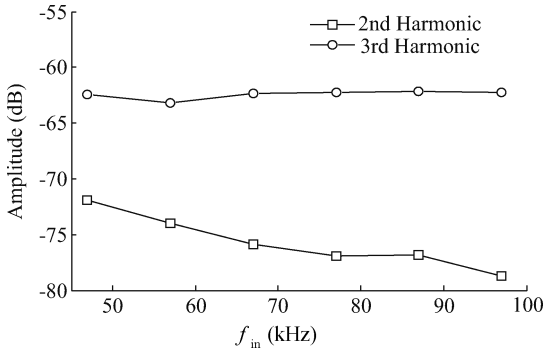

Fig. 12. The 2nd and 3rd harmonic versus input frequency.

ADC. The FOM of this work is several times larger than the results in Ref. [2] because of a higher power supply and the differential architecture in this design. However, in this design, the even-harmonics are effectively suppressed and the offset of the comparator is cancelled with on chip circuitry, which is important for SOC applications. To improve the design, the power supply (1.8 V in this design) can be lowered and the unit capacitor (388 fF in this design) in the capacitor array of DAC can be minimized. The sampling switches can also be improved to reduce the distortion.

5. Conclusion

A low power SAR ADC with a differential time domain comparator is designed and manufactured by a 0.18-μm CMOS process. The offset of the comparator is cancelled by a PFD and a charge pump. The proposed ADC achieves 200-kS/s operation speed with power consumption of 72 μW. It has an ENOB of 9.56 bits and a FOM of 477 fJ/conversion-step.

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