

Forward gated-diode method for parameter extraction of MOSFETs*

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Abstract: The forward gated-diode method is used to extract the dielectric oxide thickness and body doping concentration of MOSFETs, especially when both of the variables are unknown previously. First, the dielectric oxide thickness and the body doping concentration as a function of forward gated-diode peak recombination–generation (R–G) current are derived from the device physics. Then the peak R–G current characteristics of the MOSFETs with different dielectric oxide thicknesses and body doping concentrations are simulated with ISE-Dessis for parameter extraction. The results from the simulation data demonstrate excellent agreement with those extracted from the forward gated-diode method.

Key words: forward gated-diode method; recombination–generation current; parameter extraction; MOSFETs

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1. Introduction

With the aggressively scaling down of MOSFETs to sub-0.1 micrometers, interface states and gate oxide traps have become significant reliability concerns during measurement and parameter extraction^[1–7]. Except for interface state analysis, device parameter extraction is another key issue for industry since most parameters are hardly measured directly^[8–13]. Thus, methods for extracting parameters such as dielectric oxide thickness and body doping concentration are urgently needed. However, fewer parameter extraction methods are introduced to extract device parameters correctly with the serious impact of the interface states.

Recently, a sensitive and accurate forward gated-diode method has been used to characterize the interface traps and extract the bulk carrier recombination lifetime in the MOSFET devices by measuring the R–G current^[14,15]. In this article, this method is further introduced to extract parameters such as the dielectric thickness and the doping concentration of the MOSFET devices, and the results show excellent agreement with the ISE-Dessis simulation.

2. MOSFETs' parameter extraction using the forward gated-diode method

Based on the Shockley–Read–Hall recombination theory, the recombination rate R is obtained as

$$R = \left(n_i^2 \exp \frac{qV_{bs}}{kT} - n_i^2 \right) \left[\tau_n \left(\frac{n_i^2 \exp \frac{qV_{bs}}{kT}}{n} + n_i \exp \frac{E_i - E_t}{kT} \right) + \tau_p \left(n + n_i \exp \frac{E_t - E_i}{kT} \right) \right]^{-1}, \quad (1)$$

where n is the density of electrons at the front surface, n_i is the intrinsic silicon carrier concentration, V_{bs} is the substrate voltage, and τ_n and τ_p are lifetime of the electrons and holes, respectively.

To find out the maximum R_{max} , $dR/dn = 0$ is solved by supposing $\tau_n = \tau_p = \tau$.

$$n = p = n_i \exp \frac{qV_{bs}}{2kT}. \quad (2)$$

Equation (2) indicates that n equals p when the R–G current reaches the peak.

The schematic view of the MOSFET device used in this study is shown in Fig. 1 and the parameters of the device are shown in Table 1. The substrate is biased at a low, positive voltage, which is appropriate $V_{bs} = 0.3$ V. The drain and source are grounded and the gate bias is swept from -0.6 to -0.1 V. The drain and the substrate are formed as a diode, which is controlled by the gate.

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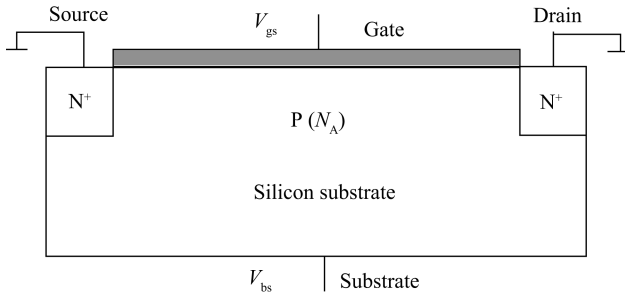


Fig. 1. Schematic structure of the MOSFET biased as a forward gate-diode device.

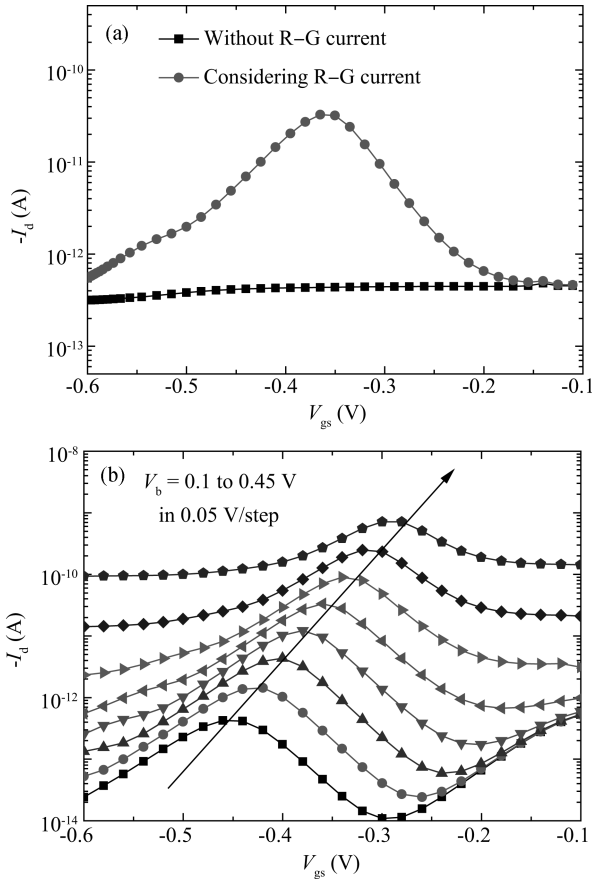


Fig. 2. I_d - V_g curves. (a) Drain current and the drain current without R-G current. (b) Surface R-G current while scanning the gate voltage.

Table 1. Parameters of the device.

Parameter	Length of channel	Width of channel	N^+/P^+ doping
Value	1.4 μm	1 μm	$1 \times 10^{20} \text{ cm}^{-3}$

When the gate voltage varies from -0.6 to -0.1 V, the front surface shifts from accumulation to depletion, and the surface R-G current covers a high percentage of the drain current, over 98% in the peak current, which is shown in Fig. 2(a). The maximum R-G current appears when the intrinsic Fermi level consists with the middle of the two quasi Fermi levels at the surface of the silicon/oxide. The shift of the peak R-G current with different V_{bs} simulated by ISE is shown in Fig. 2(b).

Under the condition of the maximum recombination rate,

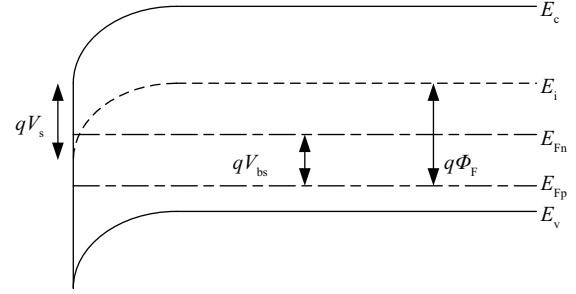


Fig. 3. Energy band of the MOSFET when applying V_{bs} .

substrate voltage V_{bs} is supplied which is separated the quasi Fermi energy level of the electron and hole. The band diagram in the substrate is shown in Fig. 3. The intrinsic Fermi level is supposed just in the middle of the two quasi Fermi levels at the surface of Si/Oxide. The surface potential is obtained as

$$V_s = \phi_F - V_{bs}/2. \quad (3)$$

Here, ϕ_F is the Fermi energy and V_s is the surface potential. The relationship between the gate voltage and the surface potential is written as

$$V_{gs} = V_{FB} + V_s + \gamma_B \sqrt{V_s} + V_{bs}, \quad (4)$$

where γ_B is the body effect coefficient and V_{FB} is the flat band voltage and is equated as $V_{FB} = \phi_{MS} - Q_{ox}/C_{ox}$, ϕ_{MS} is the difference of the work function between the N type polysilicon and the silicon. $\phi_{MS} = -0.55 - \phi_F$. Q_{ox} is the fixed charge in the gate silicon region. In this experiment, the variable is set to zero.

Combining Eqs. (3) and (4), the gate voltage corresponding to the maximum R-G current is

$$V_{peak} = -0.55 + \frac{V_{bs}}{2} + \gamma_B \sqrt{\phi_F - V_{bs}/2}. \quad (5)$$

In Eq. (5), $\phi_F = (kT/q)\ln(N_A/n_i)$ and $\gamma_B = T_{ox}(2\epsilon_0\epsilon_{Si}qN_A)^{0.5}/\epsilon_0\epsilon_{SiO_2}$, where N_A is the body doping concentration, T_{ox} is the dielectric oxide thickness, k is the Boltzmann constant, T is the room temperature, and q is the electron charge. Therefore, the relationship between body doping concentration and dielectric oxide thickness is found via Eq. (5).

In the simulation, T_{ox} is obtained by the following equation based on Eq. (5) with known N_A ,

$$T_{ox} = \frac{\epsilon_0\epsilon_{SiO_2} \left(V_{peak} + 0.55 - \frac{V_{bs}}{2} \right)}{\sqrt{2\epsilon_0\epsilon_{Si}qN_A(\phi_F - V_{bs}/2)}}, \quad (6)$$

where $\phi_F = (kT/q)\ln(N_A/n_i)$, that is to say, as far as V_{peak} is obtained, the dielectric oxide thickness is extracted.

For another condition, the body doping concentration N_A is also obtained by knowing T_{ox} previously. Although there is no simple expression for N_A , it is observed that Equation (7) is monotonous with the N_A variable,

$$N_A \left(\frac{kT}{q} \ln \frac{N_A}{n_i} - \frac{V_{bs}}{2} \right) = \frac{\epsilon_0\epsilon_{SiO_2}^2 \left(V_{peak} + 0.55 - \frac{V_{bs}}{2} \right)^2}{2\epsilon_{Si}qT_{ox}^2}. \quad (7)$$

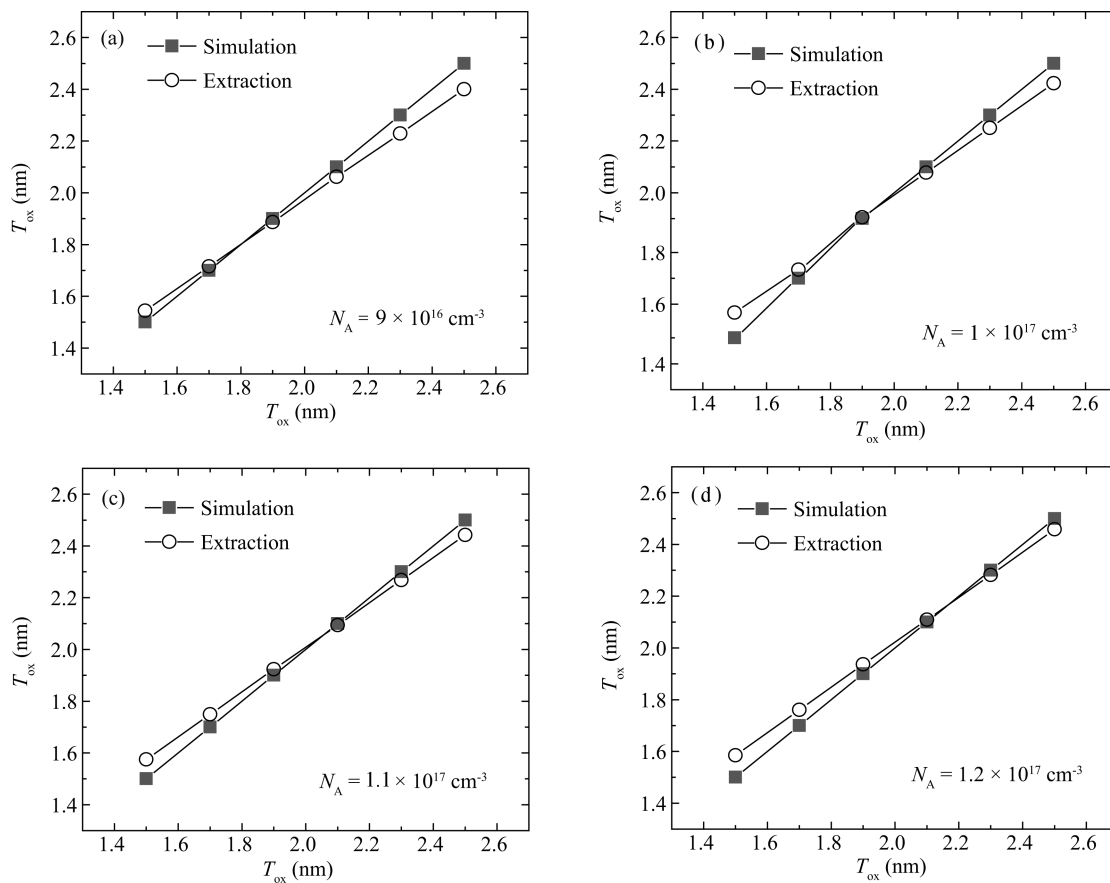


Fig. 4. T_{ox} extraction with different doping concentrations.

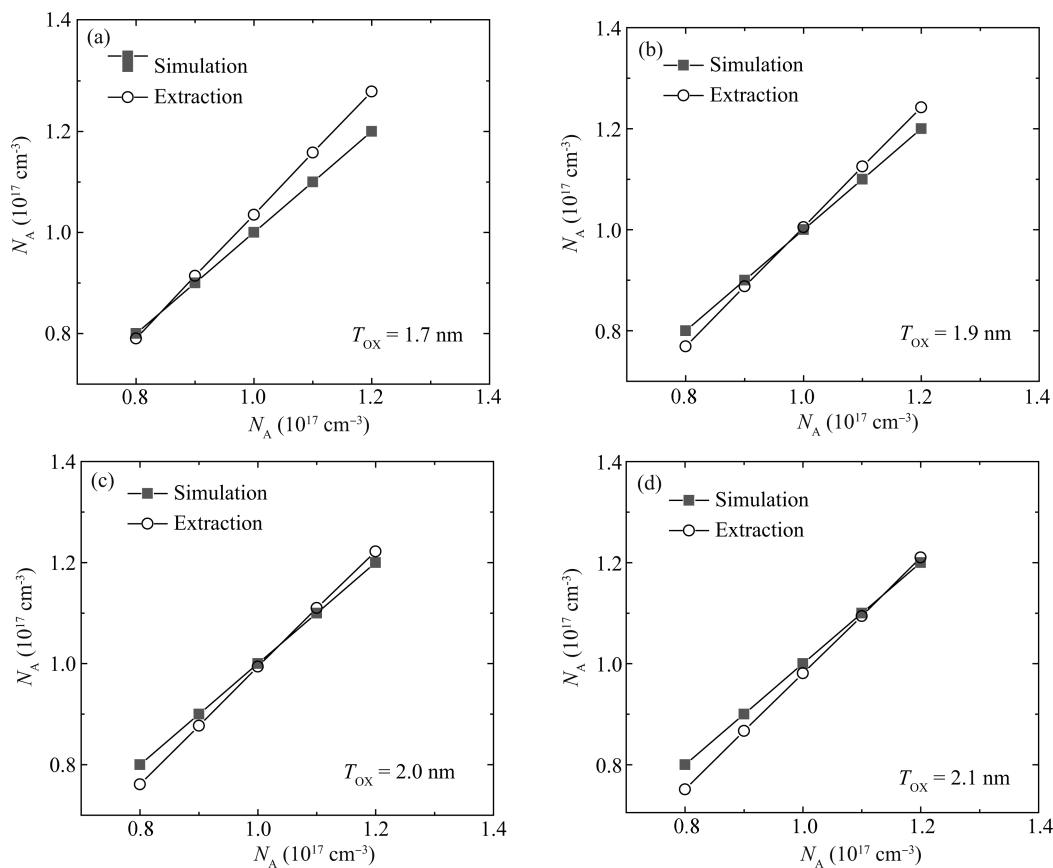


Fig. 5. N_A extraction with different dielectric oxide thicknesses.

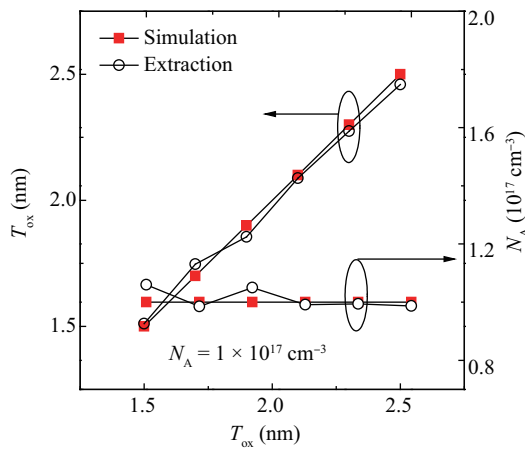


Fig. 6. N_A and T_{ox} extraction with different T_{ox} , when both variables are unknown.

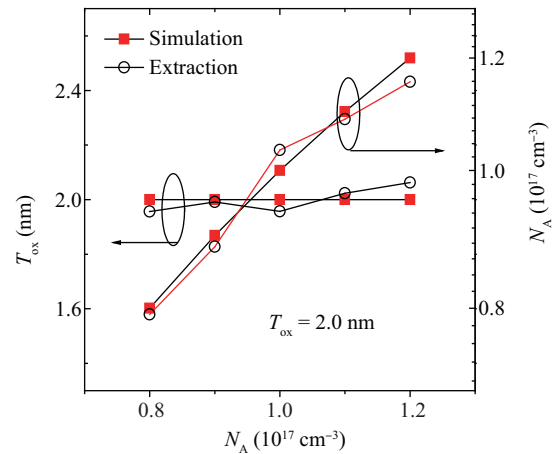


Fig. 7. N_A and T_{ox} extraction with different N_A , when both variables are unknown.

Therefore, a unique N_A is determined when T_{ox} is fixed. A binary-search method is applied to extract the body doping concentration.

When both the body doping concentration and the dielectric thickness are unknown, two different V_{peak} are obtained under different V_{bs} , as is shown in Eqs. (8) and (9).

$$V_{peak1} = -0.55 + \frac{V_{bs1}}{2} + \gamma_B \sqrt{\phi_F - V_{bs1}/2}, \quad (8)$$

$$V_{peak2} = -0.55 + \frac{V_{bs2}}{2} + \gamma_B \sqrt{\phi_F - V_{bs2}/2}. \quad (9)$$

Thus

$$N_A = n_i \exp \left[\frac{q}{kT} \frac{A^2 V_{bs2} - V_{bs1}}{2(A^2 - 1)} \right], \quad (10)$$

where $A = (V_{peak1} + 0.55 - V_{bs1}/2) / (V_{peak2} + 0.55 - V_{bs2}/2)$. As long as N_A is obtained, T_{ox} is obtained via Eq. (6).

3. Results and discussion

The results obtained by Eq. (6) and ISE simulation are compared in Fig. 4. T_{ox} is extracted with body doping concentrations varying from 8×10^{16} to $1.2 \times 10^{17} \text{ cm}^{-3}$, which are all around $1 \times 10^{17} \text{ cm}^{-3}$. In Fig. 4, the hollow-circle indicates the T_{ox} extracted from the simulation data using Eq. (6) with given body doping concentration and the square means the T_{ox} applied to the simulation. The results show that T_{ox} calculated using forward gated-diode exhibits good agreement with the simulation under different concentrations and the deviation is no more than 5%.

Figure 5 shows the N_A extraction results via Eq. (7) by giving different dielectric oxide thicknesses. It is obvious that N_A extracted by using the forward gated-diode method matches very well with the variable value applied to the simulation.

When both variables are unknown, these two variables are still extracted via Eq. (10) and the results are shown in Figs. 6 and 7.

4. Conclusion

The forward gated-diode method is used in this paper to extract the dielectric thickness (T_{ox}) and doping concentration (N_A) of MOSFETs. Based on device physics, both parameters are expressed as the function of the peak forward gated-diode R–G current. The results show good agreement with the ISE simulation no matter whether the T_{ox} and N_A are given previously, which demonstrates the validity of the proposed method.

References

- [1] Lysenko V S, Tyagulski I P, Gomeniuk Y V, et al. Effect of oxide–semiconductor interface traps on low-temperature operation of MOSFETs. *Microelectron Reliab*, 2000, 40: 735
- [2] Wang T, Chou P C, Chung S S. Effects of hot carrier induced interface state generation in submicron LDD MOSFET's. *IEEE Trans Electron Devices*, 1994, 41: 1618
- [3] Renn S H, Raynaud C, Pelloie J L, et al. A thorough investigation of the degradation induced by hot-carrier injection in deep submicron N- and P-channel partially and fully depleted unibond and SIMOX MOSFETs. *IEEE Trans Electron Devices*, 1998, 45: 2146
- [4] Sinha S P, Zaleski A, Loannou D E, et al. Hot hole induced interface state generation and annihilation in SOI MOSFETs. *IEEE Electron Device Lett*, 1996, 17: 121
- [5] Groeseneken G, Maes H E, Beltran N, et al. A reliable approach to charge-pumping measurements in MOS transistors. *IEEE Trans Electron Devices*, 1984, 31: 42
- [6] Bauza D. A general and reliable model for charge pumping—part I: model and basic charge-pumping mechanisms. *IEEE Trans Electron Devices*, 2009, 56: 70
- [7] Bauza D. A general and reliable model for charge pumping—part II: application to the study of traps in SiO₂ or in high- κ gate stacks. *IEEE Trans Electron Devices*, 2009, 56: 78
- [8] Katto H. Device parameter extraction in the linear region of MOSFET's. *IEEE Electron Device Lett*, 1997, 18: 408
- [9] He J, Xi X, Chan M, et al. Normalized mutual integral difference method to extract threshold voltage of MOSFETs. *IEEE Electron Device Lett*, 2002, 23: 428
- [10] Yan Z X, Dean M J. Physically-based method for measuring the threshold voltage of MOSFETs. *Proc Inst Electron*

- Eng—Circuits, Devices and Systems, 1991, 138: 351
- [11] Ortiz-Conde A, Gouveia Fernandes E D, Liou J J, et al. A new approach to extract the threshold voltage of MOSFETs. *IEEE Trans Electron Devices*, 1997, 44: 1523
- [12] Garcia Sanchez F J, Ortiz-Conde A, Mercato G D, et al. New simple procedure to determine the threshold voltage of MOSFETs. *Solid State Electron*, 2000, 44: 673
- [13] Ortiz-Conde A, Garcia Sanchez F J, Liou J J, et al. A review of recent MOSFET threshold voltage extraction methods. *Microelectron Reliab*, 2002, 42: 583
- [14] He J, Zhang X, Huang R, et al. Application of forward gated-diode RG current method in extracting FN stress-induced interface traps in SOI NMOSFETs. *Microelectron Reliab*, 2002, 42: 145
- [15] He J, Zhang X, Huang R, et al. A refined forward gated-diode method for separating front channel hot-carrier-stress induced front and back gate interface and oxide traps in SOI NMOSFETs. *Semicond Sci Technol*, 2002, 17: 487