A novel structure in reducing the on-resistance of a VDMOS

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Abstract: A novel structure of a VDMOS in reducing on-resistance is proposed. With this structure, the specific on-resistance value of the VDMOS is reduced by 22% of that of the traditional VDMOS structure as the breakdown voltage maintained the same value in theory, and there is only one additional mask in processing the new structure VDMOS, which is easily fabricated. With the TCAD tool, one 200 V N-channel VDMOS with the new structure is analyzed, and simulated results show that a specific on-resistance value will reduce by 23%, and the value by 33% will be realized when the device is fabricated in three epitaxies and four buried layers. The novel structure can be widely used in the strip-gate VDMOS area.

Key words: VDMOS; on-resistance; specific on-resistance; breakdown voltage; epitaxial layer resistance
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1. Introduction

In recent years, requirements for DC/DC converters, DC/AC converters, relays and relay drivers have been getting more and more stringent, thus a lot of companies and organizations pay more and more attention to research and exploration in the area, such as IR, CSMT, ST, Motorola and Vishay. As interrelated technician known, the characteristic frequency, thermal stability and input impedance of the power MOSFET are somewhat better than those of bipolar power transistors[1], and the VDMOS is also a kind of device, of which the channel conductance is controlled by gate voltage, its driving current is lower, the driving circle is much simple than that of the bipolar power transistor[1], hence the high-performance VDMOS is one of the key devices in these systems.

In particular, high output power of the VDMOS is the development trend of miniaturization and lightweight of global-system, and the relatively large on-resistance (R_{ON}) of power MOSFETs has been a considerable problem to designers[1,2]. From the original field-effect transistor introduced in the 1970s, the VVMOS, VUMOS and trench-MOSFET were proposed to reduce the R_{ON}, these device structures did some efforts on R_{ON}, but they are difficult to fabricate.

In this paper, a novel structure in reducing R_{ON} of the VDMOS is designed, and its tech-scheme is to reduce epitaxial layer resistance (R_{EPI}) by adding the buried layer (NBL), which is shown in Fig. 1. With the structure, the specific R_{ON} value of the VDMOS reduces by 22% that of the traditional VDMOS structure as the breakdown voltage maintains the same value in theory. On second thoughts, the specific R_{ON} value will reduce by 33% if the device is processed in three epitaxies and four NBLs; the novel structure can be widely used for a strip-gate VDMOS.

2. Structure and analysis

From the introduction and Fig. 1, we can see that the difficulty is to find out the tradeoff between size/doping of NBL and the breakdown voltage (BV_{DSS}) of the VDMOS.

2.1. Device design

The novel structure of the VDMOS is shown in Fig. 1, and the differences between the proposed structure and the traditional VDMOS structure is the added NBL which is fabricated before epitaxy, and the NBL is below the JFET area.

The designed process for the novel structure of the N-channel 200V-VDMOS is as follows:

Initial oxide → NBL photo/etch → thin oxide → arsenic implant → strip oxide all → epitaxy → field oxide → PBODY photo/etch → thin oxide → boron implant → guard ring photo/etch → boron implant → PBODY anneal →

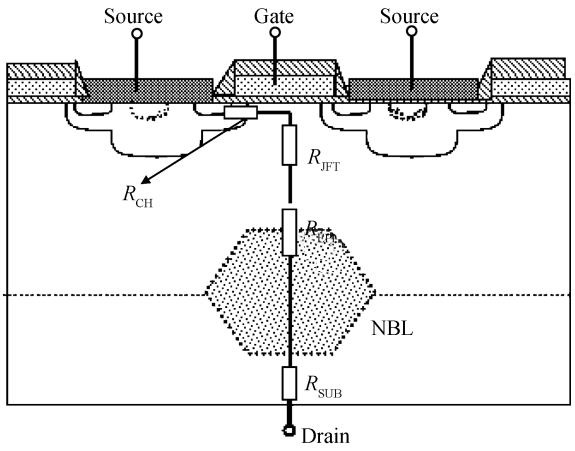

Fig. 1. Cross section of the novel VDMOS structure.

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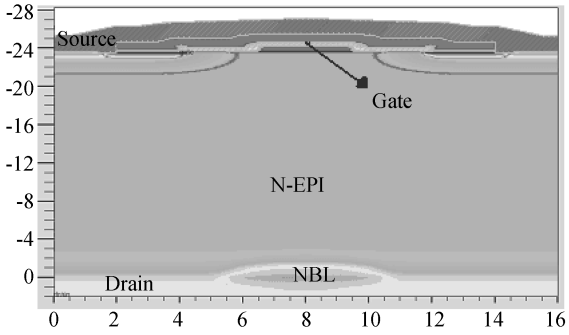

Fig. 2. Simulated cross section of the proposed structure (cell size is $16 \times 16\ \mu m^2$, and breakdown voltage is 248 V).

LPCVD SiO_2 → anneal → ACTIVE photo/etch →gate oxide → LPCVD poly-silicon → poly-silicon doping → source photo/etch → phosphorus implant → photo/etch → boron implant → LPCVD SiO_2 → anneal → contact photo/etch → metallization → passivation → test.

As the structure and process mentioned, the simulated cross section of the proposed structure is shown in Fig. 2.

2.2. On-resistance analysis

The R_{ON} of the VDMOS is made up of several components, as shown in Fig. 1, and there are only four main resistances signed in the cross section. The contact resistance between the source and drain metallization and the silicon, metallization and lead-frame are ignored, because these are normally negligible in high voltage devices[2, 3], such as 200 V. The R_{ON} of the VDMOS is given by

$$R_{ON} = R_{CS} + R_{CH} + R_{JFT} + R_{EPI} + R_{SUB} + R_{CD}, \quad (1)$$

where R_{CS} is the contact resistance between the source metallization and the silicon and source diffusion resistance, R_{CH} is the channel resistance, R_{JFT} is the component-resistance of the region between the two body regions, R_{SUB} is the substrate resistance and R_{CD} is the contact resistance between the drain metallization and the silicon.

In a general way, the epitaxial layer (EPI) is treated as a rectangle in the high-voltage VDMOS[1, 8], so calculating the R_{EPI} value is comparatively simple. As known to all, the depth of the NBODY junction (r_1) is about 2.5 μm, and the depth of the N^+ carrier diffusing in EPI (W_1) is about 2.0 μm. On the assumption that the thickness of the EPI needs 24 μm to fulfill BV_{DSS} = 200 V, and the wasting thickness of the EPI (W_4) in process is about 2.0 μm; the specific R_{EPI} value will be calculated. The traditional structure specific R_{EPI} is given by

$$R_{EPI} = \rho \frac{W_2}{S} = q\mu_n N_D \frac{W_2}{S}, \quad (2)$$

where $W_2 = W_3 - W_1 - W_4 - r_1 = 17.5\ \mu$m, $\rho = 4.35\ \Omega$·cm at 200 V device. From Eq. (2), the specific R_{EPI} is about 761250 $\Omega/\mu m^2$.

As shown in Fig. 3, if there is an NBL in the structure, $W_2 = r_2 = r_3$, specific R_{EPI} is about 609000 $\Omega/\mu m^2$, and the specific R_{EPI} is reduced by 25%.

The relationship between R_{EPI} and BV_{DSS} is shown in Fig. 4, where R_{EPI} is the best important composing in the high-voltage VDMOS, and more than 50% in 200 V in the N-channel VDMOS[2].

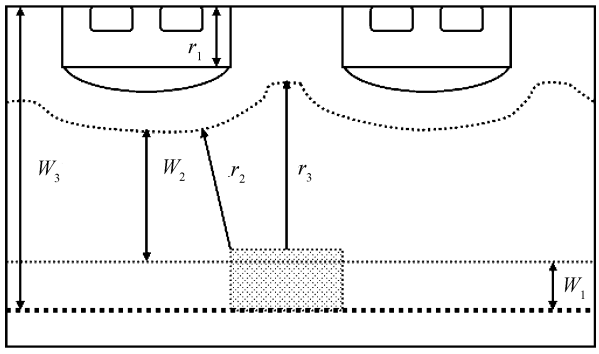

Fig. 3. Sketch map of key size for breakdown voltage and on-resistance.

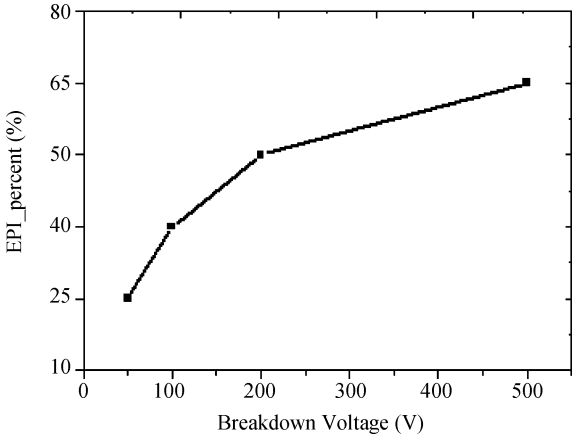

Fig. 4. Relationship between R_{EPI} and BV_{DSS} of the VDMOS[2].

3. Optimization design

Using process steps described above, the novel structure is implemented, and the specific R_{ON} is simulated. The simulated curve between specific R_{ON} and V_{DS} is shown in Fig. 5. The specific R_{ON} value of the traditional structure is 865370 $\Omega/\mu m^2$, and the value of the novel structure with one NBL is 712 743 $\Omega/\mu m^2$; the specific R_{ON} value reduced by 22% of the traditional structure as the BV_{DSS} maintained the same value, where the NBL_SIZE is 4 μm and the NBL implanted dose is 1×10^{16} cm^{-2} .

Because of the same breakdown voltage, it is important to analyze the distribution of the carrier. Figure 6 is the distribution curve of phosphorus from the Si/SiO_2 interface to the NBL, and the route is between the two body regions. From Fig. 6, the effective thickness of epitaxial layer is 20 μm, thicker than the distance from PBODY to N^+ substrate. That is $r_3 \geqslant W_2$; if $r_3 < W_2$, the BV_{DSS} of the VDMOS will fall.

So there is some space to optimize the specific R_{ON} farther. Figure 7 is the optimized cross section, and three epitaxies and four NBLs are in the structure. Figure 8 is the distribution curve of phosphorus from Si/SiO_2 interface to the NBL for the optimized structure, and the effective thickness of epitaxial layer is 14 μm, approximately the distance from PBODY to the N^+

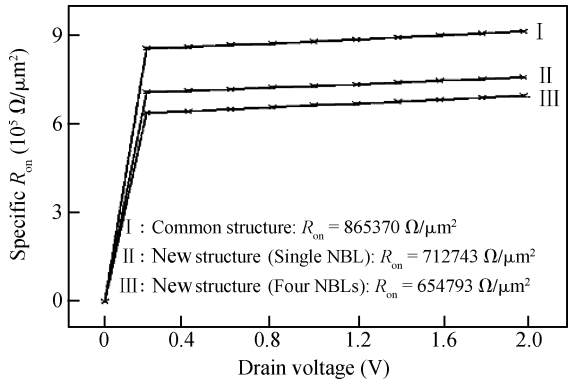

Fig. 5. Simulated specific R_{EPI} curve of the proposed structure at V_{DS} = 2 V and V_{GS} = 15 V.

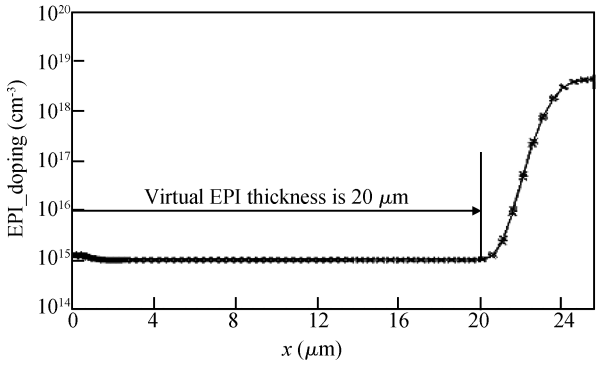

Fig. 6. Distribution curve of phosphorus from the Si/SiO_2 interface to the NBL (one NBL in the structure).

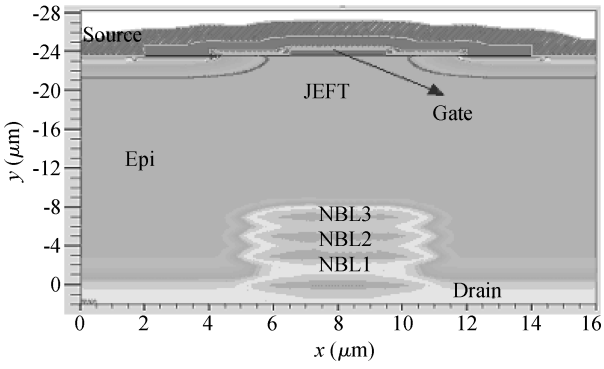

Fig. 7. Simulated cross section of the optimized structure.

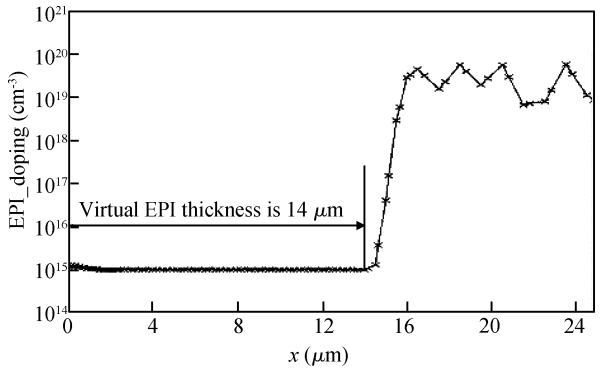

Fig. 8. Distribution curve of phosphorus from the Si/SiO_2 interface to the NBL (four NBLs in the structure).

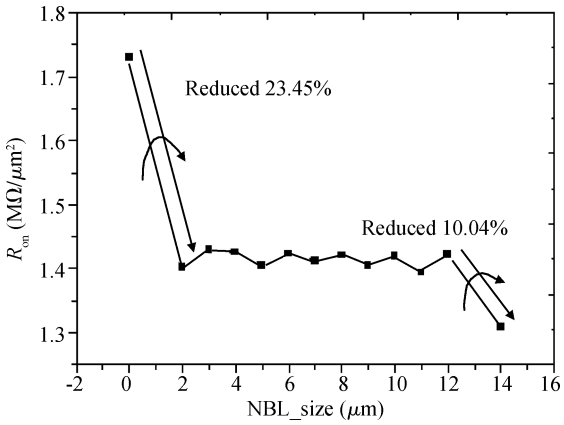

Fig. 9. Simulated specific R_{EPI} curve of the novel structure VDMOS with the NBL size varying from 2 to 14 μm in a 1 μm step.

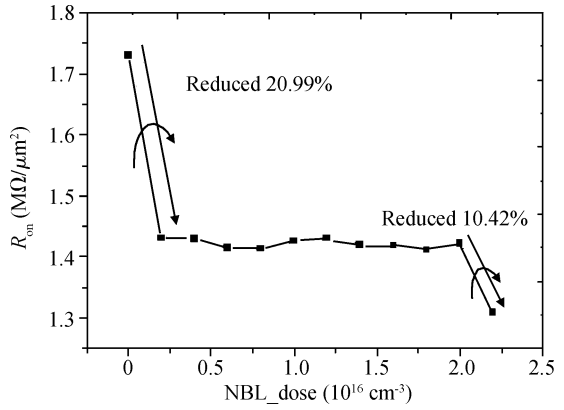

Fig. 10. Simulated specific R_{EPI} curve of the novel structure VDMOS with the NBL dose varying from 2×10^{15} to 2×10^{16} cm^{-2} in a 2×10^{15} cm^{-2} step.

substrate. In particular, with the optimized structure, the specific R_{ON} value reduced by 10% than the structure has single NBL, and the BV_{DSS} changed from 248 to 242 V, reduced by 2.5%.

In order to find out the tradeoff between the size/doping of the NBL and BV_{DSS} of the VDMOS, with TCAD tools, the relationship between the size of the NBL and BV_{DSS}/R_{ON} is simulated, which is shown in Fig. 9. From the curve, we know that the specific R_{ON} will decrease by 23.45% if there is one NBL in the structure, and the value will decrease by 33.49% if there are four NBLs in the structure. And the more important information we can get is that the specific R_{ON} and BV_{DSS} will almost maintain the same value as the size of the NBL changes from 2 to 12 μm in a 1 μm step. If the NBL is treated as a rectangle, the NBL resistor can simply be calculated from the resistor equation, and the NBL implant dose is 1×10^{16} cm^{-2}, the NBL resistor value is 0.0025 mΩ when there are four NBLs and the size of the NBL is 2 μm. The value is 0.0004 mΩ when the size of NBL is 12 μm. Finally, the specific R_{ON} will maintain the same value as the size of the NBL changes from 2 to 12 μm.

Figure 10 shows the simulated relationship curve between the implant dose of the NBL and BV_{DSS}/R_{ON} . From the curve, we know that the specific R_{ON} will decrease by 20.99% if there

is one NBL in structure, and the value will decrease by 31.41% if there are four NBLs in the structure. The more important information we can get is that the specific R_{ON} and BV_{DSS} will maintain the same value as the implant dose of the NBL changes from 2×10^{15} to 2×10^{16} cm^{-2} at 2×10^{15} cm^{-2} step.

4. Conclusion

A novel structure of VDMOS in reducing on-resistance is developed. The specific R_{ON} value will decrease by 22% of the traditional structure if there is an NBL in the VDMOS, and the value will decrease by 33% if three epitaxies and four buried layers are used in processing the new structure VDMOS. In particular, the proposed structure and its process are simulated and demonstrated to be appropriate for high-voltage strip-gate VDMOS.

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