A speaker driver for a single phase supply class G & I*

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Abstract: A speaker driver applied to class G/class I with a single phase power supply is presented. Gain expanding and compressing technology are employed in the signal processing circuit to optimize power dissipation. The circuit is implemented in 0.18 μm N-well CMOS. Experimental results show that the speaker driver has a good audio sound quality and power efficiency. Less than 0.006% THD at a low power range and less than 0.4% at a medium power range can be obtained with a 1 kHz sine wave signal. Maximum output power of 360 mW can be gained at a load of 8 Ω. The power efficiency is about twice that of a traditional class AB driver at the power range of 80 mW and shows more than 18% improvement at the higher output power range.

Key words: class G/class I; speaker driver; single phase power supply; THD
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1. Introduction

Generally, the amplitude of audio signals has a probability density function of Gaussian and large peak to average power ratio (PAR). Roughly, the PAR of audio signals is between 10 and 20 dB, with an average of 15 dB, which is 12 dB below the power of a rail-to-rail sine wave[1]. Class AB audio amplifiers have the benefit of high audio quality and less switching noise, but their average efficiency is about 10%–20% due to the high PAR of actual audio signals. Class D audio amplifiers provide the benefit of power efficiency at the cost of slightly reduced performance and a level of switching noise, which might, in some cases, interfere with RF functions, such as mobile phone, GPS or FM radio reception[2].

The class G and I audio amplifiers[3−6] are introduced to bring together the benefit of class AB and class D. These new kinds of high efficiency linear amplifiers, whose supply rails are adaptively changed according to the magnitude of the input audio signal, were developed to reduce the power dissipation while keeping the advantages of class AB amplifiers, such as good linearity and free of EMI. Class G audio amplifiers use multiple discrete supply voltages. At lower power levels, the lower supply voltage is used. When the signal becomes too large for this supply, the higher power supply takes over and delivers the output power. In this way, the average voltage drop across the output transistors is reduced and the overall efficiency can be improved[1]. Class I audio amplifiers change the supply voltage continuously according to the input signal level. When the amplitude of the input signal is small, class I amplifiers operate at a low and constant supply voltage. When the amplitude becomes large, the supply voltage tracks the absolute value of the input signal with certain headroom.

Class G[3,4] and class I[5,6] use bipolar power supply rails to realize high efficiency amplification. An inverter is always introduced to generate a negative supply and a high cost triple well process is needed. It will add the complexity of circuit and the cost of the whole chip. A low cost speaker driver suitable for single phase supply class G & I is proposed in this paper. This operates with only positive supply and a signal processing block is introduced to reduce the power loss when amplifying the output signal waveforms on the ground side. The theoretical efficiency of class G, class I and class AB is derived. The design of the nonlinear signal processing circuit is shown, and three stage class AB power amplifier applied in the proposed speaker driver is introduced.

2. Efficiency analysis of a single phase supply class G, I and class AB

The maximum supply voltage is 3.3 V in our design. The design headroom value is 0.2 V between the maximum amplitude of output signal and supply or ground. The load is a 8 Ω loudspeaker.

The amplitude probability density function of audio signals is assumed of Gaussian type. The amplitude probability density function of audio signals can be expressed as follows,

$$p(v) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{v^2}{2\sigma^2}\right), \tag{1}$$

where σ is the RMS level of the audio signal. Generally, the audio signal has an average PAR of 15 dB, and the average output power can be calculated as follows,

$$P_{\text{out}} = \left(V_{\text{MAX}}/10^{15/20}\right)^2/8 = 33.28\ \text{mW}. \tag{2}$$

When inputting low level signals, the supply voltage of class G & I is at a constant value of 1.4 V. While the amplitude of input signal rises up the threshold value, the supply voltage of class G transits to 3.3 V. The gain of positive phase signal is

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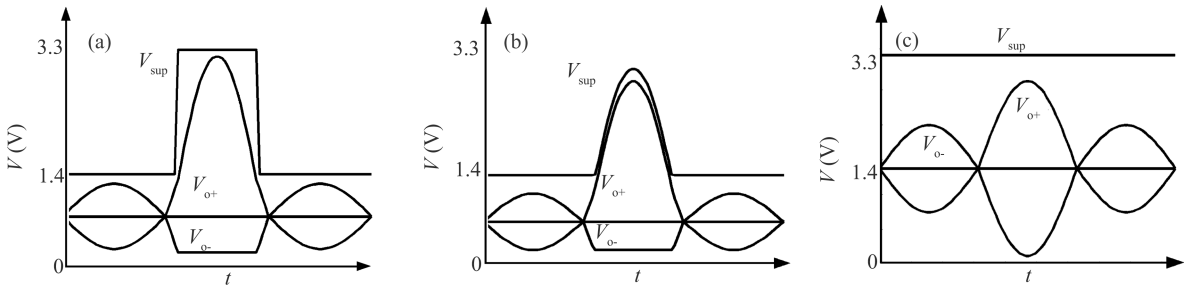

Fig. 1. Waveforms of the outputs and power supplies. (a) Class G. (b) Class I. (c) Class AB.

doubled and the negative phase signal is clamped at a constant level of 0.2 V, then the differential signal gain keeps the same as before. The supply voltage and two terminal output voltages of H-bridge of class G are shown in Fig. 1(a). The maximum output voltage swing is 1 V under the supply voltage of 1.4 V due to the headroom value of both the high side and the low side being 0.2 V. Then the average supply power and average efficiency of class G can be calculated as follows,

$$P_{\mathrm{G}} = 2 \times \int_0^1 1.4 \times \frac{v}{8} p(v)\mathrm{d}v + 2 \times \int_1^{2.9} 3.3 \times \frac{v}{8} p(v)\mathrm{d}v = 86.9\ \mathrm{mW} \tag{3}$$

$$\eta_{\mathrm{G}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{Vdd}}} = 38.3\%. \tag{4}$$

Different from class G amplifier, the supply voltage of class I tracks the amplitude of the output signal with a headroom of 0.2 V when the input signal rises up the threshold value. Then it has higher efficiency than that of class G theoretically. The supply voltage and two terminal output voltages of H-bridge of class I are shown in Fig. 1(b). Then the average supply power and average efficiency of class I can be calculated as follows,

$$P_{\mathrm{I}} = 2 \times \int_0^1 1.4 \times \frac{v}{8} p(v)\mathrm{d}v + 2 \times \int_1^{2.9} (v + 0.4) \frac{v}{8} p(v)\mathrm{d}v = 73.8\ \mathrm{mW}, \tag{5}$$

$$\eta_{\mathrm{I}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{Vdd}}} = 45.07\%. \tag{6}$$

The output waveforms of class AB amplifier with constant power supply are shown in Fig. 1(c). The average supply power and average efficiency of class AB are calculated as follows,

$$P_{\mathrm{AB}} = 2 \times \int_0^{2.9} 3.3 \times \frac{v}{8} p(v)\mathrm{d}v = 195.9\ \mathrm{mW}, \tag{7}$$

$$\eta_{\mathrm{AB}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{Vdd}}} = 16.99\%. \tag{8}$$

As mentioned above, the theoretical average efficiency of class G and I is more than twice that in class AB when amplifying the actual audio signal with PAR of 15 dB. The efficiency of these three kinds of audio amplifiers when inputting a sinusoidal signal can be derived in the same way. The calculated

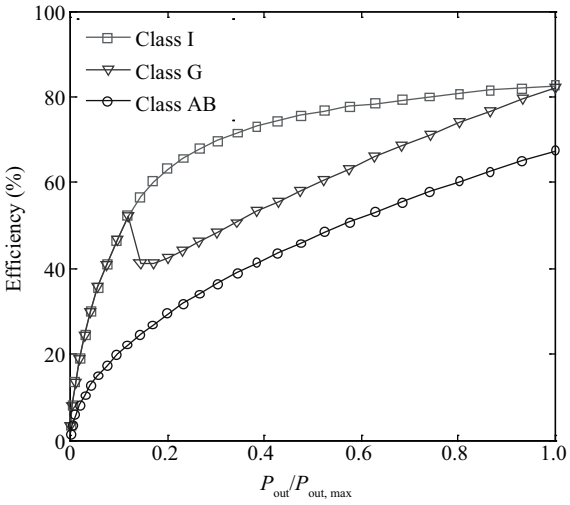

Fig. 2. Calculated efficiency of three kinds of amplifier versus output power.

efficiency curves of three kinds of amplifier versus normalized output power are shown in Fig. 2. The efficiency of class G and I is about twice that of class AB at the low power range and class I has the highest efficiency when the output power becomes larger. Nevertheless, the class G amplifier has 25% higher efficiency than that of class AB at a large output power range.

3. Nonlinear signal processing circuit design

Since the single phase class G or I audio amplifier has only positive supply rails, then the proposed speaker driver should operate properly under all of the supply voltage conditions. Also a signal processing circuit is needed to compress the negative amplitude to reduce the dissipation. This is realized by two times amplifying the positive phase signal and meanwhile suppressing the negative phase signal while only positive supply rails are made. The desired output waveforms of the speaker driver are shown in Fig. 3(a). When the input signal has a small amplitude, the input signal is amplified 1 time in the signal processing circuit just like through a normal pre-amplifier. When the amplitude of the input audio signal becomes larger, the positive phase exceeded threshold value will be amplified 2 times and the negative phase is kept at a constant level. The transfer function of the signal processing circuit is as shown in Fig. 3(b), which is similar to that in Ref. [7]. The negative side compressing circuit in Ref. [7] adopts the soft

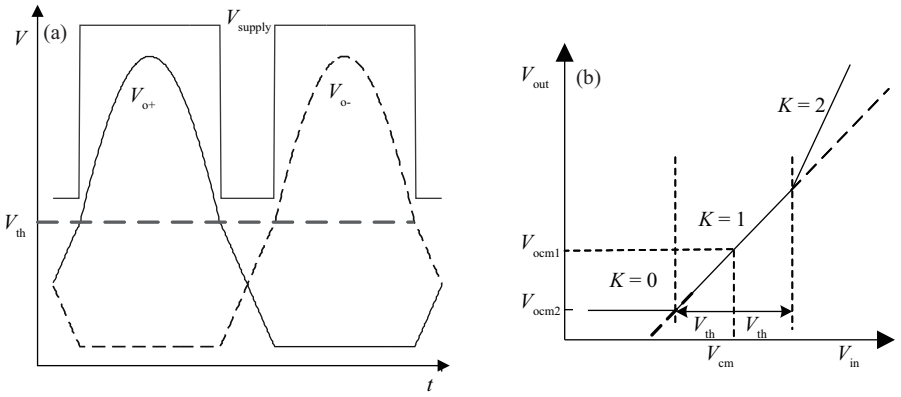

Fig. 3. (a) Waveforms of both bridge halves. (b) Input and output transfer characteristics.

limit, which is hard to keep the gain consistency when gain compressing happens. The gain variance will cause THD deterioration. The compressing in this paper adopts the hard limit, which can keep the gain consistency easily.

The whole diagram of the signal processing circuit is shown in the dashed block in Fig. 4. The audio signals $V_{\rm inp}$ and $V_{\rm inn}$ input into a fully differential operational amplifier through a high pass filter that has a crossover frequency of 15.9 Hz. $V_{\rm cm}$ is an on-chip, well-filter reference at half the supply voltage. It uses as the common mode voltage reference. The gain of the op amp is set at 6 dB by the ratios of the resistors. The outputs of the fully differential op amp $V_{\rm 1p}$ and $V_{\rm 1n}$divide through a series of resistors to get their partial voltage $V_{\rm 2p}$ and $V_{\rm 2n}$. From these resistor settings, the relation between the two pairs of voltages can be gained as follows,

$$V_{\rm 2n} - V_{\rm ocm} = (V_{\rm 1n} - V_{\rm ocm})/2, \tag{9}$$

$$V_{\rm 2p} - V_{\rm ocm} = \left(V_{\rm 1p} - V_{\rm ocm}\right)/2. \tag{10}$$

Two comparators with hysteresis are used to compare the absolute value of the $V_{\rm 1n}$ and $V_{\rm 1p}$ with a preset value to generate the switch signals of two three-input multiplexers. The hysteretic value is set at about 20 mV to prevent the oscillation at the transition point. The output voltage of the two multiplexers $V_{\rm 3n}$ and $V_{\rm 3p}$ can be expressed as follows,

$$V_{\rm 3n} = \begin{cases} V_{\rm ocm}, & V_{\rm 1n} \leqslant V_{\rm cm} - 0.25, \\ V_{\rm 2n}, & V_{\rm cm} - 0.25 < V_{\rm 1n} < V_{\rm cm} + 0.25, \\ V_{\rm 1n}, & V_{\rm 1n} \geqslant V_{\rm cm} + 0.25, \end{cases} \tag{11}$$

$$V_{\rm 3p} = \begin{cases} V_{\rm 1p}, & V_{\rm 1n} \leqslant V_{\rm cm} - 0.25, \\ V_{\rm 2p}, & V_{\rm cm} - 0.25 < V_{\rm 1n} < V_{\rm cm} + 0.25, \\ V_{\rm ocm}, & V_{\rm 1n} \geqslant V_{\rm cm} + 0.25. \end{cases} \tag{12}$$

Then the differential signal between $V_{\rm 3p}$ and $V_{\rm 3n}$ can be expressed as follows,

$$V_{\rm 3p}{-}V_{\rm 3n} = \begin{cases} V_{\rm 1p} - V_{\rm ocm}, & V_{\rm 1n} \leqslant V_{\rm cm} - 0.25, \\ V_{\rm 2p} - V_{\rm 2n}, & V_{\rm cm} - 0.25 < V_{\rm 1n} < V_{\rm cm} + 0.25, \\ V_{\rm ocm} - V_{\rm 1n}, & V_{\rm 1n} \geqslant V_{\rm cm} + 0.25. \end{cases} \tag{13}$$

Combining Eqs. (9), (10) and (13), then

$$V_{\rm 3p} - V_{\rm 3n} = V_{\rm 1p} - V_{\rm ocm} = 2\left(V_{\rm inp} - V_{\rm cm}\right), \tag{14}$$

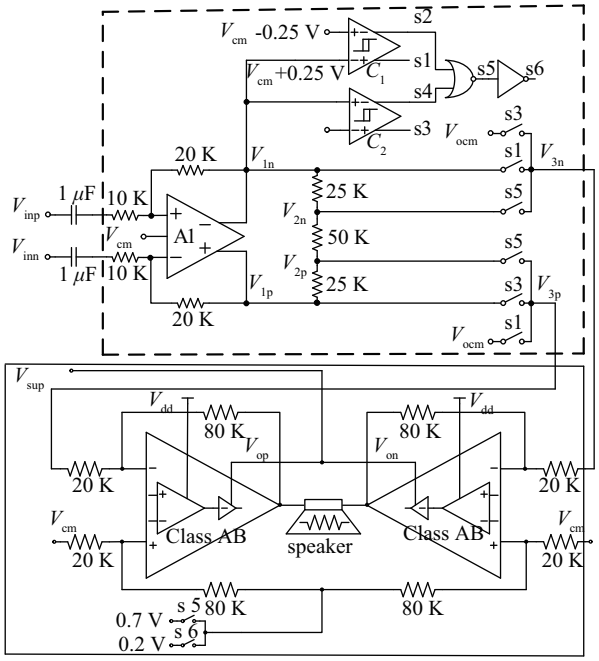

Fig. 4. Circuit diagram of the signal processing circuit.

where $V_{\rm ocm}$ is the output common mode voltage. The differential signal of $V_{\rm 3p}$ and $V_{\rm 3n}$ is proportional to the amplitude of the input signal, which means that it is a linear amplification from the differential output viewpoint. The simulation waveforms of $V_{\rm 3p}$, $V_{\rm 3n}$ and $V_{\rm 3p} - V_{\rm 3n}$ are shown in Fig. 6(a).

The schematic of the fully differential op amp A1 and the hysteretic comparator are shown in Figs. 5(a) and 5(b), respectively. As the input block of the whole system, the fully differential op amp should have high gain and low noise. The pMOS input pair is preferred for lower $1/f$ noise. The noise in the full-differential op amp can be expressed as follows,

$$\overline{dv_{\rm ieq}^2} = 2\left[\overline{dv_7^2} + \overline{dv_9^2}\left(\frac{g_{\rm m9}}{g_{\rm m7}}\right)^2\right], \tag{15}$$

where

$$\overline{dv_7^2} = \frac{4\gamma KT}{g_{\rm m7}} + \frac{KF_{\rm F}}{(WL)_7 C_{\rm ox}^2}\frac{1}{f}, \tag{16}$$

$$\overline{dv_9^2} = \frac{4\gamma KT}{g_{\rm m9}} + \frac{KF_{\rm F}}{(WL)_9 C_{\rm ox}^2}\frac{1}{f}. \tag{17}$$

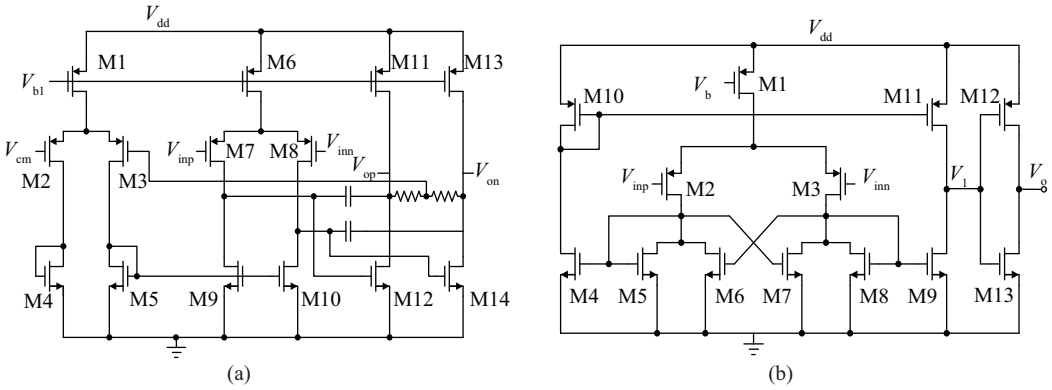

Fig. 5. (a) Schematic of full-differential op amp. (b) Schematic of hysteretic comparator.

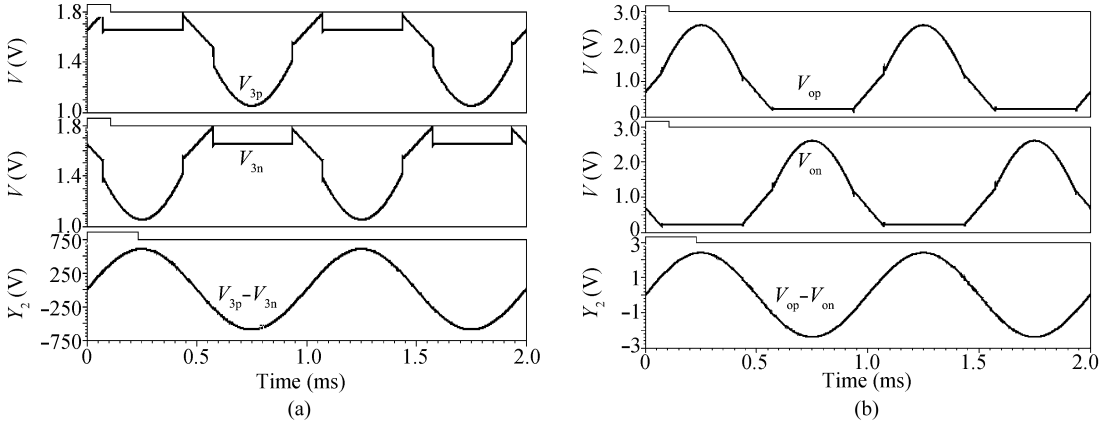

Fig. 6. Simulation waveforms. (a) V_{3p}, V_{3n} and $V_{3p} - V_{3n}$. (b) V_{op}, V_{on} and $V_{op} - V_{on}$.

The guideline to reduce the input thermal noise is to increase g_{m7} and g_{m9}/g_{m7}, and the way to reduce $1/f$ noise is to increase the area of input devices and g_{m9}/g_{m7}. Then the over-drive voltage of M7 and M8 should keep small when that of M9 and M10 should be larger. The channel length of all input and load devices should be large to reduce the $1/f$ noise, which also causes higher gain.

The hysteretic comparator is used to prevent the state oscillation at transition. There are two paths of feedback. The first is current-series negative feedback through the common source node of transistors M2 and M3. The second path is the voltage-shunt positive feedback through the gate-drain connection of transistors M6 and M7. When the ratio β_6/β_5 is greater than one, hysteresis will result. The hysteretic value is about 20 mV and the trip point is expressed as follows,

$$V_{TRP}^{+} = V_{TRP}^{-} = v_{GST3} - v_{GST2}. \tag{18}$$

4. Class AB power amplifier design

The simplified diagram of the class AB power amplifier and the feedback connection are shown in the solid block in Fig. 4. The output common mode voltage of class AB is controlled by a two-input multiplexer. It can be set at 0.2 V or 0.7 V, determined by the control signals s5 and s6. When the amplitude of the input signal is at a low level, then V_{sup} is set at 1.4 V and there is neither gain expanding nor gain compressing. The output common mode voltage is set at 0.7 V. While the amplitude of the input signal is over the threshold value, the output positive phase signal is amplified twice and the output negative phase signal is kept at a certain level of 0.2 V, which is the preset headroom to ground to guarantee a good total harmonic distortion. Under this condition, the output common mode voltage of class AB amplifier is set at 0.2 V to keep the continuity of the output waveforms. The simulated output waveforms of V_{op}, V_{on} and $V_{op} - V_{on}$ are shown in Fig. 6(b).

The proposed class AB power amplifier was incorporated in a three-stage op amp, as shown in Fig. 7. The op amp consists of a differential input stage, a non-inverting intermediate gain stage and the class AB output stage. A compensation capacitor C_c is used to stabilize the amplifier.

The PMOS-input folded-cascode architecture is applied to the first stage. The intermediate stage realizes non-inverting amplification with the active loads of MPb1/MPb2 and MNb1/MNb2. The active loads are used to control the quiescent current of the power output stage, which consists of power transistors MP and MN[8]. Under quiescent conditions, MPb1 and MNb1 operate in the saturated or sub-threshold region, and so do MP and MN. These active loads, together with output power transistors, can be viewed as two current mirrors. For instance, MPb1 and MP make up a current mirror with a proper current gain, and then the quiescent current of the power stage can be controlled through the quiescent current of MPb1, which can be preset easily. In the class B amplification mode, when the input voltage increases, the resistance con-

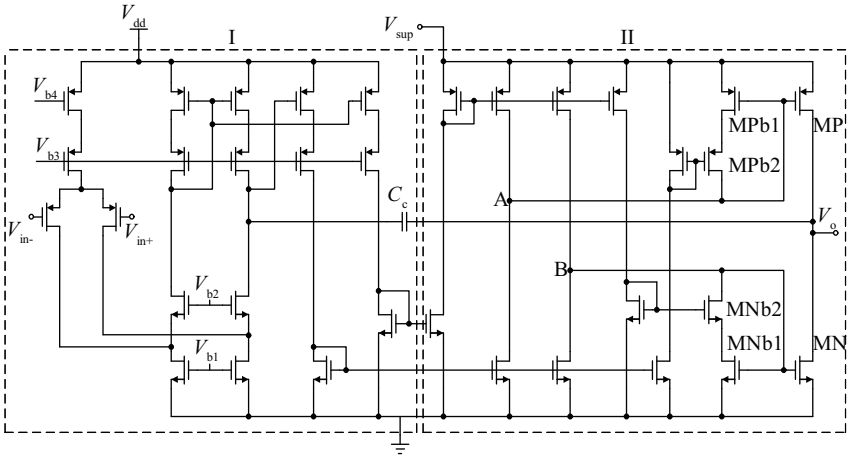

Fig. 7. Schematics of the proposed class AB op amp.

Table 1. AC characteristics summary of class AB amplifier.

Parameter		V_{sup} = 1.4 V			V_{sup} = 3.3 V		Power dissipation (mW)
		V_{out} = 0.7 V	V_{out} = 0.2 V	V_{out} = 1.2 V	V_{out} = 0.2 V	V_{out} = 3.1 V	
TT	PM (degree)	82.7	78.4	71.7	65.9	53.4	1.4 V × 6.23 mA+ 3.3 V × 265 μA
	GBW (MHz)	2.45	2.38	1.97	2.27	1.48	= 9.6 mW
	DC gain (dB)	79.3	98.5	84.9	95.3	82.7	
SS	PM (degree)	86.8	81.1	78.9	67.1	52.4	1.4 V × 6.11 mA + 3 V × 265 μA
	GBW (MHz)	1.85	1.6	1.16	1.66	1.08	= 9.5 mW
	DC gain (dB)	84.6	89.4	80.6	97.9	86	
FF	PM (degree)	75	73.6	68.5	65.8	55.8	1.4 V × 6.46 mA + 3.6 V × 265 μA
	GBW (MHz)	3.65	3.59	3.16	3.54	2.44	= 10 mW
	DC gain (dB)	70.6	94.7	77.6	90.8	73.3	

nected to node A increases, allowing the voltage swing at node A to be large enough to provide the maximum drive for the output PMOS transistor MP. Similarly, when the input voltage decreases, the resistance at node B increases, which enhances the voltage swing at node B to provide maximum drive for the output NMOS transistor MN. Nested miller compensation (NMC) is used to stabilize the proposed op amp. C_c is the compensation capacitor between the first stage and the third stage. The compensation capacitor between the second stage and the third stage is realized by the large gate-source capacitance of the output power transistors. The aspect ratios of the P-channel and the N-channel power transistor are 18500 μm/0.3 μm and 6000 μm/0.35 μm, respectively.

Since the proposed class AB amplifier operates under adaptive power supply, the circuit should operate at different power supply domains. The power supply of the circuit at block I is V_{dd} of 3.3 V. The circuit at block II operates at the power supply of V_{sup}, which is provided by the adaptive switching converter. It should be noted that the operation is not fully differential when inputting high level signals, as shown in Fig. 5(b). The AC characteristics at all extreme conditions should be carefully simulated to guarantee the stability of the class AB amplifier. The simulation results are summarized in Table 1.

5. Measured results

The proposed speaker driver is processed in SMIC 0.18 μm 3.3 V CMOS technology. The chip micrograph is depicted in Fig. 8. This mainly consists of a current bias circuit, a voltage buffer, a signal processing block, two class AB amplifiers, and four output PMOS and NMOS power transistors. The chip area is about 0.54 mm^2.

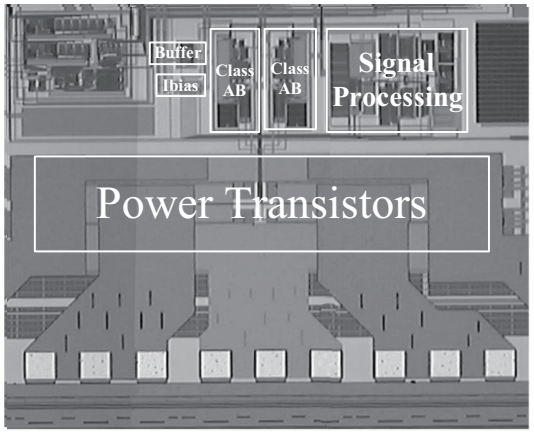

Fig. 8. Chip micrograph.

Figures 9(a) and 9(b) show the waveforms of the positive, negative and differential outputs of a class AB H-bridge at a low level sine wave with no gain variety and at a high level with gain variety, respectively. The differential outputs are both low distortion sinusoid signals.

Figure 10 shows the total harmonic distortion (THD) of the whole speaker driver versus the output power when the input is a 1 kHz sinusoid signal. It has been tested using an Au-

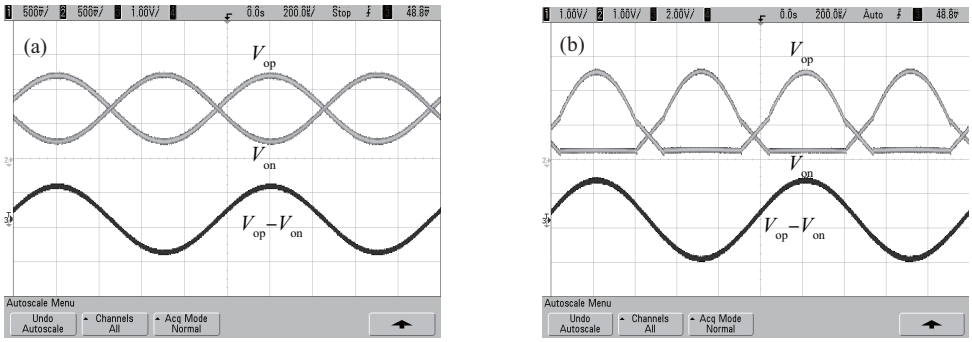

Fig. 9. Output waveforms. (a) No gain variety. (b) With gain variety.

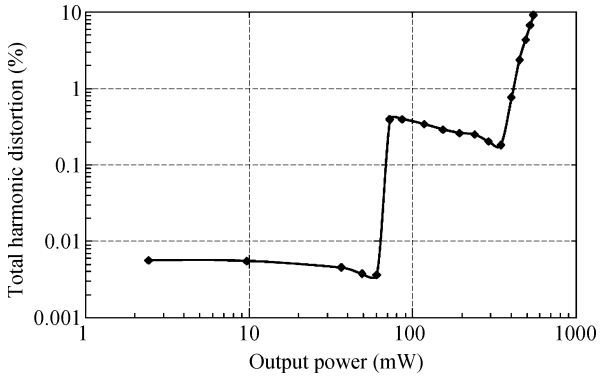

Fig. 10. THD plot versus output power.

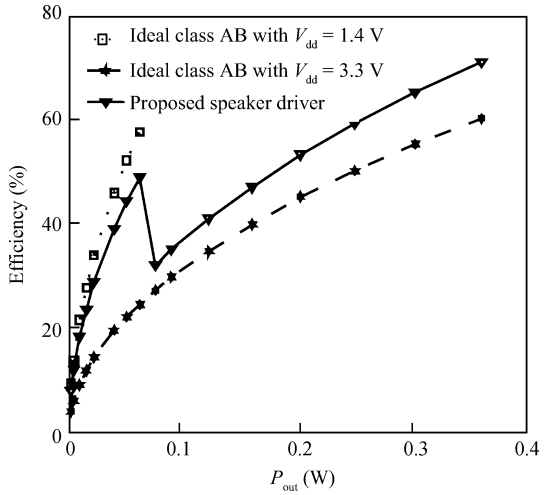

Fig. 11. Efficiency versus output power.

dio Precision Sys-2722. At the low power range, the speaker driver amplifies the audio signal likes a fully differential op amp. The THD parameter is less than 0.006% and it becomes better when the output power is larger. The THD characteristics get worse at the output amplitude corresponding to the switching point. Since nonlinear operation is applied to the input signal amplification and the switching spike is introduced to the output signal, the even harmonics cannot be suppressed. The THD performance is less than 0.4% at this power range. The other deterioration of THD is caused by the clipping due to the large output amplitude.

Figure 11 shows also the measured efficiency of the speaker driver with two level supply rails versus the output power. The efficiency of the ideal class AB can be derived via the method in Section 2. The efficiency of the proposed speaker driver has an obvious degradation at the supply switching point as that as THD. The efficiency plot displays the classical non-monotonic behavior of the proposed speaker driver: better than 30% efficiency is achieved from output power of 22.5 mW to the maximum output power of 360 mW. At the low power range, the efficiency of the proposed speaker driver is about twice that of the traditional class AB driver.

The main specifications of the proposed speaker driver are summarized in Table 2.

Table 2. Performance summary of proposed speaker driver.

Parameter	Value
Supply voltage	1.4, 3.3 V
Process	0.18 μm, 3.3 V N-well CMOS
Static power dissipation	9.6 mW
Maximum output power	360 mW @ 8 Ω
THD	0.006% @ 1 kHz, P_{OUT} = 10 mW
	0.4% @ 1 kHz, P_{OUT} = 80 mW
SNR	83.6 dB @ V_{out} = 1 Vrms
Chip area	0.54 mm^2

6. Conclusion

A speaker driver for class G/class I with a single phase supply has been presented. Nonlinear signal processing is introduced to optimize the power dissipation on the ground side. An obvious advantage of the proposed speaker driver is that it can be integrated on the same die with the base band processor using a low cost single well CMOS process. With a 1 kHz sine wave stimulus, the THD parameter is less than 0.006% at the output power range of 80 mW. Less than 0.4% THD can be obtained at medium output power range, although the input signal goes through the nonlinear processing. The experimental efficiency of the proposed speaker driver with adaptive rails shows a great improvement compared with the traditional Class AB driver.

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