A new shallow trench and planar gate MOSFET structure based on VDMOS technology*

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Abstract: This paper proposes a new shallow trench and planar gate MOSFET (TPMOS) structure based on VDMOS technology, in which the shallow trench is located at the center of the n^- drift region between the cells under a planar polysilicon gate. Compared with the conventional VDMOS, the proposed TPMOS device not only improves obviously the trade-off relation between on-resistance and breakdown voltage, and reduces the dependence of on-resistance and breakdown voltage on gate length, but also the manufacture process is compatible with that of the VDMOS without a shallow trench, thus the proposed TPMOS can offer more freedom in device design and fabrication.

Key words: power MOSFET; shallow trench; planar gate
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1. Introduction

In order to realize the low specific on-resistance (R_{on}) and high breakdown voltage (V_{BR}) of power MOSFET device, the super-junction MOSFET(SJMOS)[1] and oxide filled extended trench gate SJMOSFET[2] are the most promising structures, but SJMOS structures needs to control accurately the charge balance between the p-pillar and n-pillar regions, which are realized by multi-step epitaxy growth combined with ion implantation or multiple ion implantation[3], or trench-filling combined with trench etching[4, 5], or deep trench etching and epitaxial growth[6], resulting in a higher process cost. This paper proposes a new shallow trench planar gate MOSFET (TPMOS) structure based on conventional VDMOS technology, similar to the trench planar gate IGBT[7, 8]. The mechanism and characteristics are analyzed by ISE simulator. The results show that new TPMOS device can improve obviously R_{on} and V_{BR}, and reduce the dependence of R_{on} and V_{BR} on gate length compared with the conventional VDMOS device.

2. Device structure and fabrication process

Figure 1 indicates the TPMOS and VDMOS cell profile structures. Compared with the VDMOS as shown in Fig. 1(a), a shallow trench located at the center of the n-drift region between the cells is introduced, and filled with n-type polysilicon, as shown in Fig. 1(b). If removing the shallow trench, the TPMOS is the same as the VDMOS. The wider trench can form the channels at the trench sidewalls, and results in the variation of threshold voltage (V_T). The deeper trench can induce a premature breakdown of the trench bottom corners, and results in the fall of V_{BR}, and the increase in gate–drain capacitance (C_{GD}), simultaneously. In order to avoid the influence of the trench on the channel region and obtain better trade-off relations among blocking, conducting and switching characteristics, the depth of the trench region (d_t) must be less than the depth of the p-type region (d_p), i.e. $d_t < d_p$; the width of trench region (w_t) is narrower than the cell space (s_p), i.e. $w_t < s_p$.

TPMOS can be fabricated by the following process flow. First, the shallow trench is formed in the n- epitaxial layer by reactive ion etching (RIE). Next, the gate oxide layer is formed by dry oxidation, and the polysilicon gate is formed by chemical vapor deposition (CVD) to fill the trench, and then the planarization of polysilicon film is realized by chemical mechanism polishing (CMP) or trench-filling combined with trench etching. After that, the doping concentrations of the p-type region, the n^+ source region and the polysilicon gate can be realized by self-alignment technology using ion implantations. The rest, such as the electrode formation and the substrate attenuation, are similar to the process of the VDMOS. So the fabrication process of the TPMOS structure is compatible to that of the VDMOS, except for the front shallow trench.

3. Mechanism and characteristics analysis

3.1. On-resistance

In the conventional VDMOS, as shown in Fig. 1(a), on-resistance (R_{on}) mainly consists of the resistance of the channel region (R_{CH}), the resistance of the accumulation region (R_A),

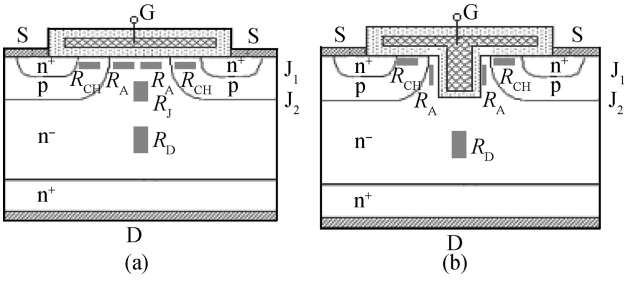

Fig. 1. Comparison of (a) VDMOS and (b) TPMOS cell structures.

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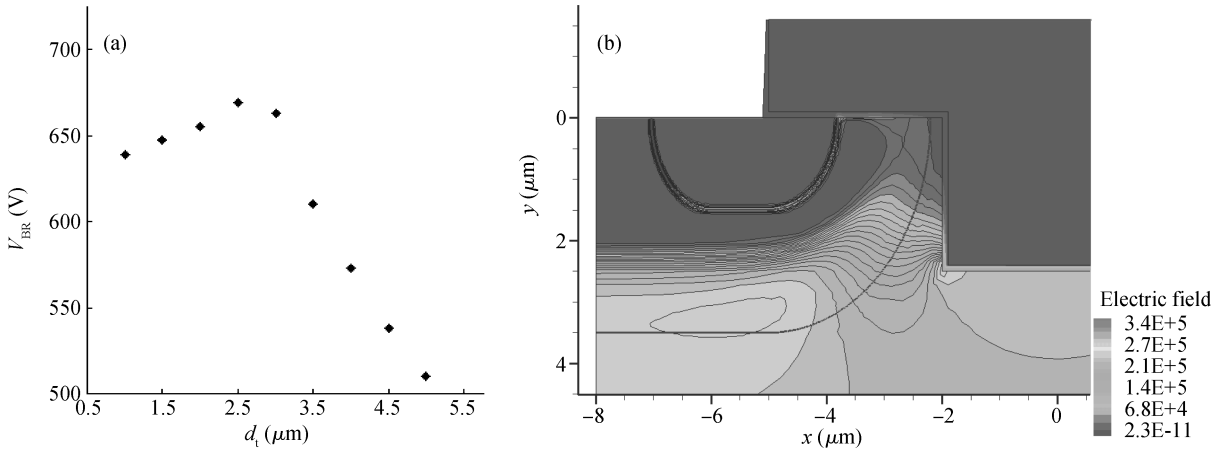

Fig. 2. (a) Influences of d_t on V_{BR} and (b) the electric field distribution of the TPMOS devie with $d_t = 2.5$ μm.

the resistance of the JFET region (R_J), and the resistance of the drift region (R_D), i.e. $R_{on} = R_D + R_J + R_A + R_{CH}$. In the TPMOS structure, as shown in Fig. 1(b), the JFET region is eliminated, and the electron accumulation can be formed along the trench sidewalls during conducting, so R_{on} of the TPMOS can be expressed as

$$R_{on} = R_D + R_A + R_{CH}, \tag{1}$$

where R_{CH} and R_D of the TPMOS are same respectively with the counterpoint of the VDMOS for the same structural parameters, but R_A of the TPMOS is smaller than the total of R_A and R_J of the VDMOS. So R_{on} of the TPMOS is smaller than that of the VDMOS.

3.2. Breakdown voltage

In the conventional VDMOS, the breakdown voltage (V_{BR}) is related to the concentrations and thicknesses of the n-drift and p-type regions at the two sides of J_2 junction, and the cell space (s_p). In the new TPMOS, the trench can affect the electric field at the J_2 junction curvature. In order to analyze the blocking mechanism of the TPMOS, Figure 2 indicates the influence of d_t on V_{BR} and the electric field distribution of the TPMOS device with $d_t = 2.5$ μm. Seen from Fig. 2(a), V_{BR} increases first and then decreases remarkably with the increase in d_t, and has the maximum 670 V when $d_t = 2.5$ μm, which can be explained by the electric field distribution in Fig. 2(b). The electric field intensity at the J_2 junction curvature (E_J) is very close to that of the trench bottom corners (E_T), so the breakdown occurs at two spots simultaneously. This shows that the maximum electric field of the TPMOS device can transfer from the J_2 junction curvature to the trench bottom corners with the increase in d_t, and V_{BR} is determined by E_J when $d_t < 2.5$ μm, and the trench is shallower, E_J is higher. Whereas V_{BR} is determined by E_T when $d_t > 2.5$ μm, and the trench is deeper, E_T is higher[9]. So the TPMOS with $d_t \approx 2.5$ μm can improve the breakdown voltage.

3.3. Input and output capacitances

The input and output capacitances can affect the device's switching loss. In the conventional VDMOS structure, the input capacitances (C_{in}) and output capacitances (C_{out}) can be expressed in $C_{in} = C_{GS} + (1 + g_m Z)C_{GD}$ and $C_{out} = C_{DS} + C_{GD}$, where C_{GS} is the gate–source capacitance, C_{GD} is the gate–drain capacitance, C_{DS} is the source–drain capacitance, g_m is transconductance and Z is the load resistance. In the TPMOS structure, an additional gate–drain capacitance (C'_{GD}) is formed along the trench sidewalls and increases with the increase in d_t. So C_{in} and C_{out} of TPMOS can be expressed respectively as

$$C_{in} = C_{GS} + (1 + g_m Z)(C_{GD} + C'_{GD}), \tag{2}$$

$$C_{out} = C_{DS} + (C_{GD} + C'_{GD}), \tag{3}$$

where C_{GS}, C_{DS} and C_{GD} of the TPMOS are the same respectively with the counterpoint of the VDMOS for the same structural parameters, so C_{in} and C_{out} of the TPMOS are a little larger than those of the VDMOS due to the additional C'_{GD}. But because C_{DS} increases with increasing V_{DS}, the influences of C'_{GD} on C_{in} and C_{out} will decrease correspondingly.

So the proper shallow trench introduced in the TPMOS can not only eliminate the JFET region and avoid the premature electric field crowding at J_2 junction curvature, thus improving V_{BR} and R_{on}, but also cannot affect obviously the input and output capacitances.

4. Simulation and validation

In order to validate the performance of the new device, as an example of a 600V TPMOS, the structural models of the VDMOS and TPMOS with the same chip area and structural parameters are set up, in which the thickness of the gate oxide layer (t_{ox}) is 0.1 μm, and the thickness of the polysilicon gate is 0.5 μm, the gate length (L_g) is 10 μm, the surface concentrations of the n^+ source and p-type regions are 1×10^{20} cm^{-3} and 1×10^{18} cm^{-3}, respectively, corresponding to the depths, which are 1.5 μm and 3.5 μm, respectively. The concentration and thickness of the n^- drift region are 2.6×10^{14} cm^{-3} and 53 μm, respectively. Additionally, the trench width (w_t) is 4 μm and the depth (d_t) is 1–4 μm. Based on the structural models, the conducting, blocking and switching characteristics of the VDMOS and TPMOS are simulated by ISE simulator and compared.

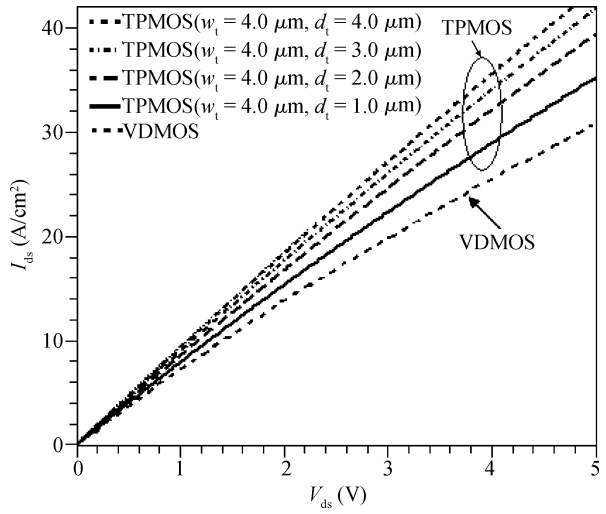

Fig. 3. Comparison of conducting characteristics of the new TPMOS and VDMOS devices.

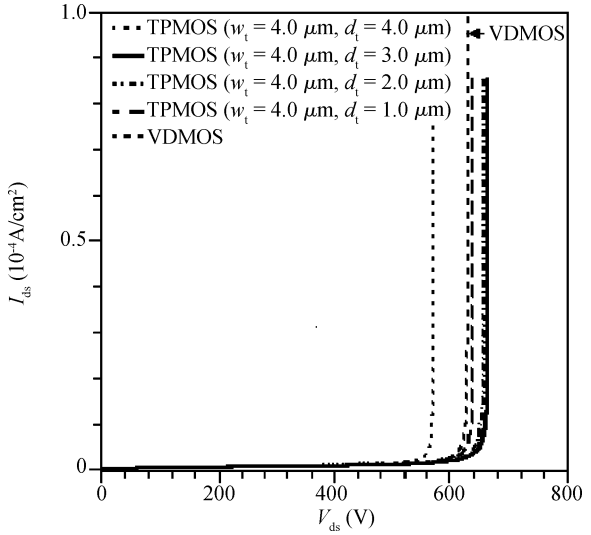

Fig. 4. Comparison of blocking characteristics of the new TPMOS and VDMOS devices.

4.1. Conducting characteristic

Figure 3 indicates the I–V characteristics of the VDMOS and TPMOS devices during conducting, in which the slope of the I–V characteristics curve expresses the specific on-resistance ($R_{on,sp}$). Seen from Fig. 3, $R_{on,sp}$ of the TPMOS is obviously lower than that of the VDMOS. $R_{on,sp}$ of the VDMOS is about 0.16 Ω·cm^2, $R_{on,\,sp}$ of the TPMOS is about 0.12 Ω·cm^2 for w_t = 4 μm and d_t = 3 μm, and it decreases with increasing d_t. This shows that the TPMOS with d_t = 3 μm and w_t = 4 μm can effectively reduce the conduction resistance by about 25%.

4.2. Blocking characteristic

Figure 4 indicates the I–V characteristics of the VDMOS and TPMOS during blocking. Seen from Fig. 4, V_{BR} of the VDMOS is about 630 V, and V_{BR} of the TPMOS is about 663 V for given w_t = 4 μm and d_t = 3 μm. This shows that the TPMOS can improve the breakdown voltage at d_t = 3 μm and w_t = 4 μm by about 5.2%.

4.3. Capacitance characteristic

Figure 5 indicates the variation curves of C_{out} with the drain voltage of the VDMOS and TPMOS. Seen from Fig. 5, for given d_t = 3 μm and w_t = 4 μm, C_{out} of the TPMOS is a little higher than C_{out} of the VDMOS when V_{DS} < 3 V, but C_{out} of the TPMOS is close to C_{out} of the VDMOS when V_{DS} > 3 V. This is because C_{DS} increases with increasing V_{DS}, resulting in the decrease in the contribution of additional C'_{GD} to C_{out}. Thus out capacitances of the TPMOS and VDMOS are very close at normal operation voltage.

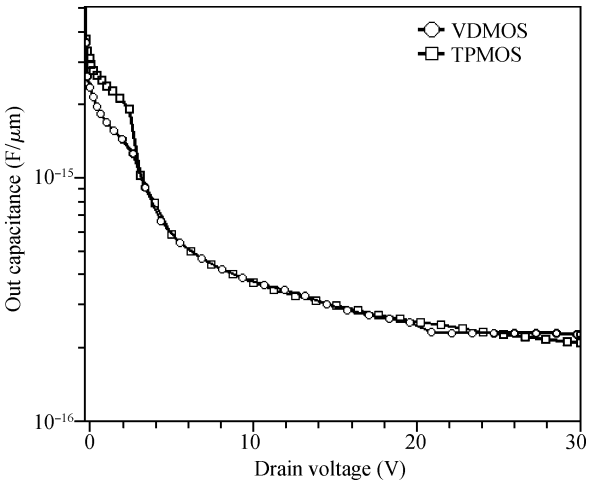

Fig. 5. Comparison of output capacitances of the new TPMOS and VDMOS devices.

4.4. Optimization of L_g

In the conventional VDMOS, the cell space (s_p) or gate length (L_g) has a significant influence on the blocking and conducting characteristics of the VDMOS, and the small s_p or L_g is beneficial to the improvement of V_{BR}, but it causes the increase in R_{on}. In order to analyze further the influences of L_g on V_{BR} and $R_{on,\,sp}$ of the TPMOS device, Figure 6 shows a comparison of V_{BR} and $R_{on,\,sp}$ of the VDMOS and TPMOS with d_t = 3 μm at difference L_g. Seen from Fig. 6, when L_g changes from 8 to 14 μm, corresponding to w_t changes from 2 to 8 μm, $R_{on,\,sp}$ of the TPMOS retains the fixedness with L_g in Fig. 6(a), and V_{BR} experiences a little rise with the increase in L_g in Fig. 6(b); but $R_{on,\,sp}$ and V_{BR} of the VDMOS decrease obviously with increasing L_g. This shows that the TPMOS device can decrease remarkably the dependence of V_{BR} and R_{on} on L_g, and offer more freedom to device design and fabrication.

In view of the practical process, the shallower and wider trench is easily realized by etching, and the process cost is also lower. But the wider trench or the longer L_g can decrease the cell number for a given chip area, resulting in the fall of the current rating. Based on the analysis results, for the 600 V TPMOS device, to obtain the trade-off relation among blocking, conducting and switching characteristics, the depth and width of the trench can be chosen at ranges of 2.5–3 μm and 4 μm

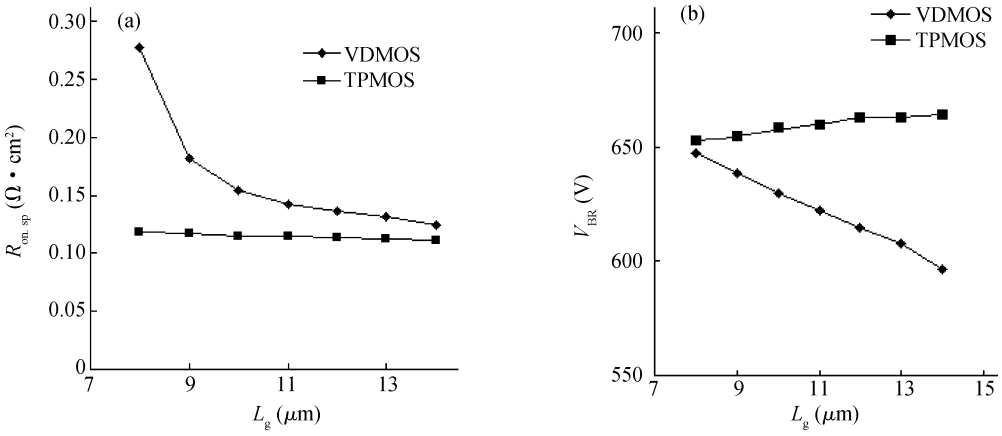

Fig. 6. Comparison of (a) $R_{on,sp}$ and (b) V_{BR} of the VDMOS and TPMOS with $d_t = 3$ μm at difference L_g.

respectively, and corresponding to L_g of about 10 μm.

5. Conclusion

The new proposed trench-planar gate MOSFET structure based on VDMOS technology offers remarkable improvements in conducting and blocking characteristics. Compared with the conventional VDMOS, the on-resistance can decrease by about 25%, the breakdown voltage can improve by about 5.2% and the out capacitance can retain the immovability. Furthermore, the 2.5–3 μm depth and 4 μm width trench region can be realized easily by the existing etching, and it retains the simple technology of the VDMOS. Thus the further requirements of high voltage power switch applications can be fulfilled with the TPMOS structure.

References

[1] Deboy G, Marz M, Stengl J P, et al. A new generation of high voltage MOSFETs breaks the limit line of silicon. Proc Int Electron Device Meeting (IEDM), 1998: 683

[2] Wang C L, Sun J. An oxide filled extended trench gate super junction MOSFET structure. Chin Phys B, 2009,18(3): 1231

[3] Ninomiya H, Miura Y, Kobayashi K. Ultra-low on-resistance 60–100 V superjunction UMOSFETs fabricated by multiple ion-implantation. Proc IEEE ISPSD, 2004: 177

[4] Nitta T, Minato T, Yano M, et al. Experimental results and simulation analysis of 250 V super trench power MOSFET (STM). Proc IEEE ISPSD, 2000: 77

[5] Yamauchi S, Shibata T, Nogami S, et al. 200V Super Junction MOSFET fabricated by high aspect ratio trench filling. Proc IEEE ISPSD, 2006: 65

[6] Li Zehong, Ren Min, Zhang Bo, et al. Above 700 V superjunction MOSFETs fabricated by deep trench etching and epitaxial growth. Journal of Semiconductors, 2010, 31(8): 084002

[7] Khanna V K. Insulated gate bipolar transistor (IGBT): theory and design. Piscataway: IEEE Press, 2003: 518

[8] Spulber O, Narayanan E M S, Hardikar S, et al. A novel gate geometry for the IGBT: a novel gate geometry for the IGBT: the trench planar insulated gate bipolar transistor (TPIGBT). IEEE Electron Device Lett, 1999, 20(11): 580

[9] Sun Cheng. New structure and process research of power MOSFET. Xi'an University of Technology, 2009: 30