Super junction LDMOS with enhanced dielectric layer electric field for high breakdown voltage*

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Abstract: The lateral super junction (SJ) power devices suffer the substrate-assisted depletion (SAD) effect, which breaks the charge balance of SJ resulting in the low breakdown voltage (BV). A solution based on enhancing the electric field of the dielectric buried layer is investigated for improving the BV of super junction LDMOSFET (SJ-LDMOS). High density interface charges enhance the electric field in the buried oxide (BOX) layer to increase the block voltage of BOX, which suppresses the SAD effect to achieve the charge balance of SJ. In order to obtain the linear enhancement of electric field, SOI SJ-LDMOS with trenched BOX is presented. Because the trenched BOX self-adaptively collects holes according to the variable electric field strength, the approximate linear charge distribution is formed on the surface of the BOX to enhance the electric field according to the need. As a result, the charge balance between N and P pillars of SJ is achieved, which improves the BV of SJ-LDMOS to close that of the idea SJ structure.

Key words: super junction; LDMOS; substrate-assisted depletion effect
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1. Introduction

Modern power electronics technology requires power devices with superior performance in high voltage, high speed and low loss, super junction (SJ) device as a new type of power device can further improve the breakdown voltage (BV), and reduce the specific on-resistance (R_{on})[1−3]. In the SJ device, a set of alternating and heavily doped N and P pillars constitute the drift region to achieve charge compensation in the off-state. The charge compensation results in the uniform electric field distribution to increase the BV for a given drift region length. On the other hand, the heavily doped N-pillars significantly decrease the specific on-resistance. For the SJ-MOSFET, the constraint relation between R_{on} and BV is improved, which breaks the "silicon limit" in conventional device[4], and improves the tradeoff between the BV and R_{on}. As SJ technology is applied in LDMOS (lateral double-diffused MOSFET), becomes SJ-LDMOS to improve the performance of device. However, the vertical electric field destroys the charge balance of SJ resulting in the low BV, which is called "substrate-assisted depletion (SAD) effect"[5]. This effect is particularly evident in the case of the SJ structure implemented on a SOI (silicon-on-insulator) substrate. It is due to the fact that an inversion layer forms below the buried oxide layer (BOX) like a MOS capacitor structure resulting in a vertical electric field component which is a function of the lateral position in the drift region. The vertical electric field depletes a part of N-type charges in N-pillars of SJ, which gives rise to surplus of P-type charges in P-pillars. The delicate charge balance is broken between the N and P pillars of SJ, resulting in the decrease of the BV.

Some specific structures have been reported to relieve the SAD effect. Adopted solutions in these structures can be roughly classified to three categories. The first option is to completely remove the substrate depletion by using an insulating substrate[6] such as sapphire or removing the silicon substrate by back etching[7]. The second option is to improve the charge balance between N and P pillars in SJ by charge compensation, such as unbalanced SJ-LDMOS[8], SJ/RESURF LDMOS[9], SLOP LDMOS[10] and SJ-LDMOS with N-buffer layer[11]. The third option is to avoid the charge imbalance of SJ by replacing P-pillars with oxide-bypassed (OB) structure[12,13]. A new solution based on enhancing dielectric layer electric field is investigated in this paper to overcome the SAD effect. Almost all vertical block voltage is assigned to BOX because the high density interface charges enhance the electric field in BOX, which suppresses the influence of vertical electric field on SJ. For promoting the precise charge balance of SJ, it is necessary to pursue the linear interface charge distribution. We have preliminary proposed a SOI SJ-LDMOS with trenched TBOX[14], the TBOX captures the holes as a dynamic interface charge layer to enhance the electric field of BOX. Because TBOX self-adaptively collect charges according to the variable electric field strength, the approximate linear charge distribution is achieved. In this paper, the performances of SJ-LDMOS with TBOX are further investigated on the basis of the proposed solution.

2. ENDIF SJ-LDMOS

For the high voltage SOI LDMOS in the off-state, the ver-

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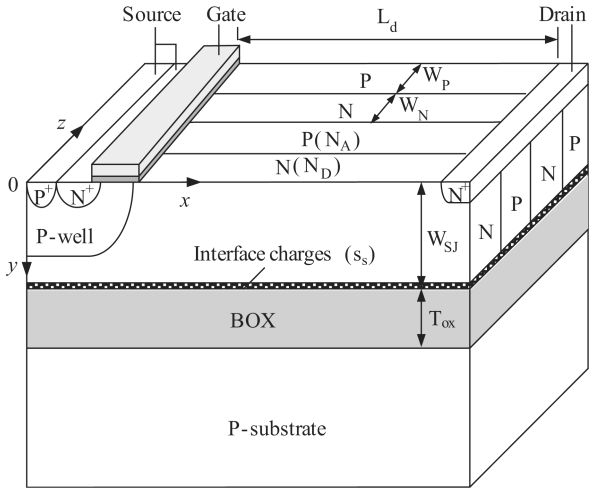

Fig. 1. Three-dimensional structure of ENDIF SJ-LDMOS.

tical block voltage V_{ver} is undertaken by the SOI layer and BOX layer, which is expressed as $V_{ver} = V_s + V_{BOX}$, where V_s and V_{BOX} are the vertical voltage components in silicon and BOX layer, respectively. Because the electric field in SOI is approximately linear, V_{ver} can be represented by

$$V_{ver} = 0.5T_{dep}E_s + E_{ox}T_{ox}, \tag{1}$$

where E_s is the maximum electric field in the silicon layer, and E_{ox} is the electric field in BOX. T_{dep} is the vertical depletion width in the silicon layer, and T_{ox} is the thickness of the BOX. By the continuity of electric displacement including interface charge, E_{ox} is shown as

$$E_{ox} = E_s\varepsilon_s/\varepsilon_{ox} + q\sigma_s/\varepsilon_{ox}, \tag{2}$$

where ε_s and ε_{ox} are the dielectric constants of silicon and oxide, respectively. σ_s is the interface charge density.

In the conventional SOI SJ-LDMOS, $\sigma_s = 0$, so $E_{ox} = \varepsilon_s E_s/\varepsilon_{ox}$. According to the Poisson equation, $E_s = qN_D T_{dep}/2\varepsilon_s$, N_D is the doping concentration of N pillars of SJ and set the widths of N and P pillars are equal. So the V_{ver} is obtained as

$$V_{ver} = \frac{qN_D}{2\varepsilon_s}\left(\frac{T_{dep}^2}{2} + \frac{\varepsilon_s T_{dep}T_{ox}}{\varepsilon_{ox}}\right). \tag{3}$$

With the increasing of drain voltage, the vertical block voltage V_{ver} increases and the vertical depletion charges are from the N pillars of SJ, which can be shown as

$$Q_{ver} = qN_D T_{dep}/2. \tag{4}$$

Equation (4) shows that the N-pillars are induced with the inversion layer below the BOX in addition to depleting with P-pillars. The P-type charges coming from P-pillars are surplus. The charge imbalance will result in the high electric field at drain region, which reduces the BV dramatically.

For the SJ-LDMOS with enhanced dielectric layer electric field (ENDIF SJ-LDMOS) as shown in Fig. 1, σ_s is greatly

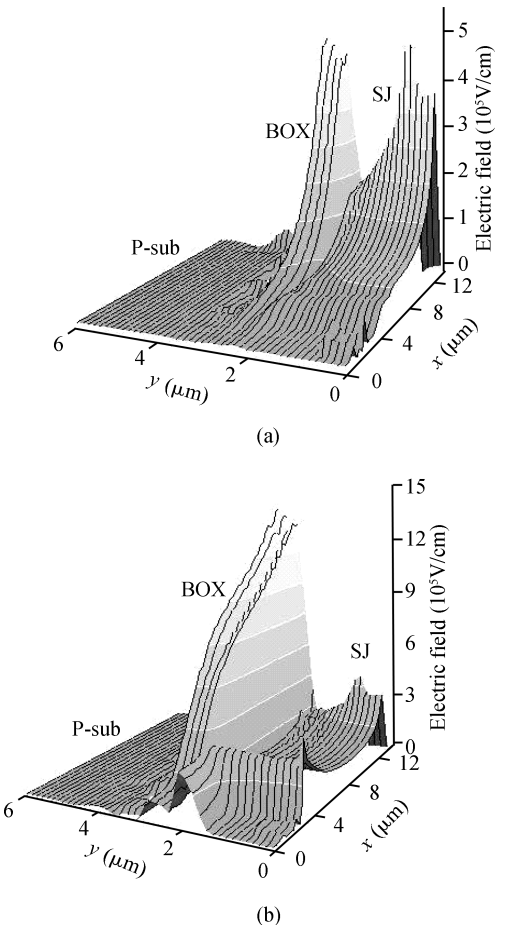

Fig. 2. Electric field distribution at x–y plane of SJ-LDMOS. (a) Conventional SOI SJ-LDMOS, $\sigma_s = 0$. (b) ENDIF SJ-LDMOS, $\sigma_s = 2 \times 10^{12}$ cm^{-2}.

increased by the electric field enhancing technology, and enhanced electric field $E_{en} = q\sigma_s/\varepsilon_{ox}$, so V_{ver} is represented by

$$V_{ver} = \frac{qN_D}{2\varepsilon_s}\left(\frac{T_{dep}^2}{2} + \frac{\varepsilon_s T_{dep}T_{ox}}{\varepsilon_{ox}}\right) + \frac{T_{ox}}{\varepsilon_{ox}}q\sigma_s. \tag{5}$$

We assume $\Delta V = q\sigma_s T_{ox}/\varepsilon_{ox}$, the vertical depletion charges coming from N pillars can be reduced, which are expressed as, $Q_{ver} = qN_D T_{dep}/2 \rightarrow V_{ver} - \Delta V$. When the interface charges are sufficient for all vertical voltage, $V_{ver} = q\sigma_s T_{ox}/\varepsilon_{ox}$, the N pillars does not participate in the vertical depletion, $Q_{ver} = 0$, the charge imbalance is eliminated.

Three-dimensional device simulations were performed by ISE TCAD at fallowing device parameters ($L_d = 10$ μm, $W_N = W_P = 1$ μm, $T_{SJ} = 2$ μm, $T_{ox} = 1$ μm, $N_D = N_A = 4 \times 10^{16}$ cm^{-3}). According to the simulation results, Figure 2 compares the electric field distribution of SOI SJ-LDMOS at different interface charge densities to illuminate the operation of ENDIF SJ-LDMOS. For the conventional SOI SJ-LDMOS, $\sigma_s = 0$, the vertical electric field is produced by the ionized positive charges coming from N pillars and the inversion layer (electrons) below BOX, which results in the charge imbalance between N and P pillars of SJ. Electric field in SJ and BOX rapidly increases from source to drain region because charge imbalance causes concentration of electric fluxlines, which results in the low BV of 64 V. For the ENDIF SJ-LDMOS, $\sigma_s =$

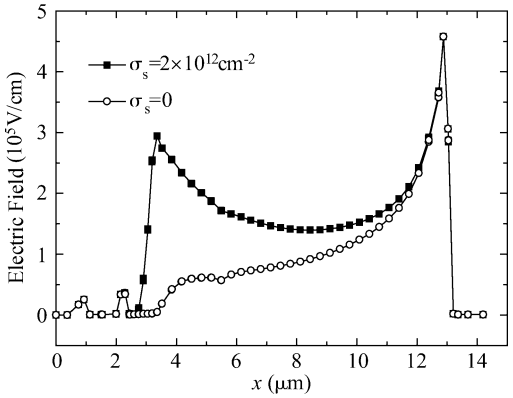

Fig. 3. Electric field profiles at surface of SJ-LDMOS along the center line of P pillars.

2×10^{12} cm^{-2}, the interface charges enhance the electric field of BOX to 1.3×10^6 V/cm from 4.8×10^5 V/cm of conventional device. The increased voltage ΔV undertakes the partial vertical voltage to improve the charge balance, so the electric field distribution in SJ is improved. As a result, the higher BV of 162 V is obtained.

Figure 3 shows the surface electric field of SOI SJ-LDMOS when $\sigma_s = 0$ and 2×10^{12} cm^{-2}. In the absence of interface charges, the high electric field in drain region causes premature breakdown. When $\sigma_s = 2 \times 10^{12}$ cm^{-2}, the electric field is improved to arc distribution, which is different from rectangular distribution of ideal SJ. Because the vertical block voltage component is a function of the lateral position in the drift region, the uniform interface charge density can't satisfy the requirement of enhancing electric field.

Supposing SJ achieves the charge balance, the lateral potential in drift region of SJ-LDMOS is linear distribution, which is expressed as

$$V_{\text{lat}}(L_{\text{x}}) = kL_{\text{x}} = \frac{\text{BV}}{L_{\text{d}}}L_{\text{x}}, \quad L_{\text{x}} \in [0, L_{\text{d}}], \tag{6}$$

where L_{x} is the position parameter in drift region, L_{d} is the length of drift region, and k is the linear coefficient. Because the substrate always is zero potential, the vertical block voltage V_{ver} is function satisfying Eq. (6), which can be written as $V_{\text{ver}}(L_{\text{x}}) = \text{BV}L_{\text{x}}/L_{\text{d}}$. For satisfying the balance condition, the interface charges should be linear distribution according to the enhancing electric field principle, which can be obtained as

$$Q_{\text{s}}(L_{\text{x}}) = q\sigma_{\text{s}}(L_{\text{x}}) = \frac{V_{\text{ver}}(L_{\text{x}})\varepsilon_{\text{ox}}}{T_{\text{ox}}} = \frac{\text{BV} \times \varepsilon_{\text{ox}}}{L_{\text{d}}T_{\text{ox}}}L_{\text{x}}. \tag{7}$$

The vertical voltage is highest at drain region, and the corresponding interface charge density is highest, which can be represented by

$$\sigma_{\text{s-max}} = \sigma_{\text{s}}(L_{\text{x}})|_{L_{\text{x}}=L_{\text{d}}} = \frac{\text{BV} \times \varepsilon_{\text{ox}}}{qT_{\text{ox}}}. \tag{8}$$

3. TBOX SJ-LDMOS

For approaching the idea interface charge distribution as Eq. (7), the SOI SJ-LDMOS with trenched buried oxide (TBOX SJ-LDMOS) is presented, as shown in Fig. 4. Surface drift region still is SJ structure consists of alternation of N and P pillars. The prominent characteristic of the proposed structure is the TBOX is implemented as insulator. TBOX forms dielectric charge traps capturing the mobile charges (holes), and the captured charges enhances the electric field in BOX as interface charges. The TBOX is self-adaptive to collect the additional charges according to the variable electric fields strength, which forms a dynamic buffer between SJ and substrate. More importantly, these charges in trenches are approximate linear distribution from source to drain region according to the vertical potential. In addition, there is the partial reservations of N epitaxy layer (N-epi) blew the SJ for avoiding the SJ process in trenches. Worthy of note is that the N-epi layer can slightly compensate charges in N pillars, so the doping concentration of epitaxy should be low for preventing the destruction of linear feature of interface charge.

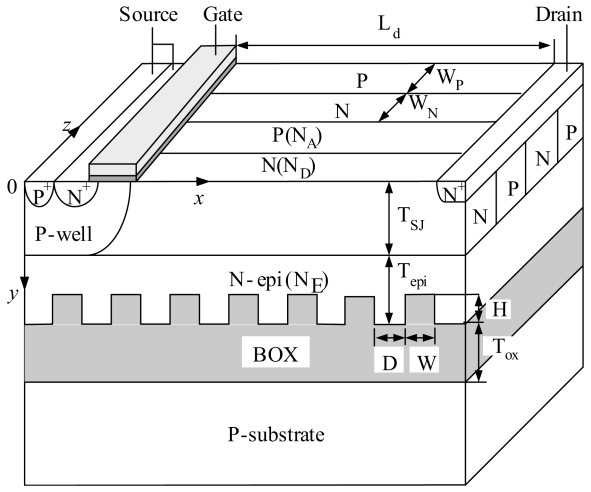

Fig. 4. Three-dimensional structure of TBOX SJ-LDMOS.

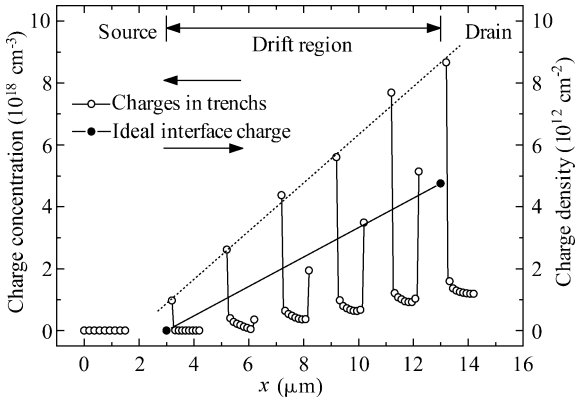

Fig. 5. Charge distribution on the surface of BOX at BV point ($N_{\text{E}} = 2 \times 10^{15}$ cm^{-3}, $W = D = 0.5$ μm, $H = 1$ μm).

In order to verify the performance of the TBOX SJ-LDMOS, three-dimensional device simulations were performed by ISE[15], and major device parameters are as follows: $L_{\text{d}} = 10$ μm, $W_{\text{N}} = W_{\text{P}} = 1$ μm, $T_{\text{SJ}} = 2$ μm, $T_{\text{epi}} = 1.5$ μm $T_{\text{ox}} = 1$ μm, $N_{\text{D}} = N_{\text{A}} = 4 \times 10^{16}$ cm^{-3}.

The charge distribution in trenches is important feature of device operation. Figure 5 shows the charge distribution at

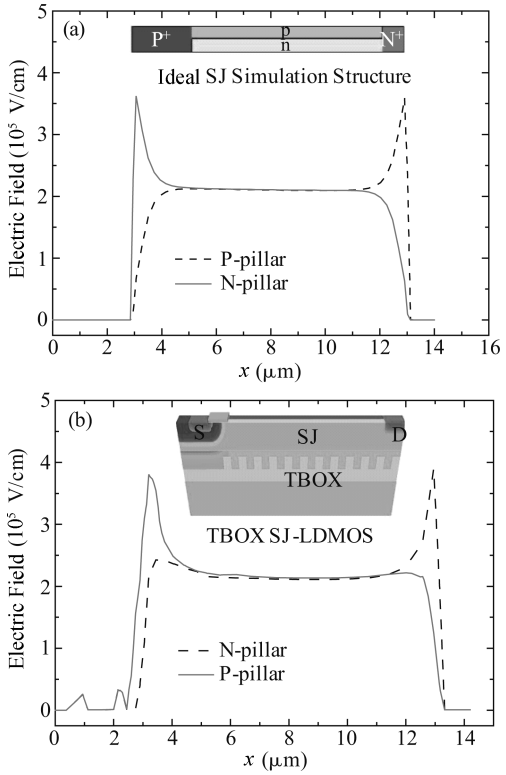

Fig. 6. Simulation structures and the corresponding electric field distributions in SJ at breakdown. (a) Idea SJ structure. (b) TBOX SJ-LDMOS and electric field at $y = 0.1$ μm. $N_E = 2 \times 10^{15}$ cm^{-3}, $W = 0.5$ μm, D = 0.5 μm, $H = 1$ μm.

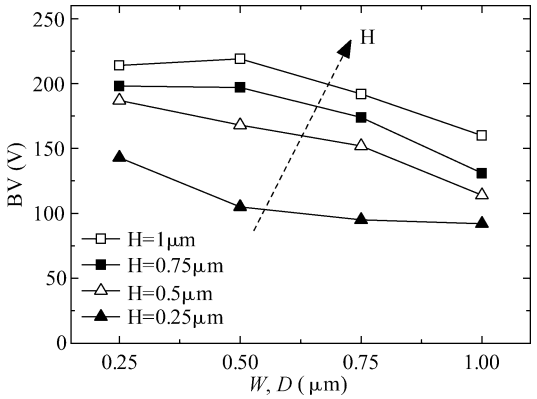

Fig. 7. Dependence of BV on the size of trenches.

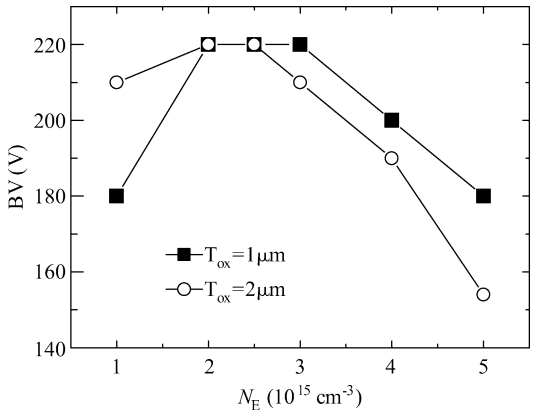

Fig. 8. Influence of N-epi doping concentration on BV of TBOX SJ-LDMOS at different BOX thicknesses.

BV of 220 V. If the vertical voltage all is undertaken by the BOX, according to Eq. (8), the highest interface charge density $\sigma_{\text{m s-max}}$ is 4.75×10^{12} cm^{-2} in the drain region. The lowest charge density $\sigma_{\text{s-min}}$ is 0 at source region, and the idea distribution is linear in drift region. For the TBOX SJ-LDMOS, the accumulated charges (holes) only present in trenches, which forms the discrete distribution. Because the holes quantity is variable with the vertical electric field strength, the charge concentration distribution approximate is linear from source to drain region. From Fig. 5, the charges in one trench are U-shaped distribution, and the charge concentration in the corner is higher than that in the middle part of trench. Further, in a given trench, the charges concentrate at the source side of trench is higher than that at drain side because charges move toward source side under the influence of lateral electric field. The highest concentration in the trench is about 9×10^{18} cm^{-3}. Because the charge accumulation layer is very thin, the charge density is high enough to undertake the all vertical block voltage, so the SAD effect is suppressed thoroughly.

A 2-dimensional SJ diode structure is adopted to simulate the idea SJ. The widths and concentrations of N and P pillars are 1 μm and 4×10^{16} cm^{-3} respectively, which are the same as parameters of TBOX SJ-LDMOS. Figure 6 compares the electric field distribution of the idea SJ and TBOX SJ-LDMOS at $y = 0.1$ μm. The almost same electric field is obtained in two structures because the SAD effect in TBOX SJ-LDMOS is eliminated. For the TBOX SJ-LDMOS, the peaks of electric field along the N and P pillar are equal at source and drain, indicating that the charge balance of SJ is achieved. The electric field in drift region is straight, which results in the high BV of 219 V close to 220 V of idea SJ.

The influence of size of trenches on BV is investigated in Fig. 7. With reducing the width W/D and increasing the depth H, it is helpful to capture more holes for enhancing the electric field. As a result, when $H = 1$ μm, the accumulated charges are more adequate than that of 0.75 μm, 0.5 μm and 0.25 μm, so the BV is higher. Similarly, when $W/D = 0.25$ μm, the accumulated charges are more sufficient. But the highest BV is obtained at $W = D = 0.5$ μm, $H = 1$ μm, instead of $W = D = 0.25$ μm, $H = 1$ μm. The reason is that the N-epi layer provides the excess positive charges, so the compromise trench size is the latter.

Figure 8 shows the influence of N-epi concentration on BV at different BOX thicknesses. The depleted positive charge in N-epi can make up for the shortage of accumulated charges in trenches, but we should try to improve the charges in trenches for exerting its self-adaptive advantage. Usually, the N-epi concentration is very low. When $H = 1$ μm, $W = 0.5$ μm, $D = 0.5$ μm, the optimal N-epi concentration is from 2 to 2.5×10^{15} cm^{-3}, the highest BV achieves 219 V at $T_{ox} = 1$ μm and 2 μm. With increasing the concentration, the positive charges are surplus resulting in the decrease in the BV. If $N_E < 2 \times 10^{15}$ cm^{-3}, the BV is lower than the optimal 219 V for the shortage of interface charges. The thicker BOX is useful to tolerate the shortage of N-epi concentration, but not conducive to the ex-

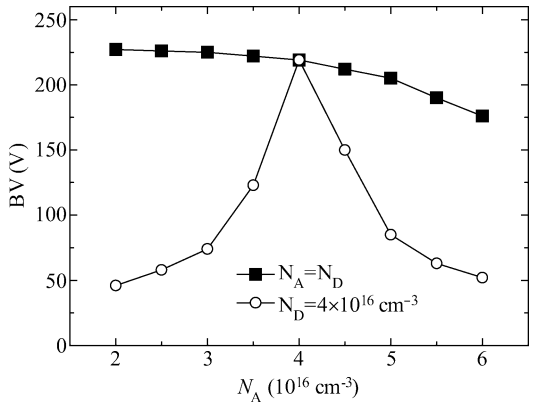

Fig. 9. Influence of the doping concentration in N and P pillars on BV of TBOX SJ-LDMOS.

cess of N-epi concentration.

Figure 9 shows the influence of N and P pillars concentration on the BV of TBOX SJ-LDMOS. When $N_A = N_D$, the BVs change slowly with increasing the concentration because SJ always maintains the charge balance. According to SJ effect, the higher doping concentration reduces the BV, and reduces the on-state resistance also. On the other hand, when N_A is variable from 2×10^{16} to 6×10^{16} cm^{-3} at $N_D = 4 \times 10^{16}$ cm^{-3}, the BVs change severely for the charge imbalance between N and P pillars. The highest BV is obtained at $N_D = N_A = 4 \times 10^{16}$ cm^{-3}, which indicates the SAD effect is eliminated in TBOX SJ-LDMOS.

4. Conclusion

A new solution is proposed to overcome the SAD effect of SOI SJ-LDMOS by enhancing the electric field technology. The high-density interface charges enhance the electric field in BOX to undertake the vertical block voltage of device, which shields the SJ from the substrate depletion. As a result, the proposed solution ensures the charge balance between N and P pillars of SJ, and improves the BV. A TBOX SOI SJ-LDMOS is investigated according to the enhancing electric field principle. TBOX self-adaptive captures the holes, which forms the interface charges for enhancing electric field. The discrete linear charge distribution is obtained in trenches because the concentration of holes is variable according to the vertical electric field strength, which is ideal for improving the charge balance of SJ. Simulation results show that the uniform electric field is achieved in SJ resulting in the BV of 220 V, compared with the 64 V of the conventional device.

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