A low-power 10-bit 250-KSPS cyclic ADC with offset and mismatch correction*

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Abstract: A low power 10-bit 250-k sample per second (KSPS) cyclic analog to digital converter (ADC) is presented. The ADC's offset errors are successfully cancelled out through the proper choice of a capacitor switching sequence. The improved redundant signed digit algorithm used in the ADC can tolerate high levels of the comparator's offset errors and switched capacitor mismatch errors. With this structure, it has the advantages of simple circuit configuration, small chip area and low power dissipation. The cyclic ADC manufactured with the Chartered 0.35 μm 2P4M process shows a 58.5 dB signal to noise and distortion ratio and a 9.4 bit effective number of bits at a 250 KSPS sample rate. It dissipates 0.72 mW with a 3.3 V power supply and occupies dimensions of 0.42 × 0.68 mm^2.

Key words: cyclic ADC; improved RSD algorithm; low power; offset cancelling
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1. Introduction

Recently, analog to digital converters (ADCs) have been in great demand for use in multimedia and communication fields, such as computers, digital media players, and mobile phones. These applications are developed toward low power, low cost and miniaturization for portable products. Consequently, power and area efficient architectures must be used in the ADCs.

Cyclic ADCs are well known for their ability to achieve moderate resolution with small silicon area at low or medium frequencies[1], compared with other ADC architectures, such as pipelined ADCs, successive approximation register (SAR) ADCs, and single slope ADCs[2−4]. Conventional cyclic ADCs are two-stage structures including a sample-and-hold (S/H) stage and a multiplying digital to analog converter (MDAC) stage[5, 6]. In this paper, the architecture of an amplifier's offset cancelling with the inherent S/H function in an MDAC is used to reduce the complexity of the analog circuits. And improved redundant signed digit (RSD) principle in digital correction circuit is employed to compensate for the comparator's offset errors and gain errors resulting from component mismatch. Compared with other mismatch error cancelling structures[1, 6−8], the complexity of the analog circuit is also reduced.

2. Proposed cyclic architecture

2.1. Structure of offset cancelling

Two operational amplifiers are included in conventional cyclic ADCs[5, 6]. One amplifier is used in the S/H structure to sample the analog input signal and the MDAC residue output. The other one is used in the MDAC to achieve residue operation. As shown in Fig. 1, the proposed cyclic ADC consists of a MDAC, an sub-ADC. The S/H structure is removed in the ADC through the architecture of an amplifier shared with two sets of sampling capacitors in the MDAC.

The timing diagram of proposed the MDAC is shown in Fig. 2. The MDAC configurations during different phases A, B, C, and D are shown in Figs. 3(a)–3(d), respectively. Each bit decision requires only one clock phase, and one sample phase, as illustrated in Fig. 3(a), is necessary to cancel the amplifier's offset before all of the nine bit decision phases start (a 10 bit resolution needs nine decision phases).

During the sample phase, the voltage $V_{\rm in}$ is sampled by C1s and C3s while C2s and C4s are reset. The amplifier's offset is sampled on C1f and C3f. The charges stored in capacitors C1s, C3s, C1f and C3f are equal to

$$Q_{1\rm s} = C_{\rm s}(V_{\rm offset} - V_{\rm in+}), \tag{1}$$

$$Q_{3\rm s} = C_{\rm s}(0 - V_{\rm in-}), \tag{2}$$

$$Q_{1\rm f} = C_{\rm f}V_{\rm offset}, \tag{3}$$

$$Q_{3\rm f} = C_{\rm f}(0 - V_{\rm offset}), \tag{4}$$

where $C_{\rm s}$ is the value of the sample capacitors, and $C_{\rm f}$ is the value of the feedback capacitors. $V_{\rm offset}$ is the offset voltage of the amplifier. $V_{\rm in+}$ and $V_{\rm in-}$ are the differential input signal.

During the first bit decision phase, as illustrated in Fig. 3(b), the charges stored in the capacitors are equal to

$$Q_{1\rm s} = C_{\rm s}\frac{V_{\rm offset}}{2}, \tag{5}$$

$$Q_{3\rm s} = C_{\rm s}(0 - \frac{V_{\rm offset}}{2}), \tag{6}$$

$$Q_{1\rm f} = C_{\rm f}(V_{\rm offset} - V_{\rm o1+}), \tag{7}$$

$$Q_{3\rm f} = C_{\rm f}(0 - V_{\rm o1-}), \tag{8}$$

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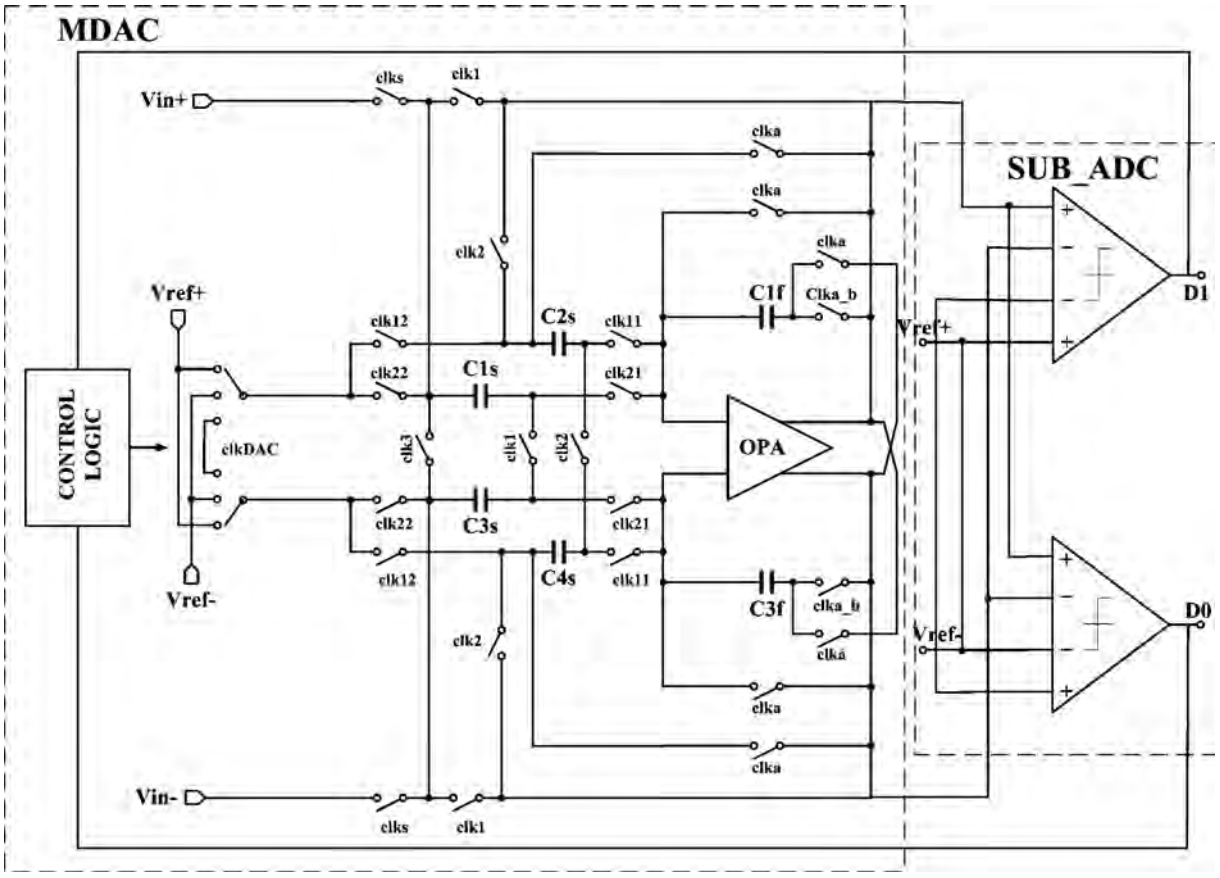

Fig. 1. Schematic diagram of proposed cyclic ADC.

where V_{o1+} and V_{o1-} are the differential outputs. It is supposed that all of the capacitors have the same value ($C_s/C_f = 1$). Because the total charges $Q_{1s} + Q_{1f}$ and $Q_{3s} + Q_{3f}$ are invariable during phases A and B, the output voltage can be obtained from Eq. (1) to Eq. (8) as

$$V_{o1} = V_{in} - V_{offset}, \tag{9}$$

where $V_{o1} = V_{o1+} - V_{o1-}$, and $V_{in} = V_{in+} - V_{in-}$. Therefore, the input voltage V_{in} is transferred to the output and an offset voltage is subtracted from it. Meanwhile, the output voltage V_{o1} is sampled by C2s and C4s, and delivered to the sub-ADC to generate the first 1.5 bit control bit b_1. The charges stored in C2s and C4s are equal to

$$Q_{2s} = C_s\left(\frac{V_{o1+} + V_{o1-}}{2} - V_{o1+}\right), \tag{10}$$

$$Q_{4s} = C_s\left(\frac{V_{o1+} + V_{o1-}}{2} - V_{o1-}\right). \tag{11}$$

Figure 3(c) shows the second bit decision phase. The charges stored in the capacitors are equal to

$$Q_{2s} = C_s(V_{offset} - b_1 V_{ref+}), \tag{12}$$

$$Q_{4s} = C_s(0 - b_1 V_{ref-}), \tag{13}$$

$$Q_{1f} = C_f(V_{offset} - V_{o2+}), \tag{14}$$

$$Q_{3f} = C_f(0 - V_{o2-}), \tag{15}$$

where V_{o2+} and V_{o2-} are the differential residue outputs. V_{ref+} and V_{ref-} are two reference voltages. The first control bit $b_1 =$ 1, –1 or 0 depending on V_{o1} is more than $V_{ref}/4$, less than $-V_{ref}/4$ or between $-V_{ref}/4$ and $V_{ref}/4$ here $V_{ref} = V_{ref} - V_{ref-}$.

From Eq. (7) to Eq. (15), the residue voltage is obtained as

$$\begin{aligned} V_{o2} &= 2V_{o1} + V_{offset} - b_1 V_{ref} \\ &= 2(V_{in} - V_{offset}) + V_{offset} - b_1 V_{ref} \\ &= 2V_{in} - b_1 V_{ref} - V_{offset}, \end{aligned} \tag{16}$$

where $V_{o2} = V_{o2+} - V_{o2-}$. Meanwhile, the residue voltage is sampled by capacitors C1s and C3s, and delivered to the sub-ADC to generate the second control bit b_2 for the next bit decision phase, shown in Fig. 3(d).

After nine bit decision phases, the final residue output $V_{residue}$ is equal to

$$V_{residue} = 2^9 V_{in} - 2^8 b_1 V_{ref} - 2^7 b_2 V_{ref} - \cdots - b_9 V_{ref} - V_{offset}, \tag{17}$$

where the control bit b_i ($i = 1, 2, \ldots, 9$) is equal to 1, –1, or 0, depending on whether the ith residue voltage is more than $V_{ref}/4$, less than $-V_{ref}/4$ or between $-V_{ref}/4$ and $V_{ref}/4$.

Equations (9), (16) and (17) show that each residue voltage only has a negative offset voltage resulting from the offset cancelling structure during the signal sampling phase. After repeating 9 cycles, the total offset error is also equal to $-V_{offset}$. The offset error of the input is equivalent to

$$V_{error} = V_{offset}/2^9 \approx 0. \tag{18}$$

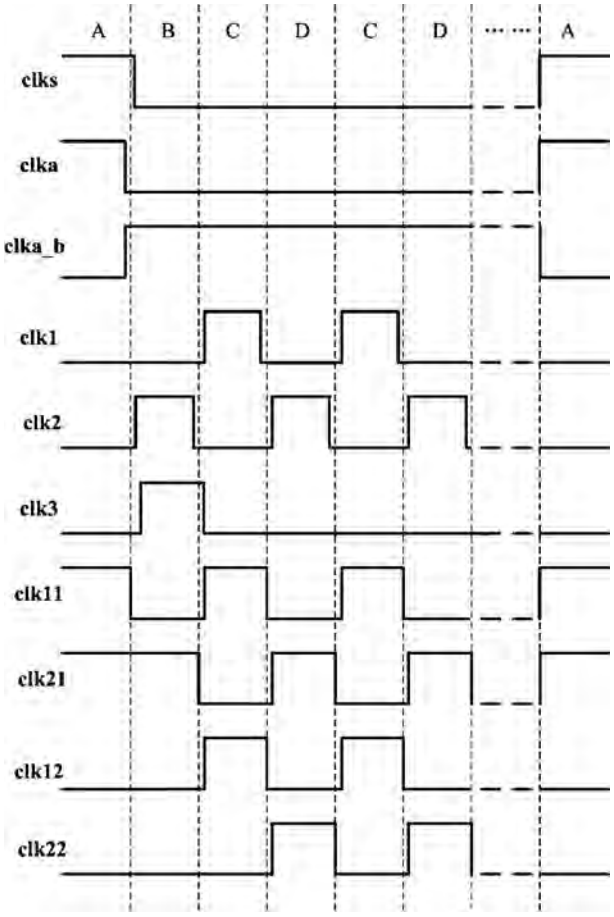

Fig. 2. Timing diagram of the proposed MDAC.

Accordingly, the offset error is considered to be cancelled out. If the offset cancelling at the first sample phase is not used, the offset voltage is added to the residue voltage and multiplied during each phase. The offset error after 9 cycles is

$$V_{\text{error}} = V_{\text{offset}}(1 + 2^1 + \cdots + 2^9). \tag{19}$$

And the offset error of the input is equivalent to

$$V_{\text{error}} = V_{\text{offset}}(1 + 2^1 + \cdots + 2^9)/2^9 \approx 2V_{\text{offset}}. \tag{20}$$

2.2. Improved RSD digital correction technique

The RSD cyclic conversion algorithm is based on the Sweeny–Roberton–Tocher division principle. High levels of comparator's noise and offset are allowed in RSD cyclic ADCs, which lead to the reduction of power consumption[1]. However, the precise multiplication by a factor of 2 is necessary for RSD converters. Therefore, RSD converters require high matching of switched capacitors. Capacitor mismatch error cancelled structures can be used to obtain high resolution cyclic conversion. However, these structures increase the complexity of analog circuits and power consumption[1, 6–8]. In this paper, an improved RSD digital correction technique is utilized to improve the tolerable range of the switched capacitor mismatching ratio. Considering a gain error ($C_s/C_f \neq 1$), Equation (17) can be rewritten as

$$\begin{aligned} V_{\text{residue}} &= (1+\delta)\Big\{(1+\delta)\Big[(1+\delta) \\ &\quad \left(\delta V_{\text{in}} - V_{\text{offset}} - \frac{\delta}{1+\delta} b_1 V_{\text{ref}}\right) \\ &\quad - \frac{\delta}{1+\delta} b_2 V_{\text{ref}} + \delta V_{\text{offset}}\Big] - \cdots - \frac{\delta}{1+\delta} b_9 V_{\text{ref}} + \delta V_{\text{offset}}\Big\} \\ &= \delta(1+\delta)^9 V_{\text{in}} - \delta(1+\delta)^8 b_1 V_{\text{ref}} - \cdots - \delta b_9 V_{\text{ref}} - V_{\text{offset}}, \end{aligned} \tag{21}$$

where gain error factor $\delta = C_s/C_f$.

The RSD correction algorithm is considered the inversion of MDCA residue operation. And $(V_{\text{residue}} + V_{\text{offset}})/\delta(1+\delta)^9$, as the quantized noise voltage, is ignored in the digital domain, and $V_{\text{ref}} = 2^9$ in the digital domain. Thus, from Eq. (21) the algorithm can be written as

$$V_{\text{in}} = 2^9[b_9/(1+\delta)^9 + b_8/(1+\delta)^8 + \cdots + b_1/(1+\delta)]. \tag{22}$$

The conventional RSD correction algorithm is written as

$$V_{\text{in}} = b_9 + 2b_8 + \cdots + 2^8 b_1. \tag{23}$$

If the gain error factor $\delta = 1$, the improved RSD algorithm Equation (22) is equivalent to the conventional RSD correction algorithm Eq. (23). However, due to the mismatch of switched capacitors, the gain error factor δ is not equal to one in the actual circuit. Compared with the conventional RSD algorithm, the improved RSD algorithm is relatively complicated, whereas the result is more accurate given the gain errors. Figure 4 shows the signal to noise and distortion ratio (SNDR) of the proposed cyclic ADC compared with a conventional RSD cyclic ADC with a different switched capacitor mismatching ratio. With the mismatching ratio increasing, the SNDR of the conventional RSD cyclic ADC decreases rapidly, whereas that of the improved RSD cyclic ADC decreases gently. When the mismatching ratio increases to 10%, the SNDR of the proposed cyclic ADC still reaches 55.6 dB and the effective number of bits (ENOB) approximates to 9 bits, while the SNDR and ENOB of the conventional RSD cyclic ADC are only 37.1 dB and 5.9 bits, respectively. Therefore, a high level of capacitor mismatch error is tolerable in the proposed cyclic ADC, which is available in the standard CMOS process.

The improved RSD digital circuit is composed of an accumulator, a calibration factor look-up table (LUT), a multiplicator and some registers. The block diagram is shown in Fig. 5. The improved RSD structure employs a foreground digital calibration technique to measure the gain error factor δ in testing mode and to realize Eq. (22) in conversion mode. The accumulator achieves addition or subtraction, which is controlled by control bits from the sub-ADC. The calibration factors $\Delta = 1/(1+\delta)$ are saved in the LUT, and the range of the calibration factor Δ is from 1/1.95 to 1/2, which realizes 5% mismatching tolerance, and assures ENOB of more than 9 bits. In order to ensure the range of the actual gain factor δ is from 0.95 to 1, the matching of switched capacitors is implemented to be a little less than one. The multiplicator is used to realize Δ^k through self-multiplication.

When the ADC starts operating, the digital circuit is set in testing mode first. The calibration factor Δ is set to 1/2. The

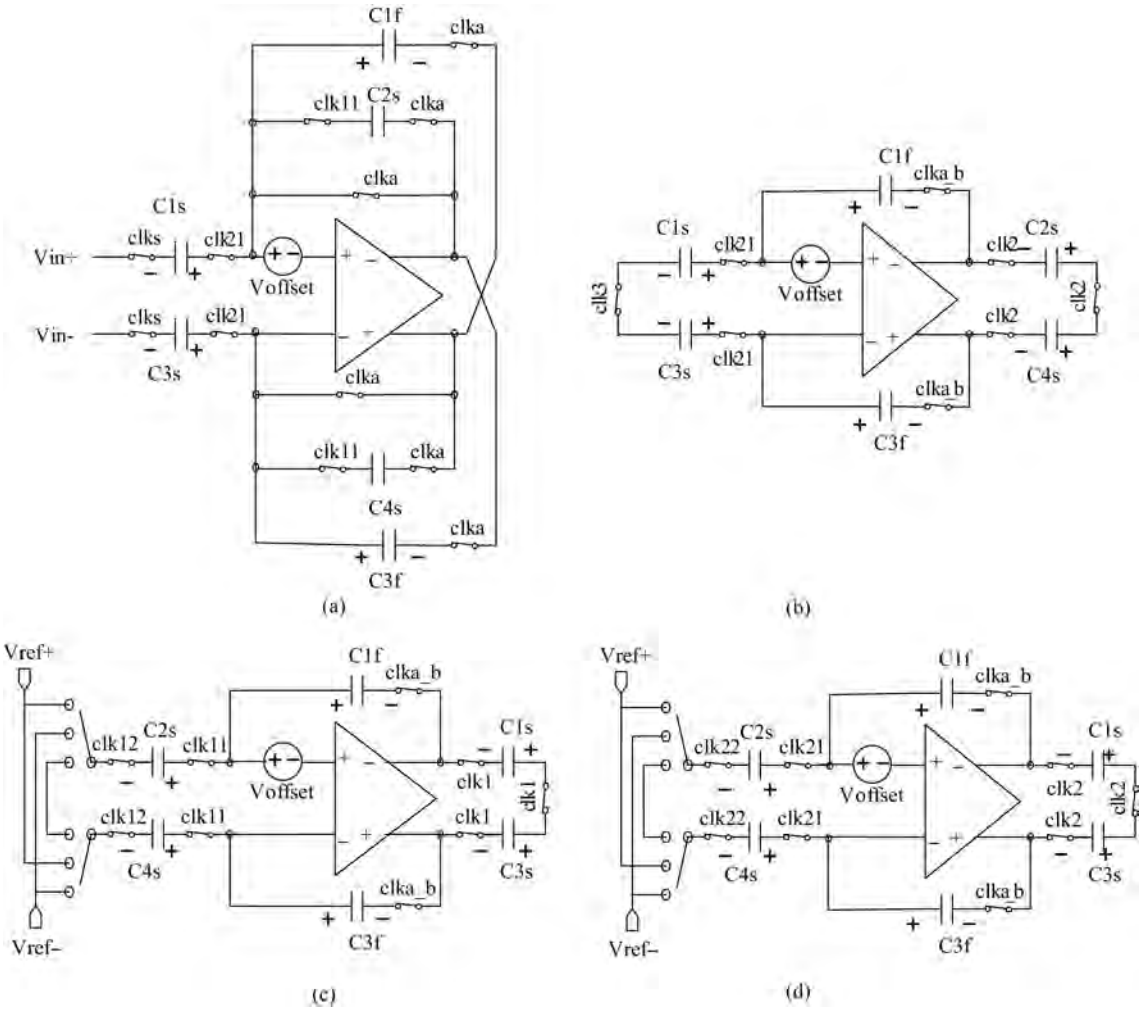

Fig. 3. MDAC configurations during different phases.

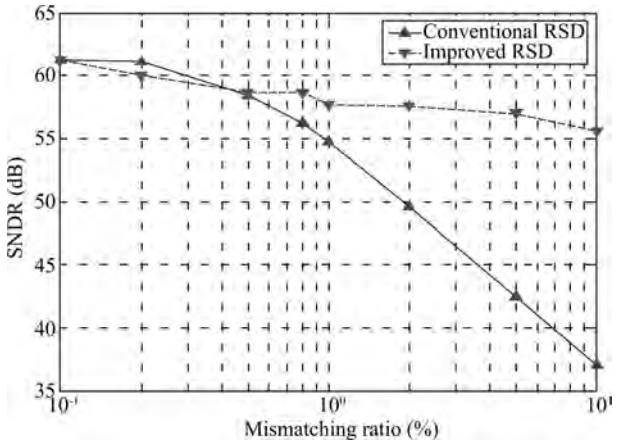

Fig. 4. SNDR versus switched capacitor mismatching ratio.

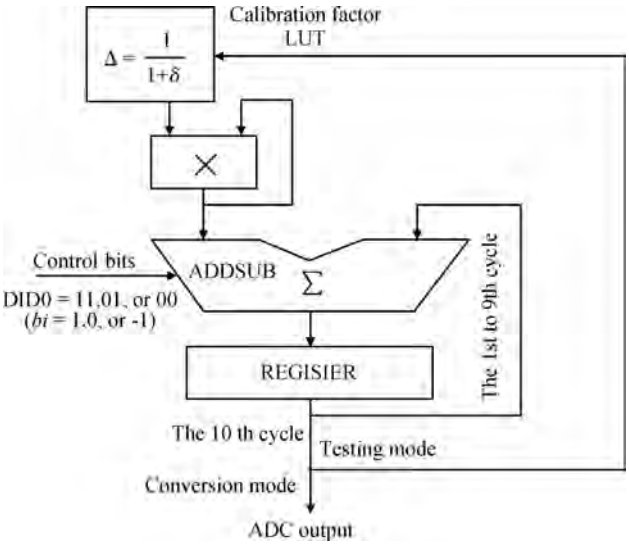

Fig. 5. Block diagram of the improved RSD correction.

input of the cyclic ADC is connected to the reference voltage V_{ref}, and the calibration factors $1/2^k, k = 1, 2, ..., 9$ are used to achieve conventional RSD function in Eq. (23). Because gain errors exist in the MDAC, the output code is inaccurate. Figure 6 shows the potential output codes referring to different gain error factors. By checking the output code, the actual gain error factor δ is determined and a relevant calibration factor Δ is read out from the LUT. Then the circuit is changed to conversion mode, the input of the cyclic ADC is connected to the actual signal, and Δ^k are used to achieve Eq. (22) to correct the gain error. By increasing the tolerable gain error range, the implementation of the cyclic ADC is simplified, which results in the reduction in the chip area and power consumption.

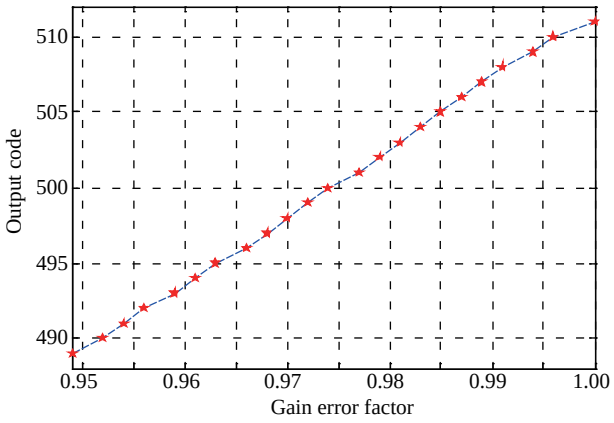

Fig. 6. Output code versus gain error factor.

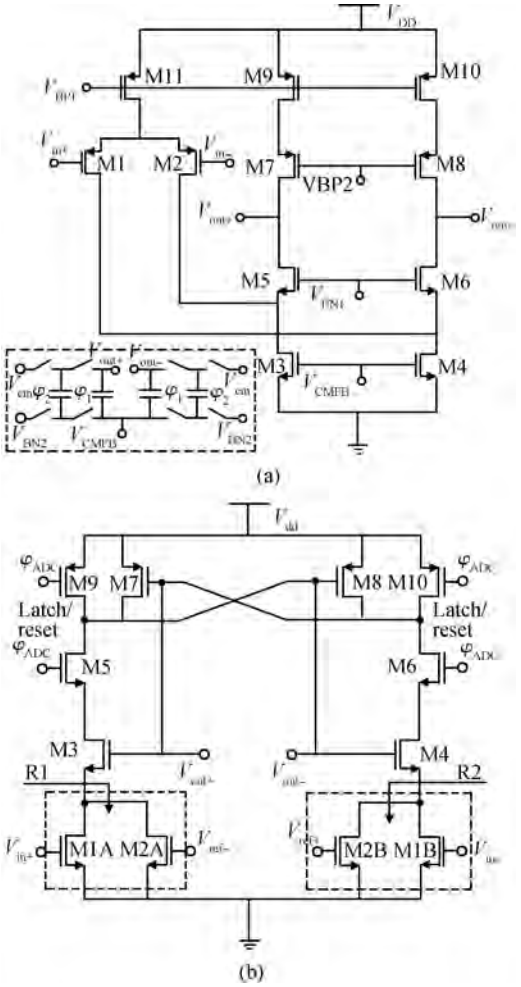

Fig. 7. (a) Amplifier circuit. (b) Comparator circuit.

Compared with other calibration algorithms[9, 10], the proposed structure can be easily realized in a digital circuit.

2.3. Design of the low-power amplifier and comparators

In cyclic ADCs, the amplifier and comparators dissipate most of the power. Hence, the proper design of amplifier and comparators can significantly reduce power consumption. Because the improved RSD algorithm can tolerate high levels of gain error and comparator's offset, relatively simple structures

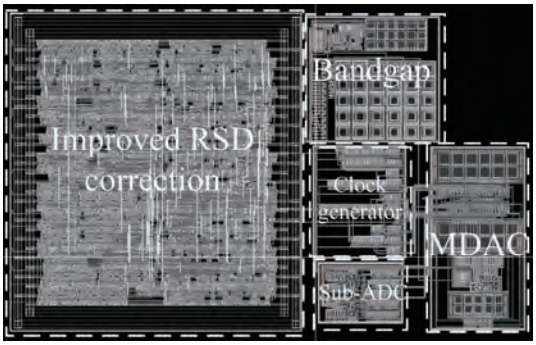

Fig. 8. Layout of the cyclic ADC.

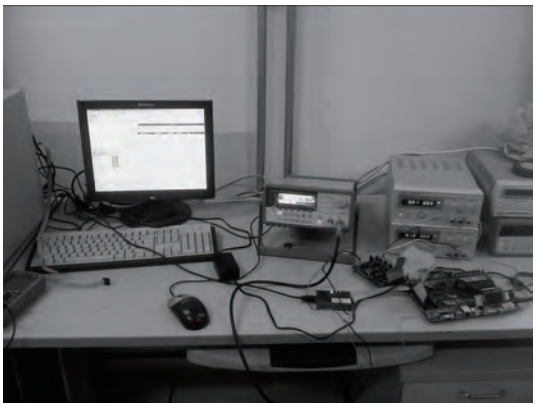

Fig. 9. Test system.

of amplifier and comparators are used in the proposed ADC, resulting in the reduction in power consumption, as shown in Fig. 7.

A low-power fully differential folded cascade amplifier with switched capacitors common-mode feedback net is used in the MDAC. This structure provides large output swing with low power. The post-layout simulated results show that the amplifier has a 73 dB DC gain, 72° phase margin and 16 MHz bandwidth with 0.3 mW power consumption. Two dynamic comparators with latch structure are utilized in the sub-ADC. This structure has the advantages of low power and high speed. The power consumption of the comparator is only 25 μW.

3. Experimental results

The prototype circuit of a 10 bit cyclic ADC has been designed using a Chartered 0.35 μm CMOS process. As shown in Fig. 8, the chip area is 0.42×0.68 mm^2.

The test system is illustrated in Fig. 9. As the test signal of the ADC, a 3 kHz full scale sine wave signal is generated through an Agilent 33250A waveform generator and a MAX275 antialiasing filter. The clock and reset signals are provided by FPGA. A Tektronix TLA5201 logic analyzer is used to record the results. Measured results show that the differential nonlinearity (DNL) is within –0.71/0.8 LSB and the integral nonlinearity (INL) is within –0.81/0.85 LSB, as shown in Fig. 10(a). At a conversion rate of 250-k sample per second (KSPS), the measured SNDR is 58.5 dB, as shown in Fig. 10(b).

The ADC dissipates 0.72 mW with a 3.3 V supply. The

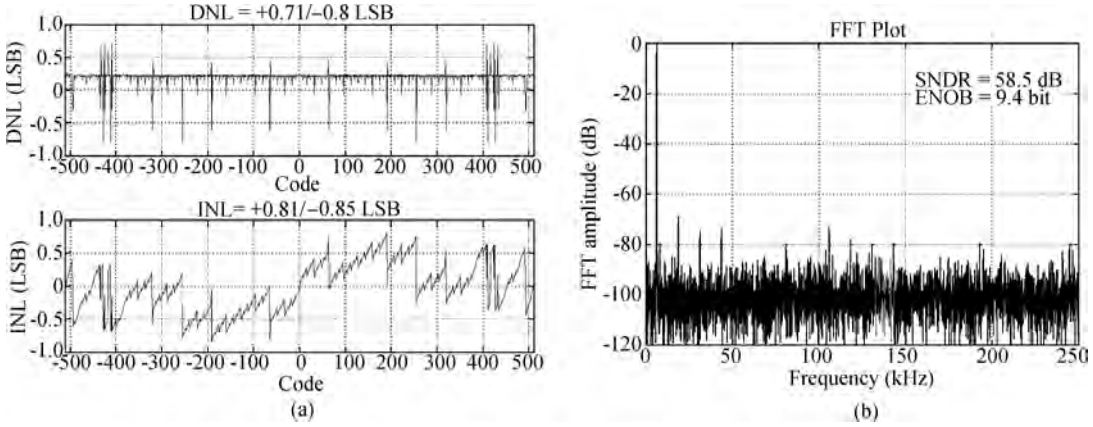

Fig. 10. (a) DNL and INL of the ADC. (b) Output spectrum for input frequency of 3 kHz.

Table 1. Comparison with some previous works.

Parameter	Ref. [8]	Ref. [11]	Ref. [12]	Ref. [13]	Ref. [14]	This work
Resolution (bit)	12	10	12	8	14	10
Technology (μm)	0.35	0.35	0.35	0.18	0.18	0.35
Active area (mm^2)	0.63	N/A	0.175	0.12	1.04	0.28 (with bandgap and digital circuit)
Conversion rate (MHz)	0.667	1	0.143	0.004	0.357	0.25
SNDR (dB)	60.8	56	N/A	47.1	70.1	58.5
Supply voltage (V)	3.3	3	3.5	1.8	3	3.3
Power consumption (mW)	21	< 100	3.94	0.0125	4.2	0.72
FOM (pJ/step)	30.7	< 158	> 6.7	17.2	4.3	4.2

common figure of merit (FOM) is 4.2 pJ/step according to

$$\mathrm{FOM} = \frac{P}{2^{\mathrm{ENOB}} \times f_{\mathrm{s}}}, \tag{24}$$

where P is the power consumption and f_{s} is the sampling rate. Table 1 shows the comparison of the proposed ADC with several previous works. Compared with other cyclic structures, the proposed ADC has the advantages of superior FOM, relatively simple circuit configuration, small chip area, and low power consumption.

4. Conclusion

A novel cyclic ADC with offset cancelling and improved RSD correction is designed and manufactured in this work. The structure has the advantages of simple circuit configuration, moderate resolution with small chip area and low power dissipation. And it can tolerate high levels of comparator's offset errors and switched capacitor mismatch errors. Simulation and experimental results indicate a potential superiority of implementing the ADC architecture for applications in low power and intense integrated systems.

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