A 10-bit 80-MS/s opamp-sharing pipelined ADC with a switch-embedded dual-input MDAC*

Yin Rui(尹睿)[1,2], Liao Youchun(廖友春)[2], Zhang Wei(张卫)[1], and Tang Zhangwen(唐长文)[1,†]

[1]ASIC & System State Key Laboratory, Fudan University, Shanghai 201203, China
[2]Ratio Microelectronics Co., Ltd, Shanghai 200433, China

Abstract: A 10-bit 80-MS/s opamp-sharing pipelined ADC is implemented in a 0.18-μm CMOS. An opamp-sharing MDAC with a switch-embedded dual-input opamp is proposed to eliminate the non-resetting and successive-stage crosstalk problems observed in the conventional opamp-sharing technique. The ADC achieves a peak SNDR of 60.1 dB (ENOB = 9.69 bits) and a peak SFDR of 76 dB, while maintaining more than 9.6 ENOB for the full Nyquist input bandwidth. The core area of the ADC is 1.1 mm^2 and the chip consumes 28 mW with a 1.8 V power supply.

Key words: pipelined ADC; opamp-sharing; low power; switch-embedded; dual-input MDAC
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1. Introduction

Applications used in many electronic systems, such as video decoder and a high-speed wire line and wireless communication, require high-resolution low-power Nyquist-rate analog-to-digital converters (ADCs). The specifications of conversion rates higher than 50 MSample/s and signal-to-noise-and-distortion ratio (SNDR) in the range of 50–60 dB are usually required. To meet the applications of the integration of on-chip ADCs in the analog front-end with digital signal processors, low-power ADCs are much preferred. In addition, for the increasingly popular portable amusement, low power consumption is even more crucial for extending the duration of the system powered by a battery. Among many ADC architectures, the pipelined ADC architecture has commonly been employed to optimize speed, resolution, power dissipation and chip area, and has proved to be very efficient in meeting these requirements of high speed, high resolution, and low power consumption. The efficiency mainly depends on the "pipeline" operation of the ADC stages. Each stage processes data from the previous stage as soon as its output is passed to the next stage for sampling. This means that the pipelined ADC can achieve one conversion in each clock cycle. The most efficient method that has been utilized to obtain significant power saving is opamp sharing between multiplying digital-to-analogue converter (MDAC) stages in pipelined ADCs[1−5]. That is because the signal amplification in each MDAC stage is in alternate phases, so the operational transconductance amplifier (OTA) only works in a half clock cycle. Therefore, half of the opamps can be removed, leading to nearly 50% power reduction. However, the conventional opamp-sharing MDAC has the issues of non-resetting and successive stage crosstalk. To overcome these problems, this paper proposes an opamp-sharing pipelined ADC utilizing a switch-embedded dual-input MDAC that achieves a very high accuracy.

2. Conventional opamp-sharing MDAC

Although opamp sharing technology can save nearly half of the power consumption, it is achieved at the cost of resolution reduction, since the conventional opamp-sharing ADC has two serious problems. First, because the opamp input summing node is never reset, every input sample is affected by the error voltage stored on the input capacitor due to the previous sample. Thus it suffers from the memory effect, which can be considered as a signal-dependent OTA offset[1]. To avoid memory effects, the OTA inputs can be reset using a short duration third phase. However, this would reduce the time available for MDAC stage output settling. Second, there is a potential crosstalk path between two successive stages caused by the parasitic capacitors of switches, which are used to implement opamp sharing. The conventional opamp-sharing MDAC with parasitic capacitance is shown in Fig. 1. The signals in the current and successive stages, which appear at input nodes of the shared opamp, will influence each other through the crosstalk path. In addition, the opamp-sharing switches also introduce charge injection and signal-dependent resistance. These factors degrade both the linearity and the signal-to-noise-ratio (SNR).

To alleviate the non-resetting problem, the feedback signal polarity inverting (FSPI) is used to alternate the signal polarity, but it can only reduce the opamp offset by 2/3[2]. To break the crosstalk path, isolation switches are added to tie the parasitic capacitance to ground in the sample phase, the SNDR is improved only by 1–2 dB, but the added switches increase the series resistance and the charge injection[3]. Although opamp current reuse can solve the problems of non-resetting and crosstalk path by using both NMOS and PMOS input differ-

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† Corresponding author. Email: zwtang@fudan.edu.cn
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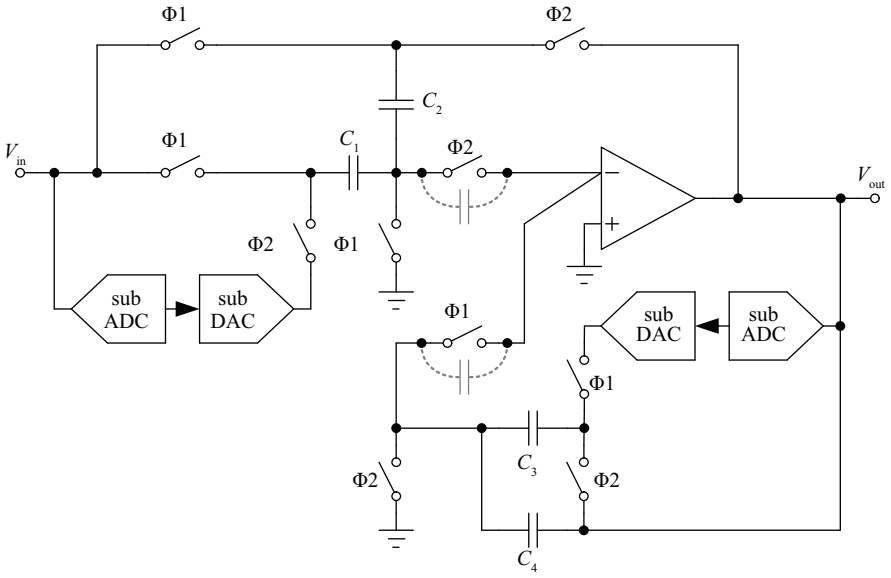


Fig. 1. Conventional opamp-sharing MDAC.

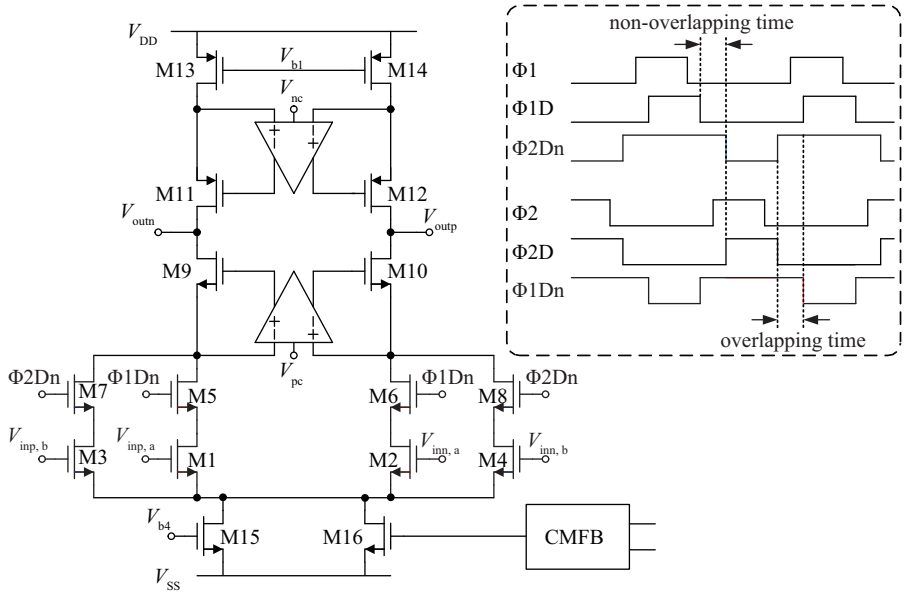


Fig. 2. Proposed two-input-differential-pair gain-boosting telescopic amplifier with clock timing.

ential pairs in shared opamps, the capacitive level shifter increases the design complexity and the PMOS input differential pair decreases the power efficiency[4]. In Ref. [5], the OTA employs dual-NMOS input differential pairs but needs two different common-mode input voltages for resetting. This methodology is restricted to telescopic cascode OTAs, which have most power efficiency and result in loss of output swing. The adding switch also reduced the OTA DC gain A_{OL} and GBW in $\Phi 2$ due to the on-resistance of the switches.

3. Proposed ADC with dual-input MDAC

To get rid of the problems of non-resetting and successive stage crosstalk, this paper proposes an opamp-sharing pipelined ADC using a switch-embedded MDAC with dual NMOS differential input pairs current-reuse OTA controlled by two-phase overlapping clocks.

3.1. Switch-embedded OTA

The topology of the proposed switch-embedded gain-boosting telescopic OTA with dual NMOS differential input pairs is shown in Fig. 2. Each input transistor (M1–M4) is connected with an embedded NMOS switch (M5–M8) in series. The switch is on when its corresponding control signal (i.e., Φ1Dn and Φ2Dn) is high, and is off when the control signal is low. To achieve a wide swing, a stable high-swing bias circuit is employed for the proposed gain-boosting telescopic amplifier, as shown in Fig. 3. To match the switch transistors in the opamp, a corresponding NMOS switch is added with its gate connected to the VDD. The opamp achieves 1.6-Vpp differential signal swing from a 1.8-V power supply considering process, temperature and power supply variations. Because of the delicate biasing, the overdrive voltage of the NMOS switch transistors is constant, thus the R_{on} of each switch only has a

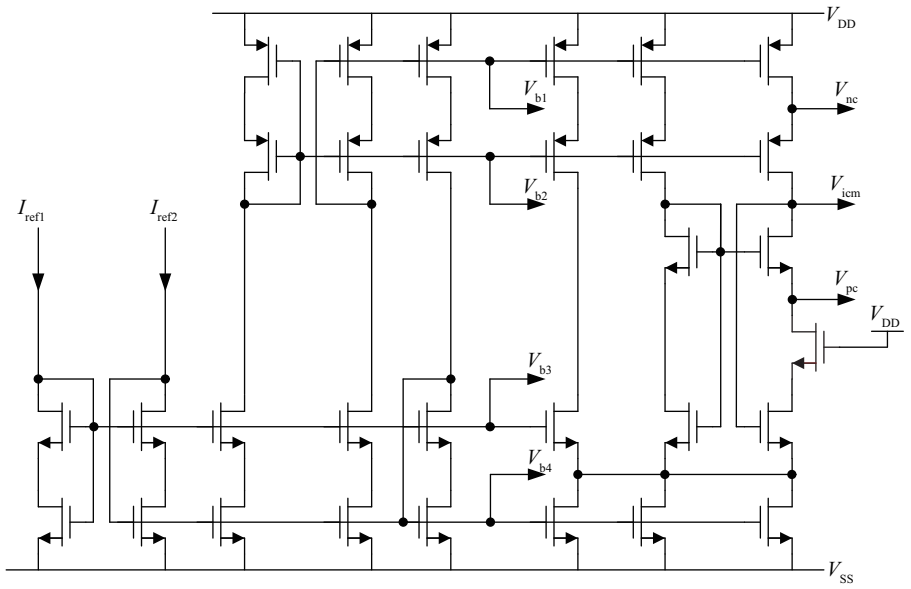


Fig. 3. Wide-swing bias circuit of the shared opamp.

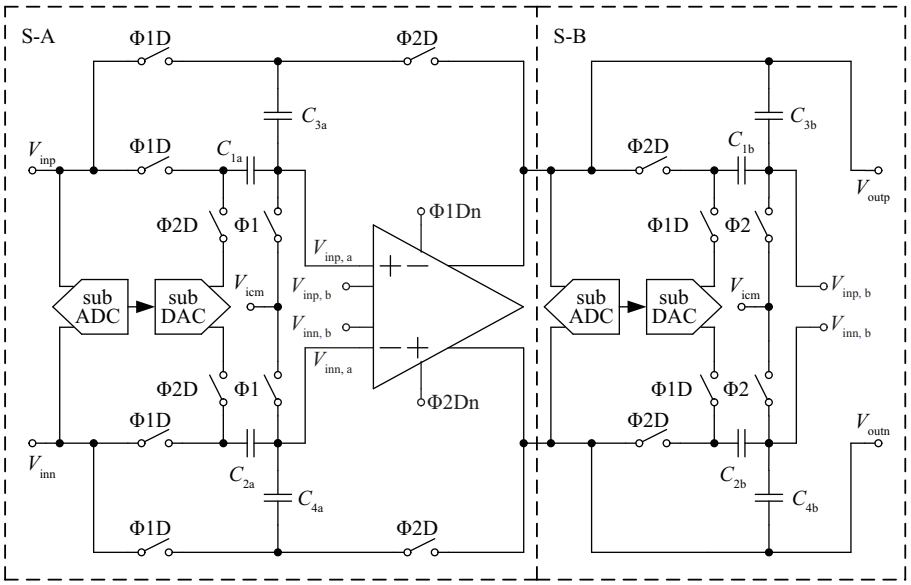


Fig. 4. Proposed opamp-sharing MDAC

small invariable resistance and will not affect the performance of the shared opamp.

3.2. Dual-input MDAC

The proposed 1.5-bit opamp-sharing MDAC using the switch-embedded amplifier is shown in Fig. 4. When Φ1 is high, both $V_{inp, a}$ and $V_{inn, a}$ are connected to the common-mode input voltage V_{icm} for resetting. When Φ1D is high, the sampling switches are on and C_{1a} and C_{2a} sample the input signal for stage-A while the opamp is working on holding mode for stage-B. At the end of the sample process, Φ1 turns to low before Φ1D, which is so called "bottom plate sampling". At the moment after the bottom plate sampling switch is completely off and the previous signal is still holding, the sub-ADC compares the result, passes the 2-bit digital codes to the sub-DAC and the digital error correction module. During the overlapping period of Φ1Dn and Φ2Dn, the opamp is working on dual-input-on mode. During this time, both pairs of input are active and have a half current, but are still in saturation. When Φ2D is high, the signal pathway is on. Meanwhile, $V_{inp, b}$ and $V_{inn, b}$ are disabled since Φ2Dn goes low, $V_{inp, a}$ and $V_{inn, a}$ are the only active inputs and the opamp is working on holding mode for stage-A.

Since both input pairs are reset to a common-mode input voltage alternately, the memory effect is completely eliminated without needing any additional clock phase. Furthermore, the opamp-sharing switches are embedded into the opamp instead of in series between the sampling capacitors and the opamp inputs, therefore the crosstalk path is avoided. In addition, since the opamp-sharing switches do not connect directly to the opamp input transistors, the charge injection and the signal-dependent resistance do not exist for the same reason.

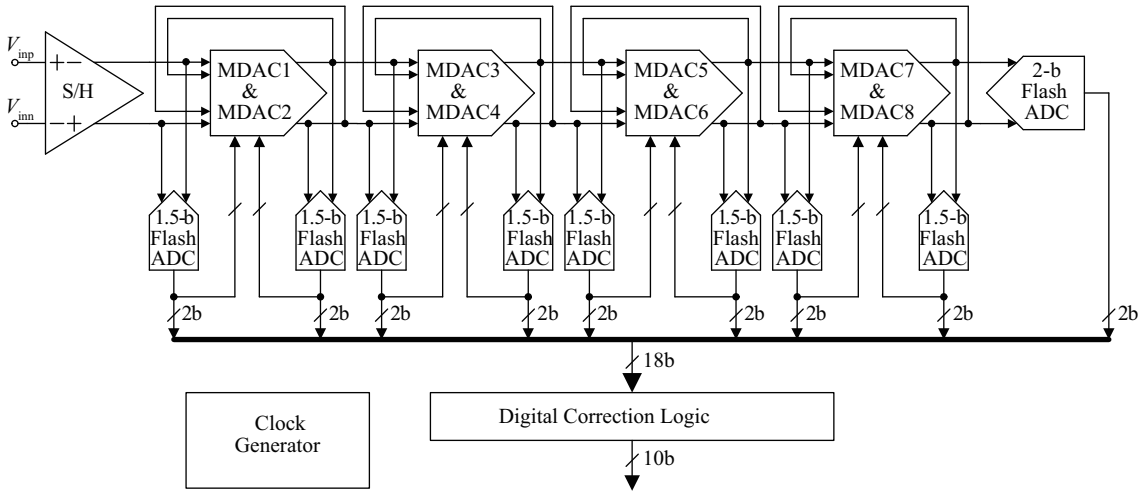
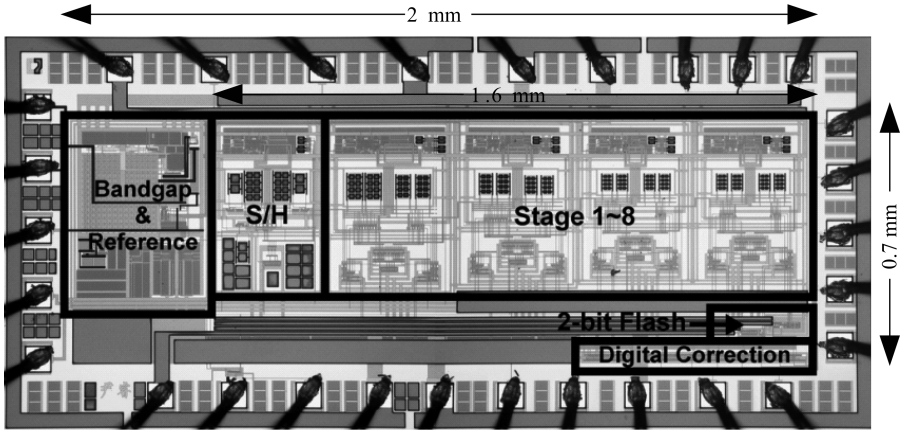


Fig. 5. Block diagram of the proposed pipelined ADC architecture.



Technology	0.18-μm CMOS	ENOB	9.69 bit @ 8 MHz Input
Resolution	10 bit		9.63 bit @ 39.5 MHz Input
Conversion rate	80 MS/s		9.64 bit @ 60 MHz Input
Input range	1.6 Vpp, diff	SFDR	76.0 dB @ 39.5 MHz Input
Supply voltage	1.8 V	Peak DNL	+0.37/–0.23 LSB
Power	32.4 mW (Core : 28 mW)	Peak INL	+0.53/–0.87 LSB
Active area	1.4 mm^2 (Core : 1.1 mm^2)	FOM	0.42 pJ/step

Fig. 6. Die micrograph and performance summary.

3.3. Timing consideration

The two-phase non-overlapping clock is always used in a pipelined ADC but is not suitable for controlling the opamp-sharing switches in the proposed OTA. If the non-overlapping clocks Φ1D and Φ2D are used, during the non-overlapping period, both pairs of opamp input transistors will be disabled, so there is no current path to the ground for PMOS transistor branches (M11–M14). The output voltages of the shared opamp will shift to a much higher level above the common output voltage during this period. In the worst case, PMOS transistors may enter into the linear region and the holding phase of MDAC stages would waste some time in the large-signal slew-rate. Therefore, the proposed opamp uses two-phase overlapping clocks (Φ1Dn and Φ2Dn) to avoid this problem. Since Φ1Dn and Φ2Dn are already used for CMOS switches, no additional clock phase is needed. The use of an overlapping working scheme will not affect the fidelity of signal transfer, settling or the quantization process. On the one hand, during the overlapping period, the shared opamp has not been working for signal settling until Φ1D/Φ2D is high. Signal transfer and settling will not be affected because there is no charge leakage path and two input differential pairs will not affect each other. Further, the opamp input transistors in saturation region in the overlapping period can improve the settling time. On the other hand, the comparing operation has already achieved at a moment between the falling edges of Φ1 and Φ1D, so the overlapping working has no adverse effect on the quantization process.

3.4. ADC architecture

A common pipelined ADC configuration is used in this work, as shown in Fig. 5. The ADC is composed of an S/H circuit, eight 1.5-bit MDACs using four shared opamps, and a 2-bit flash ADC as the last stage. The ADC also has an on-chip bandgap reference, a distributed clock generation circuit,

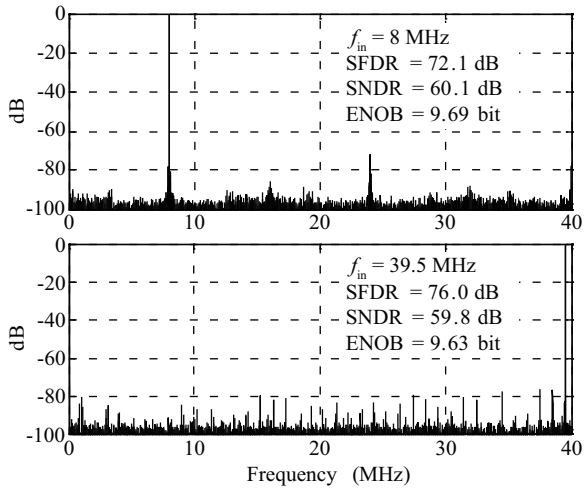


Fig. 7. Measured FFT plot at a sample frequency of 80 MHz with input signals of 8 MHz and 39.5 MHz.

a digital error correction circuit and voltage buffers.

The input-sampling switch in the S/H circuit is bootstrapped, while the bottom-sampling switch is a symmetrical gate-bootstrapping one to increase linearity[3]. Capacitor sizes are carefully chosen to meet matching and noise requirements.

By using the technique of redundant-signed-digit (RSD) correction, which allows a large offset error for a simple dynamic latch-type comparator without static power consumption, the power consumption could be reduced further. The comparators in all flash ADCs employ a high-speed mismatch-insensitive dynamic latch-type circuit without any pre-amplifier.

4. Measurement results

The ADC is fabricated in a 0.18-μm CMOS process with a core die size of 1.1 mm^2. To maintain the characteristics of full Nyquist input bandwidth, the differential input and output signal paths are carefully designed and simulated on the circuit and layout-level. For better isolation, analog and digital were placed far from each other with guard rings, respectively. MIM capacitors were also well matched. The die micrograph and performance summary are shown in Fig. 6. The chip consumes 28 mW from a 1.8 V power supply at 80 MSample/s, not including the bandgap reference and voltage buffers. Figure 7 shows the FFT plot for the input frequencies of 8 MHz and 39.5 MHz at a 80 MHz sample rate. The spurious free dynamic range (SFDR), SNR and effective number of bits (ENOB) versus input frequency are shown in Fig. 8. The ADC achieves a peak ENOB of 9.69 bits and a peak SFDR of 76 dB, while maintaining more than 9.6 ENOB for the full Nyquist input bandwidth. When the input frequency is close to sample rate, the ADC still maintains 9.47 ENOB. Figure 8 also provides SFDR, SNR and ENOB versus sample frequency at an input frequency of 8 MHz. When the sample rate rises to 100 MHz, there is still 9.1 ENOB. The measured SNDR and SFDR are better than other recently published works of 10-bit pipelined ADCs[2−5], as shown in Fig. 9. Figure 10 shows the differential nonlinearity (DNL) of +0.37/–0.23 LSB and the integral nonlinearity (INL) of +0.53/–0.87 LSB. Using a figure-of-merit

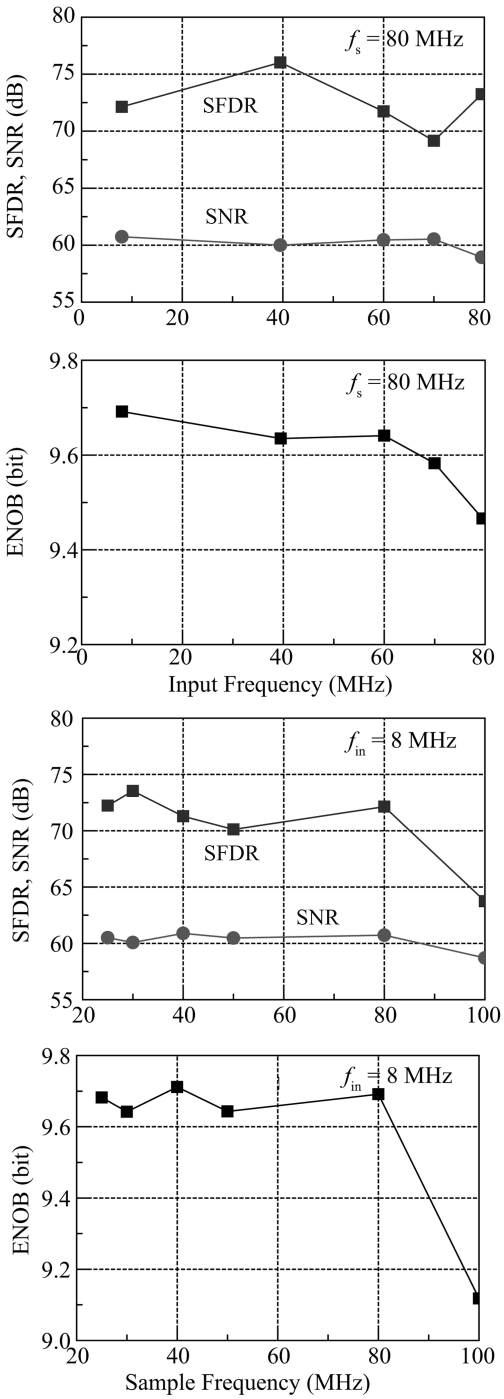
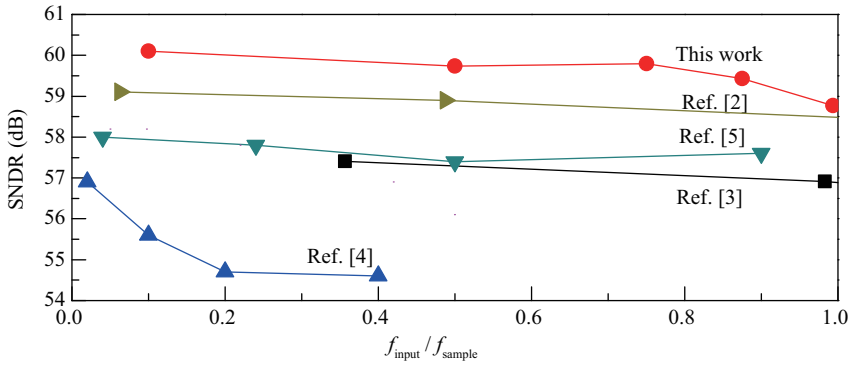


Fig. 8. SFDR, SNR and ENOB versus input frequency and sample frequency.

of Power/($2^{ENOB} \times f_s$), the ADC achieves 0.42 pJ/conversion-step.

5. Conclusion

This paper describes a 10-bit 80-MS/s pipelined ADC using the proposed switch-embedded opamp-sharing MDAC based on a dual NMOS input pairs current-reuse opamp. Compared with a traditional opamp-sharing ADC, the proposed opamp-sharing method achieved an improved accuracy by eliminating the memory effect and crosstalk path without any additional power, area consumption and clock phase. The mea-



Ref.	Process	V_{DD} (V)	f_s (MS/s)	FOM (pJ/step)	SFDR (dB)	ENOB (bit)
Ref. [2]	0.18 μm DGO CMOS	3	80	1.21	74	9.47
Ref. [3]	0.18 μm CMOS	1.8	30	1.19	69	9.24
Ref. [4]	0.18 μm CMOS	1.8	50	0.61	70	9.2
Ref. [5]	0.18 μm CMOS	1.8	50	0.29	74	9.3
This work	0.18 μm CMOS	1.8	80	0.42	76	9.69

Fig. 9. SNDR and other performance comparisons with some recently published works.

sured SNDR and SFDR are 60.1 dB and 76 dB, respectively. This technique is also suitable for other ADC architectures, such as multi-bit per stage and multi-channel for achieving high power efficient and high accuracy applications.

References

[1] Nagaraj K, Fetterman H S, Anidjar J, et al. A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers. IEEE J Solid-State Circuits, 1997, 32(3): 312

[2] Min B, Kim P, Boisvert D, et al. A 69 mW 10 b 80 MS/s pipelined CMOS ADC. ISSCC Digest of Technical Papers, 2003: 324

[3] Li J, Zeng X, Xie L, et al. A 1.8-V 22-mW 10-bit 30-MS/s pipelined CMOS ADC for low-power subsampling applications. IEEE J Solid-State Circuits, 2008, 43(2): 321

[4] Ryu S, Song B, Bacrania K. A 10-bit 50-MS/s pipelined ADC with opamp current reuse. IEEE J Solid-State Circuits, 2007, 42(3): 475

[5] Chandrashekar K, Bakkaloglu B. A 10 b 50 MS/s opamp-sharing pipeline A/D with current-reuse OTAs. IEEE CICC, 2009: 263