A 1.0 V differential VCO in 0.13 μm CMOS technology*

Cao Shengguo(曹圣国), Han Kefeng(韩科锋), Tan Xi(谈熙)†, Yan Na(闫娜), and Min Hao(闵昊)

State Key Laboratory of ASIC & System, Fudan University, Shanghai, 201203, China

Abstract: A differential complementary LC voltage controlled oscillator (VCO) with high Q on-chip inductor is presented. The parallel resonator of the VCO consists of inversion-mode MOS (I-MOS) capacitors and an on-chip inductor. The resonator Q factor is mainly limited by the on-chip inductor. It is optimized by designing a single turn inductor that has a simulated Q factor of about 35 at 6 GHz. The proposed VCO is implemented in the SMIC 0.13 μm 1P8M MMRF CMOS process, and the chip area is 1.0×0.8 mm^2. The free-running frequency is from 5.73 to 6.35 GHz. When oscillating at 6.35 GHz, the current consumption is 2.55 mA from a supply voltage of 1.0 V and the measured phase noise at 1 MHz offset is –120.14 dBc/Hz. The figure of merit of the proposed VCO is –192.13 dBc/Hz.

Key words: differential voltage controlled oscillator; CMOS; inversion-mode MOS; capacitors; on-chip inductors
DOI: 10.1088/1674-4926/32/2/025010 **EEACC:** 1230B

1. Introduction

The voltage controlled oscillator (VCO) is one of the most crucial building blocks in radio frequency transceivers. The design of low noise VCOs is challenging, with low supply voltage and noisy active devices in modern CMOS processes. According to previous works[1–5], there are many noise sources in differential VCOs. In order to suppress phase noise, the VCO should have fewer noise sources, lower voltage-to-frequency gain and a higher-Q resonator. In this paper, we present a CMOS differential LC VCO, which has no other active components except for two pairs of cross-coupled transistors. The Q factor of the resonator is optimized by designing a single turn inductor with a simulated Q factor of about 35 at 6 GHz. With the relatively high-Q resonator, the proposed VCO can operate at a 1.0 V supply with a figure of merit (FOM) of –192.13 dBc/Hz.

2. Circuit design and resonator optimization

The schematic of the proposed differential LC VCO is shown in Fig. 1 which is a complementary VCO with cross-coupled PMOS and NMOS transistors. A tail LC-tank resonated at the second harmonic is used to block the second harmonic. In the absence of a tail current source, the voltage headroom is released and the noise source is reduced. The LC-tank resonator is formed by I-MOS capacitors and a single turn differential inductor. The switched capacitors for subfrequency bands are inversion mode PMOS capacitors, and varactors are inversion mode NMOS capacitors. In order to program the VCO gain, the I-MOS varactors are controlled by switches. When a varactor is switched on, its equivalent capacitance is controlled through the transmission gates in series[6].

When the transistor is working in inversion mode, the channel resistor of the I-MOS capacitor can be calculated[7]. So the inversion channel sheet resistance $R_{\mathrm{ch,w}}$ can be deduced to

$$R_{\mathrm{ch,w}} = \frac{1}{\mu C_{\mathrm{ox}}(|V_{\mathrm{GS}}| - |V_{\mathrm{T}}|)}, \tag{1}$$

where μ is the carrier mobility and C_{ox} is the unit area capacitor of the gate oxide. The Q factor of the I-MOS capacitor can be expressed as[8]

$$\begin{aligned} Q &= \frac{1}{\omega C R_{\mathrm{s}}} = \frac{1}{\dfrac{\omega C_{\mathrm{ox}}}{12}(R_{\mathrm{ch,w}} L^2 + R_{\mathrm{poly,w}} W^2)} \\ &= \frac{12}{\omega C_{\mathrm{ox}} R_{\mathrm{ch,w}} L^2 + \omega C_{\mathrm{ox}} R_{\mathrm{poly,w}} W^2}. \end{aligned} \tag{2}$$

where $R_{\mathrm{poly,w}}$ is the sheet resistance of gate, and ω is the resonation frequency. W and L are the width and length of the transistor. The channel resistor dominates the total series resistance. From Eqs. (1)–(2), the Q factor approximates to

$$Q = \frac{12}{\omega C_{\mathrm{ox}} R_{\mathrm{ch,w}} L^2} = \frac{12\mu(|V_{\mathrm{GS}}| - |V_{\mathrm{T}}|)}{\omega L^2}. \tag{3}$$

Equation (3) shows that the Q factor of the proper channel length I-MOS capacitors with sufficient overdrive voltage will be high enough at the frequency below 10 GHz, e.g., minimum length PMOS capacitors can have a Q factor higher than 100. The inversion PMOS switched capacitor sources/drains are biased at the power supply higher than the VCO supply when switched on to have sufficient overdriven voltage over the entire oscillating cycle. The varactors are implemented by native NMOS transistors. All of the I-MOS capacitors, including switched capacitors and varactors, have a high Q factor. Additionally, the proper biased switched I-MOS capacitors suppress AM to FM noise conversion through their nonlinearity.

The inductor in the parallel LC-tank resonator is a single turn spiral differential inductor. In physical analysis, the simplified double-π inductor model[9] is used as shown Fig. 2.

* Project supported by the Important National Science and Technology Specific Projects of China (No. 2009ZX01031-003-002) and the National High Technology Research and Development Program of China (No. 2009AA011605).
† Corresponding author. Email: tanxi@fudan.edu.cn
Received 13 August 2010, revised manuscript received 26 September 2010 © 2011 Chinese Institute of Electronics

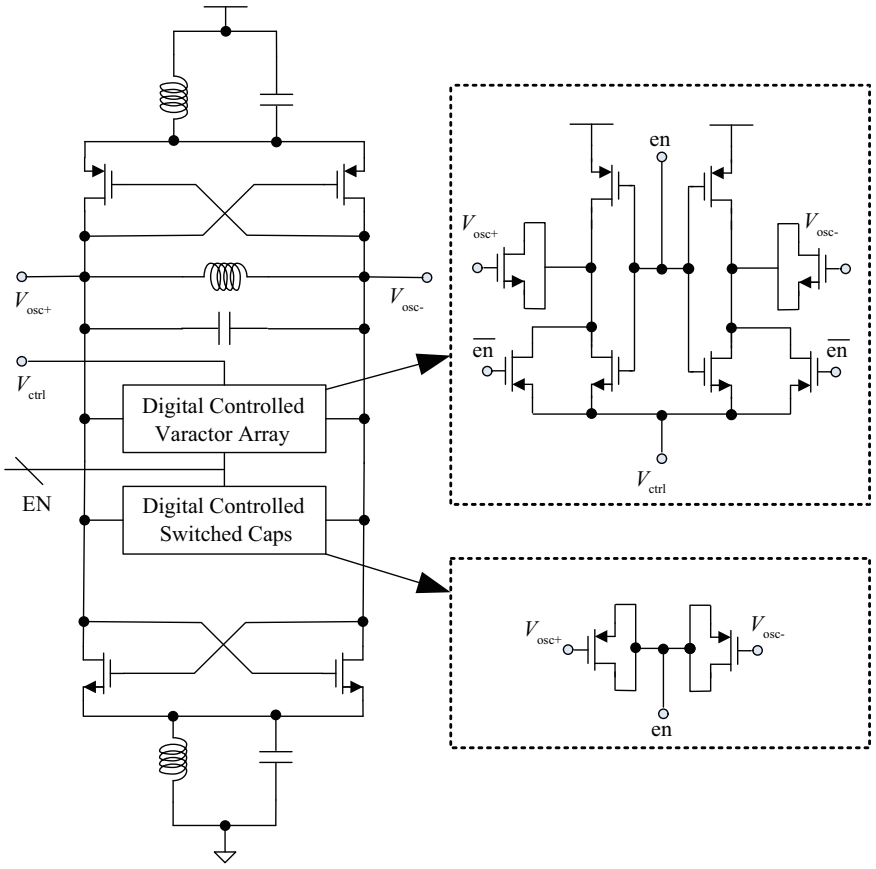

Fig. 1. Circuit diagram of the proposed differential LC VCO.

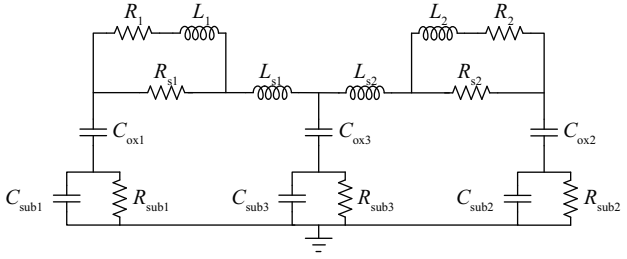

Fig. 2. Simplified double-π equivalent circuit of a single turn spiral inductor.

The series R_{si} and L_{si} ($i = 1, 2$) characterize the uniformly distributed DC current inside the conductor. The additional R_i and L_i ladder is used to capture the different current density caused by the skin effect when the frequency goes up. The substrate network can be modeled by C_{oxi}, C_{subi} and R_{subi}, with C_{oxi} representing the metal–oxide capacitance, and C_{subi} and R_{subi} representing the substrate capacitance and resistance, respectively. The components representing the coupling capacitance between adjacent tracks and the overlap capacitance between the spiral and underpass metal are negligible, because it is a single turn inductor without any crossover interconnections. The inductor is fully symmetrical, and then relationships of the components in the equivalent circuit are shown in Eqs. (4) and (5). The series branch partition:

$$\frac{R_1}{R_2} = \frac{R_{s1}}{R_{s2}} = \frac{L_1}{L_2} = \frac{L_{s1}}{R_{s2}} = 1. \tag{4}$$

The oxide capacitance and substrate branch partition:

$$\frac{C_{ox1}}{C_{ox2}} = \frac{R_{sub1}}{R_{sub2}} = \frac{C_{sub1}}{C_{sub2}} = 1. \tag{5}$$

The summation rules for the middle branch $C_{ox3} = C_{ox1} + C_{ox2}, C_{sub3} = C_{sub1} + C_{sub2}, 1/R_{sub3} = 1/R_{sub1} + 1/R_{sub2}$[9] will be accurate.

Single turn inductors can have superior quality factors because the ohmic loss in the top metal trace is less and the proximity effect leading to Q factor degradation at high frequency is ruled out. The eddy current in the relatively high resistivity substrate (10 Ω·cm) is not the dominating substrate loss compared to the substrate ohmic losses from displacement currents conducted through turn-to-substrate capacitors C_{oxi}[10]. The inductor suffers significant power dissipation mechanisms, including ohmic losses in the substrate and interconnections, and the skin effect at high frequency. The skin effect loss will be reduced when the trace width increases[11], but the substrate ohmic losses will be increased under the same conditions. It will be seen directly after parameter extraction and mapping that R_i, R_{si}, R_{subi} and L_i will decrease while C_{oxi} and C_{subi} will increase. The inductor Q factor can be optimized by taking tradeoff of the skin effect loss, DC ohmic loss and substrate ohmic losses into consideration. The optimized single turn differential spiral inductor has a simulated Q factor of about 35 at 6 GHz and its self resonation frequency is 48 GHz in the Agilent Momentum environment. The results are shown in Fig. 3.

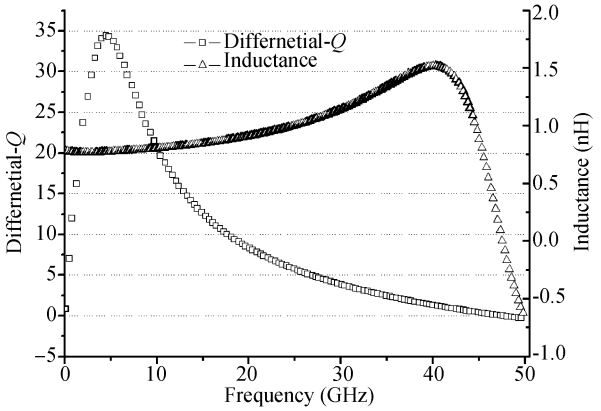

Fig. 3. Simulated Q factor and inductance of the on-chip inductor.

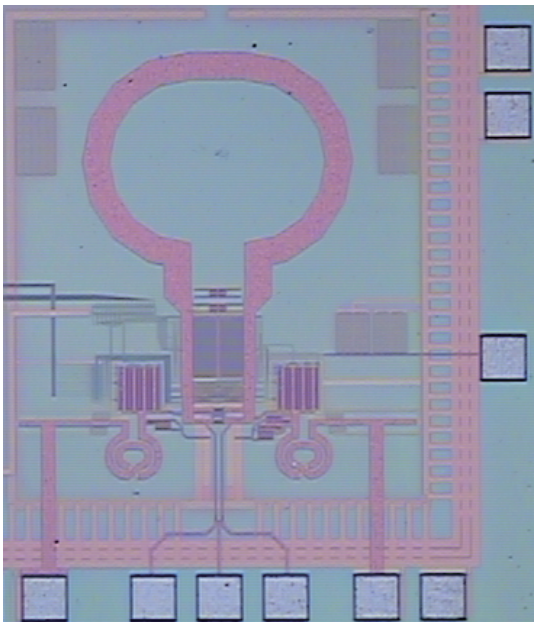

Fig. 4. Chip photograph of proposed differential LC VCO.

3. Measurement

The VCO was designed and fabricated in the SMIC 0.13 μm 1P8M MMRF CMOS technology. Two single-ended RF open sources on chip output buffers are used to drive the test instrument. Figure 4 shows the micrograph of the proposed VCO, which has a chip area of 1.0×0.8 mm^2, including pads. The VCO chip is supplied by Agilent E3631A at a voltage of 1.0 V. The phase noise of the proposed VCO is measured by an Agilent E4440A spectrum analyzer. Figure 5 illustrates the measured phase noise at 6.35 GHz with current consumption of 2.55 mA. The figure of merit (FOM) is defined as

$$\mathrm{FOM} = L\{\Delta\omega\} + 10\lg\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}} - 20\lg\frac{\omega_0}{\Delta\omega}, \qquad (6)$$

where ω_0 is the oscillating frequency, $\Delta\omega$ is the offset frequency, $L\{\Delta\omega\}$ is the phase noise at $\Delta\omega$ and PDC is the DC power consumption of the oscillator. The phase noise is –120.14 dBc/Hz at 1 MHz offset from the oscillation frequency of 6.35 GHz. The FOM of this proposed differential VCO is –192.13 dBc/Hz at 1 MHz offset. The measured oscillating frequency can be tuned from 5.73 to 6.35 GHz, and the VCO gain (K_{vco}) can be programmed from 2 to 200 MHz/V. This feature is very useful for changing the bandwidth when implemented in the phase lock loop (PLL). Table 1 lists the comparison of differential VCO performance. The proposed VCO has better performance than[12–16].

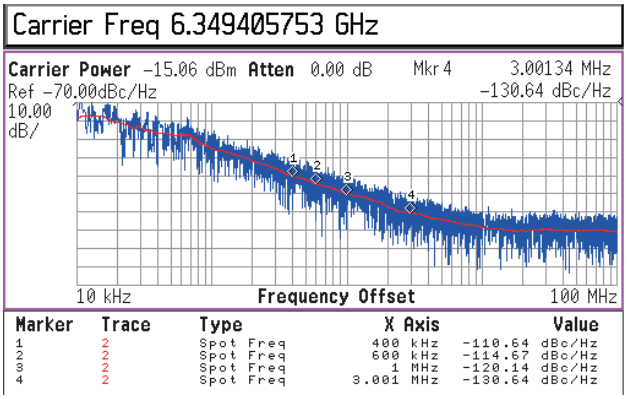

Fig. 5. Measured phase noise of proposed differential LC VCO.

Table 1. VCO performance comparison.

Ref.	Tech. (μm)	Freq. (GHz)	V_{dd} (V)	P_{DC} (mW)	Phase noise @ 1 MHz (dBc/Hz)	FOM
[12]	0.18	5.2	1.8	9.7	–113.7	–180.0
[13]	0.18	5.46	1.8	6.4	–120.2	–186.9
[14]	0.18	5.6	1.2	2.4	–119.1	–190.3
[15]	0.13	2.17	1.2	5.92	–119.1	–189.5
[16]	0.18	5.6	1.4	6.44	–122.7	–189.6
This	0.13	6.35	1.0	2.55	–120.1	–192.1

4. Conclusion

A differential complementary LC VCO has been proposed. The VCO has a parallel LC resonator constituted by I-MOS capacitors and a single turn differential inductor. The Q factor of the resonator is mainly limited by the on-chip inductor. The inductor Q factor is optimized by taking advantage of its single turn geometry and taking the tradeoff of losses into consideration. The simulated Q factor of the single turn spiral inductor is about 35 at 6 GHz. Also, the complementary structure without current source reduces the noise source and the tail tanks resonated at second harmonic block the second harmonic which degrade the Q factor. The 5.73 GHz to 6.35 GHz tuning range VCO has been implemented in the SMIC 0.13 μm 1P8M CMOS technology. The current consumption is 2.55 mA from a 1.0 V supply at 6.35 GHz. The measured phase noise at 1 MHz offset is –120.14 dBc/Hz and the FOM of the proposed VCO is –192.13 dBc/Hz.

References

[1] Wu Y, Aparin V. A monolithic low phase noise 1.7 GHz CMOS VCO for zero-IF cellular CDMA receivers. IEEE ISSCC Tech Dig, 2004: 396

[2] Ismail A, Abidi A. CMOS differential LC oscillator with suppressed up-converted flicker noise. IEEE ISSCC Tech Dig, 2003:

98
[3] Hajimiri A, Lee T. Design issues in CMOS differential LC oscillators. IEEE J Solid-State Circuits, 1999, 34(5): 717
[4] Rael J, Abidi A. Physical processes of phase noise in differential LC oscillator. Proc IEEE CICC, 2000: 569
[5] Hajimiri A, Lee T. Phase noise in CMOS differential LC oscillators. Proc Symp VLSI Circuits, 1998: 48
[6] Lu L, Chen J, Yuan L, et al. An 18-mW 1.175–2-GHz frequency synthesizer with constant bandwidth for DVB-T tuners. IEEE Trans Microw Theory Tech, 2009, 57(4): 928
[7] Andreani P, Mattisson S. On the use of MOS varactors in RF VCOs. IEEE J Solid-State Circuits, 2000, 35(6): 717
[8] Hung C M, Ho Y C, Wu I C, et al. High-Q capacitors implemented in a CMOS process for low-power wireless applications. IEEE Trans Microw Theory Tech, 1998, 46(5): 505
[9] Huang F, Lu J, Jiang N, et al. Frequency-independent asymmetric double-Π equivalent circuit for on-chip spiral inductors: physics-based modeling and parameter extraction. IEEE J Solid-State Circuits, 2006, 41(10): 2272
[10] Kuhn W B, Ibrahim N M. Analysis of current crowding effects in multiturn spiral inductors. IEEE Trans Microw Theory Tech, 2001, 49(1): 31
[11] Hasegawa H, Furukawa M, Yanai H. Properties of microstrip line on Si–SiO_2 system. IEEE Trans Microw Theory Tech, 1971, 19(11): 869
[12] Moon Y J, Roh Y S, Jeong C Y, et al. A 4.39–5.26 GHz LC-tank CMOS voltage-controlled oscillator with small VCO-gain variation. IEEE Microw Wireless Compon Lett, 2009, 19(8): 524
[13] Hou J A, Wang Y H. A 5 GHz differential colpitts CMOS VCO using the bottom PMOS cross-coupled current source. IEEE Microw Wireless Compon Lett, 2009, 19(6): 401
[14] Jang S L, Liu C C, Wu C Y, et al. A 5.6 GHz low power balanced VCO in 0.18 μm CMOS. IEEE Microw Wireless Compon Lett, 2009, 19(4): 233
[15] Kim H, Ryu S, Chung Y, et al. A low phase-noise CMOS VCO with harmonic tuned LC tank. IEEE Trans Microw Theory Tech, 2006, 54(7): 2917
[16] Park J, Park J, Choi Y, et al. A fully-differential complementary Hartley VCO in 0.18 μm CMOS technology. IEEE Microw Wireless Compon Lett, 2010, 20(2): 91