Numerical analysis of the self-heating effect in SGOI with a double step buried oxide*

Li Bin(李斌)†, Liu Hongxia(刘红侠), Li Jin(李劲), Yuan Bo(袁博), and Cao Lei(曹磊)

Key Laboratory for Wide Band Gap Semiconductor Materials and Devices of Education, School of Microelectronics, Xidian University, Xi'an 710071, China

Abstract: To reduce the self-heating effect of strained Si grown on relaxed SiGe-on-insulator (SGOI) n-type metal–oxide–semiconductor field-effect transistors (nMOSFETs), this paper proposes a novel device called double step buried oxide (BOX) SGOI, investigates its electrical and thermal characteristics, and analyzes the effect of self-heating on its electrical parameters. During the simulation of the device, a low field mobility model for strained Si MOSFETs is established and reduced thermal conductivity resulting from phonon boundary scattering is considered. A comparative study of SGOI nMOSFETs with different BOX thicknesses under channel and different channel strains has been performed. By reducing moderately the BOX thickness under the channel, the channel temperature caused by the self-heating effect can be effectively reduced. Moreover, mobility degradation, off state current and a short-channel effect such as drain induced barrier lowering can be well suppressed. Therefore, SGOI MOSFETs with a thinner BOX under the channel can improve the overall performance and long-term reliability efficiently.

Key words: self-heating effect; step BOX; SGOI; mobility model; numerical analysis

DOI: 10.1088/1674-4926/32/3/034001 **PACC:** 7340Q; 7300; 7360H

1. Introduction

Historically, scaling down becomes an effective solution to improve the performance of Si-based MOSFETs. However, in the nanoscale regime, some unexpected phenomenon can appear, such as gate leakage current, an excessive off state current resulting from the short-channel effect, and degradation of mobility due to the increasing channel-doping density[1, 2]. The SGOI MOSFET is a leading candidate that combines the advantages of silicon-on-insulator (SOI) MOSFETs and bulk strained silicon MOSFETs, exhibiting a steep subthreshold slope, low junction current, improved mobility and reduced threshold-voltage variation due to impurity concentration[3−6].

However, one of the major issues related to SGOI MOSFETs is prone to the self-heating effect[7]. In Refs. [8, 9], experimental data show that the thermal conductivity of a silicon film with a thickness of less than 300 nm is less than that of bulk silicon (1.45 W/(cm·K)) due to phonon boundary scattering. The thermal conductivity of 10 nm silicon film varies from 0.14 to 0.2 W/(cm·K). And the thermal conductivities of SiGe alloy (0.05–0.1 W/(cm·K)) and SiO_2 (0.014 W/(cm·K)) upon the Si substrate are much smaller than bulk silicon thermal conductivity[9], leading to a large increase in temperature in the vicinity of the drain-body junction. This restricts the expansion of the application of SGOI MOSFETs to high temperature operation[10, 11].

In this work, numerical analysis of a gate length of 50 nm SGOI nMOSFETs with double step BOX under the channel is carried out using a device simulator called ISE TCAD[12]. A low field mobility model for a strained Si device has been established to account for the enhancement of mobility caused by channel strain. Moreover, we have taken the self-heating effect into account and incorporated reduced thermal conductivity caused by phonon boundary scattering in thin silicon film into TCAD for better accuracy. By reducing the BOX thickness under the channel, we investigate the effect of self-heating on various performance parameters of SGOI nMOSFETs.

2. Modeling

The cross-section view of SGOI nMOSFETs with a double step BOX under the channel is shown in Fig. 1. $T_{\text{mid-BOX}}$ is the

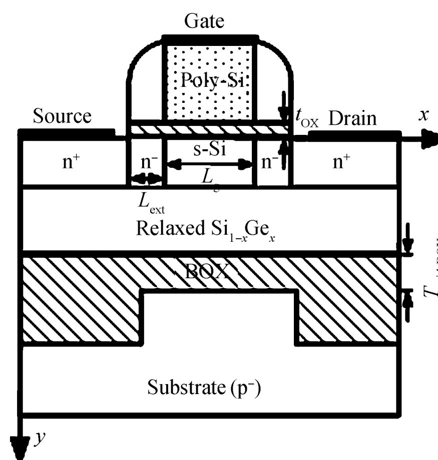

Fig. 1. Schematic cross-sectional view of SGOI nMOSFETs with a double step BOX.

* Project supported by the National Natural Science Foundation of China (Nos. 60976068, 60936005), the Cultivation Fund of the Key Scientific and Technical Innovation Project, Ministry of Education of China (No. 708083), and the Specialized Research Fund for the Doctoral Program of Higher Education, China (No. 200807010010).

† Corresponding author. Email: 13389232181@189.cn

Received 16 August 2010, revised manuscript received 10 November 2010 © 2011 Chinese Institute of Electronics

Table 1. Device structure parameters.

Device parameter	SGOI with double step BOX
N^+ source (S)/drain (D) doping	1×10^{20} cm^{-3}
N^- S/D extension (SDE) doping	5×10^{18} cm^{-3}
P^- channel doping	5×10^{17} cm^{-3}
N^+ poly-Si doping	1×10^{20} cm^{-3}
Gate length (L_g)	50 nm
Source/drain extension length (L_{ext})	100 nm
Gate oxide thickness (t_{ox})	4 nm
Buried layer ($T_{mid\text{-}BOX}$)	SiO_2 (10–100 nm)
P^- substrate doping	5×10^{16} cm^{-3}
Ge content in $Si_{1-x}Ge_x$	0–0.4

thickness of the BOX under the channel. Compared to conventional SGOI nMOSFETs, $T_{mid\text{-}BOX}$ ranges from 10 to 100 nm.

The detailed parameters for the simulated device are shown in Table 1.

To describe the electron transport properties in strained Si-base MOSFETs, a low-field carrier mobility model must be established. The models proposed by Lombardi[13] and Darwish[14] are suitable to describe carrier transport properties of Si-based devices. This is feasible by extending the mobility model of Si-based devices to strained Si devices. Therefore, the $C(x)$, $B(x)$, and $\delta(x)$ function of Ge content x in surface mobility models can be used to account for the improvement in phonon-limited mobility and surface roughness-limited mobility caused by strain. Originating from the mobility model of conventional Si MOSFETs, the surface acoustic phonon scattering caused carrier mobility for strained Si MOSFETs can be modeled as[14]

$$\mu_{ph} = \frac{B(x)}{E_\perp} + \frac{C(x)(N_i)^\tau}{E_\perp^{1/3}T'}, \tag{1}$$

where τ is the fitting parameter, N_i is the doping concentration in the channel region, and $E_\perp$ is the electric field normal to the semiconductor-insulator interface. $T' = (\frac{T}{300})^{1.75}$ and T is the lattice temperature. For strained Si nMOSFETs, electron mobility is enhanced dramatically as the Ge content x increases from 0 to 0.2. When the Ge content x increases from 0.2 to 0.3, improvement of the electron mobility becomes weak. The electron mobility remains unchanged as the Ge content x ranges from 0.3 to 0.4[11, 15]. The reason for this behavior is that the energy splitting of six fold degenerate valleys in the Si conduction band minimum is so great that almost all electrons are situated in the lowered two valleys[15]. Hence, the acoustic phonon scattering rate decreases no further. $B(x)$ and $C(x)$ are modeled to describe the behavior of strained Si nMOSFETs[16],

$$B(x) = B_0 \left\{ \frac{\alpha x}{\left[1 + \left(\frac{\alpha x}{0.999}\right)^\beta\right]^{\frac{1}{\beta}}} + 1 \right\}, \tag{2}$$

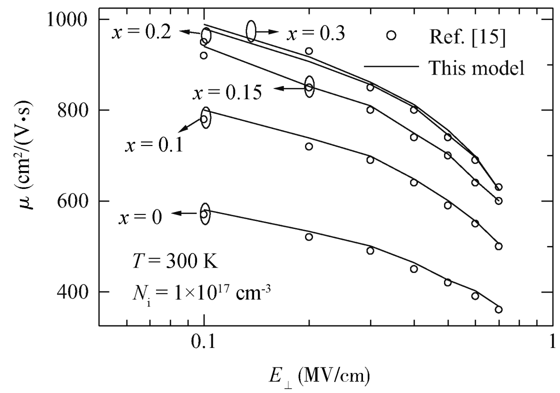

Fig. 2. Electron mobility versus vertical field for strained Si/$Si_{1-x}Ge_x$ nMOSFETs at room temperature. This model is shown in line. Data reported by Currier *el al*.[15] are shown in the hollow circle.

$$C(x) = C_0 \left\{ \frac{\alpha x}{\left[1 + \left(\frac{\alpha x}{0.999}\right)^\beta\right]^{\frac{1}{\beta}}} + 1 \right\}, \tag{3}$$

where B_0 and C_0 are the values with Ge content of 0, and x is the Ge content in the relaxed $Si_{1-x}Ge_x$ layer.

Similarly, the carrier mobility μ_{sr} corresponding to the surface roughness scattering in strained Si nMOSFETs is modeled as[14]

$$\mu_{sr} = \frac{\delta(x)}{E_\perp^{-\gamma}}, \tag{4}$$

where $\delta(x)$ is modeled as[16]

$$\delta(x) = \delta_0 \left\{ \frac{\alpha x}{\left[1 + \left(\frac{\alpha x}{0.999}\right)^\beta\right]^{\frac{1}{\beta}}} + 1 \right\}, \tag{5}$$

where δ_0 is the value with a Ge content of 0. The low field carrier mobility is approximated by the sum of the surface mobility and the bulk mobility μ_b according to Mathiessen's rule,

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_b} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}, \tag{6}$$

where bulk mobility μ_b employs the Masetti G model[17], which includes the doping-dependence mobility in a Si-based device. An optimized parameter value in phonon scattering-limited mobility μ_{ph} and surface roughness-limited mobility μ_{sr} can be obtained from Ref. [14]. The values of B_0 and C_0 are 3.61×10^7 cm/s and 1.7×10^4 cm/(V·s) separately. The parameter τ has a value of 0.0233, and γ has a value of 2.78. The value of δ_0 is 3.58×10^{18} cm^2/(V·s). Fitting parameters $\alpha = 5$ and $\beta = 25$ are extracted from the enhancement and saturation characteristic of strained Si nMOSFETs, respectively[15].

Table 2. Values of coefficients for thermal conductivity in various silicon films.

Silicon film	10 nm	50 nm
κ (W/(cm·K))	0.31	1.03
κ_b (W/cm)	-6.5×10^{-4}	5×10^{-7}
κ_c (W/cm)	-2.75×10^{-3}	-2.5×10^{-6}

Figure 2 shows the calculated electron mobility versus Currier's data[15] for various Ge content x for electrons. It agrees with the reference.

When studying heat transport in the device, a thermodynamic model is used to calculate the lattice temperature distribution in the simulated device. The simple expression of heat flow transport is modeled as[10]

$$C_s \frac{\partial T}{\partial t} = \nabla(\kappa_s \nabla T) + \boldsymbol{J} \cdot \boldsymbol{E}, \tag{7}$$

where T is the local lattice temperature, C_s is the lattice heat capacity, κ_s is the thermal conductivity, and $\boldsymbol{J} \cdot \boldsymbol{E}$ is the thermal generation. The thermal conductivity can be written as[8, 9]

$$\kappa_s = C_s \upsilon \Lambda_s / 3, \tag{8}$$

where Λ_s is phonon mean free path, and υ is the average phonon velocity. The mean free paths of phonon in the bulk silicon and $Si_{0.8}Ge_{0.2}$ at 300 K are approximately 300 nm and 11 nm, respectively[8]. When studying the heat transport in ultra thin body SOI, the thickness of thin silicon film is much smaller than the phonon mean free path in bulk silicon. Because of phonon boundary scattering, it results in nearly an order of magnitude reduction in the thermal conductivity of thin silicon film compared to the bulk silicon[8].

To obtain the temperature-dependent phonon boundary scattering, a model has been proposed by Liu *et al*.[18] to account for phonon boundary scattering in thin silicon film. According to this model, the thermal conductivities of 10 nm, 25 nm, 50 nm and 100 nm silicon film at different temperatures are obtained, which are in good agreement with the experimental data. In our simulation, the thermal conductivities of 10 nm and 50 nm silicon film in the temperature range from 300 to 600 K are used. The temperature-dependence of thermal conductivity in silicon film is approximated in the form of a polynomial,

$$\kappa_s = \kappa_b + \kappa_b T + \kappa_c T^2, \quad 300\,\mathrm{K} \leqslant T \leqslant 600\,\mathrm{K}. \tag{9}$$

Table 2 lists the values of coefficients for thermal conductivity in 10 nm and 50 nm silicon film used in the simulator.

3. Results

Our investigation performance of SGOI nMOSFETs with double step BOX under the channel involves a subthreshold swing, output characteristics, the self-heating effect, the short-channel effect, off state current and device total capacitance.

3.1. Subthreshold swing and output characteristics

We will focus on the comparison of subthreshold swing as a function of $T_{\text{mid-BOX}}$ and channel strain for SGOI nMOSFETs.

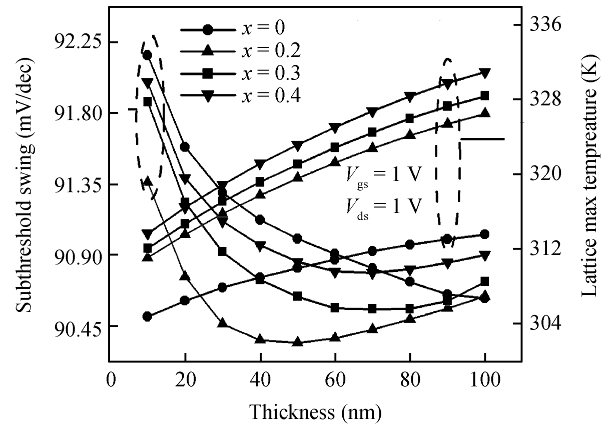

Fig. 3. Subthreshold swing and maximum lattice temperature of SGOI versus BOX thickness.

When Ge content x in $Si_{1-x}Ge_x$ is equal to 0, SGOI MOSFETs are equivalent to fully-depleted SOI (FD-SOI) MOSFETs. For FD-SOI MOSFETs, when neglecting the quality of front and back oxide interfaces, the subthreshold swing (S) is given as[19]

$$\frac{1}{S} = \frac{q}{k_B T} \frac{\dfrac{1}{C_{Si}} + \dfrac{1}{C_{BOX}}}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_{Si}} + \dfrac{1}{C_{BOX}}}, \tag{10}$$

where k_B is the Boltzmann constant, q is the elementary electronic charge, C_{Si} is the Si film capacitance, C_{BOX} is the buried oxide capacitance, and C_{ox} is the gate oxide capacitance. Starting from Eq. (10), one can obtain an equivalent expression as

$$S = \frac{k_B T}{q} \left(1 + \frac{C_{Si} C_{BOX}}{C_{ox}(C_{Si} + C_{BOX})}\right). \tag{11}$$

In the general case, C_{ox} is much larger than C_{BOX}, and C_{Si} is much larger than C_{BOX}. Hence, S is simplified as

$$S = \frac{k_B T}{q} \left(1 + \frac{C_{BOX}}{C_{ox}}\right). \tag{12}$$

One can observe that S is inversely proportional to $T_{\text{mid-BOX}}$ when the ambient temperature remains constant. The effect of $T_{\text{mid-BOX}}$ on the subthreshold swing is shown in Fig. 3.

For $x = 0$, the subthreshold swing increases from 90.627 to 92.165 mV/dec when $T_{\text{mid-BOX}}$ decreases from 100 to 10 nm. The trend is in good agreement with Eq. (12). And the lattice maximum temperature decreases from 313.6 to 304.8 K in this range. This indicates that thinner $T_{\text{mid-BOX}}$ decreases the self-heating temperature. This result can be explained by the thermal resistance R_{th} expression[20] ,

$$R_{th} = \frac{1}{2W} \left(\frac{t_{BOX}}{\kappa_{BOX} \kappa_{Si} t_{Si}}\right)^{1/2}, \tag{13}$$

where W is the device width, t_{BOX} and t_{Si} are the thickness of the BOX and Si body, respectively, and κ_{Si} and κ_{BOX} are the thermal conductivity of the BOX and Si layer, respectively. According to Eq. (13), R_{th} is proportional to $T_{\text{mid-BOX}}$. There is a difference between SGOI ($x > 0$) and FD-SOI ($x = 0$) in

the subthreshold swing. For Ge content being not equal to 0, as the BOX thickness increases from 10 to 100 nm, the subthreshold swings decrease to a minimum, then begin to increase and even become greater than that in FD-SOI. This phenomenon can be explained as follows. As can be seen from Eq. (12), S increases with an increasing lattice temperature T and decreases with an increasing $T_{\text{mid-BOX}}$. Thus, when $T_{\text{mid-BOX}}$ increases to a certain critical thickness, the reduction in subthreshold swing caused by increasing $T_{\text{mid-BOX}}$ carries more weight compared to the increase in subthreshold swing resulting from increasing lattice temperature. As $T_{\text{mid-BOX}}$ is beyond this critical thickness, the latter is a more dominant factor than the former.As for FD-SOI ($x = 0$), the subthreshold swing is mainly dependent on $T_{\text{mid-BOX}}$ because of slight variation in the lattice temperature, as can been seen in Fig. 3. Degradation of the subthreshold swing can be attributed to that the self-heating temperature increases with increasing Ge content. The subthreshold swing of SGOI nMOSFETs is within a range from 0.2 to 0.4, which is smaller than that of FD-SOI nMOSFETs. This is because the equivalent capacitance of strained Si/$\text{Si}_{1-x}\text{Ge}_x$ compound layer in SGOI nMOSFETs is less than that of Si film in FD-SOI nMOSFETs. According to Eq. (10), this will lead to a slight decrease in the subthreshold swing. The subthreshold swing of the SGOI nMOSFETs increases with Ge content increases from 0.2 to 0.4. This is because the equivalent capacitance of the strained Si/$\text{Si}_{1-x}\text{Ge}_x$ compound layer is enhanced with increasing permittivity of $\text{Si}_{1-x}\text{Ge}_x$originated from increasing Ge content[21]. In addition, increasing Ge content can result in a higher self-heating temperature, as shown in Fig. 3. This is because the thermal conductivity (0.05–0.1 W/(cm·K)) of $\text{Si}_{1-x}\text{Ge}_x$is very poor and more heat is generated by enhanced current density caused by greater Ge content.

In the case of different $T_{\text{mid-BOX}}$ and channel strain, the output characteristics of SGOI nMOSFETs with and without the self-heating effect are shown in Fig. 4. The gate bias is held at 1.5 V and the drain bias is ramped up from 0 to 2 V. SGOI with a $T_{\text{mid-BOX}}$ of 100 nm suffers a lot from the self-heating effect in comparison to SGOI with a $T_{\text{mid-BOX}}$ of 10 nm and 50 nm. The thicker BOX, the more serious the degradation becomes, as shown in Figs. 4(a), 4(b) and 4(c), respectively. This is because the thermal resistance of a thicker BOX is larger than that of a thinner BOX. Under the condition of identical $T_{\text{mid-BOX}}$, the degradation of the output characteristics of SGOI MOSFETs becomes severe as the Ge content increases. This is because of the poor thermal conductivity of $\text{Si}_{1-x}\text{Ge}_x$ and a large temperature rise caused by enhanced carrier mobility.

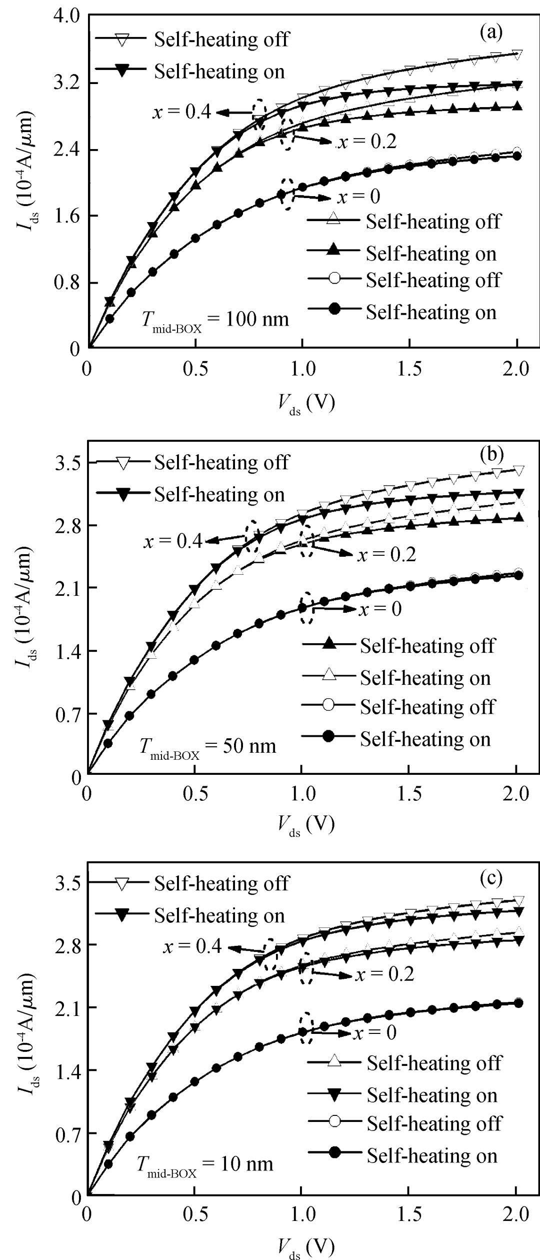

Fig. 4. Output characteristics of the SGOI. (a) $T_{\text{mid-BOX}} = 100$ nm. (b) $T_{\text{mid-BOX}} = 50$ nm. (c) $T_{\text{mid-BOX}} = 10$ nm.

3.2. The self-heating effect

A temperature distribution in SGOI nMOSFETs with a Ge content of 0.4 in case of a $T_{\text{mid-BOX}}$ of 50 nm is shown in Fig. 5. The gate bias is held at 1.5 V and the drain bias is ramped up from 0 to 2 V. The initial temperature of the device is assumed to be 300 K. The temperature profile is extracted along the channel and 5 nm below the gate oxide layer in different Ge contents and the $T_{\text{mid-BOX}}$, as shown in Fig. 5. This shows that most heat is generated near the drain-body junction. The self-heating temperature decreases with decreasing $T_{\text{mid-BOX}}$, as shown in Fig. 5. The heat generation in the channel can be transferred into the substrate through a thinner BOX quickly. The self-heating temperature of the SGOI MOSFETs with a Ge content of 0.4 is higher than that of SGOI MOSFETs with a Ge content of 0. For example, in the case of a $T_{\text{mid-BOX}}$ of 50 nm, the maximum lattice temperature in the SGOI with a Ge content of 0.4 is 377 K, and the maximum lattice temperature in the SGOI with a Ge content of 0 is 338 K. This is attributed to a lower thermal conductivity of the $\text{Si}_{1-x}\text{Ge}_x$layer and a higher current density, which degrades device performance and long-term reliability.

The heat generation near the drain-body junction results in the decline of electron velocity and degradation of mobility in SGOI nMOSFETs, as shown in Figs. 6 and 7. Figure 6 shows that the electron velocity increases with decreasing $T_{\text{mid-BOX}}$. This is because the electron mobility distribution in the SGOI with a thinner BOX is higher than that in the SGOI with a thicker BOX, as shown in Fig. 7. In addition, the electron ve-

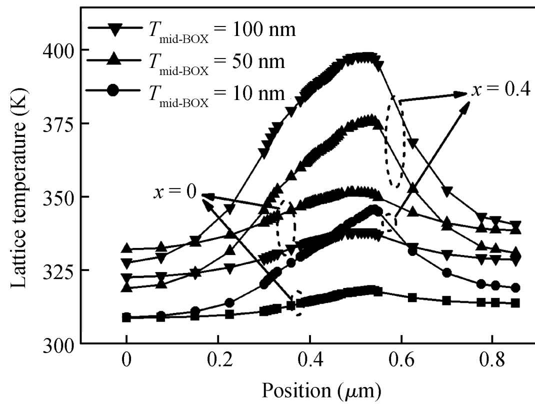

Fig. 5. Temperature profile of the SGOI with $T_{\text{mid-BOX}}$ and channel strain.

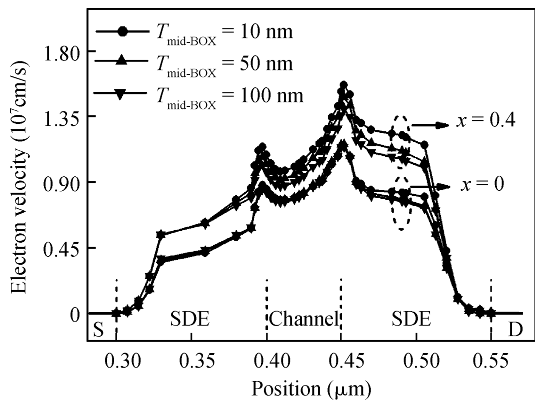

Fig. 6. Electron velocity profile along the channel in the SGOI with different $T_{\text{mid-BOX}}$ and channel strains.

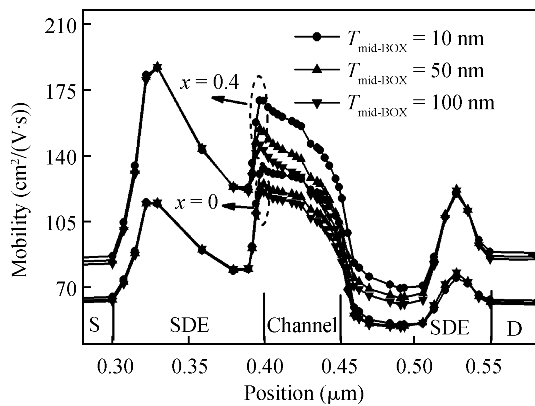

Fig. 7. Electron mobility profile along the channel in the SGOI with different $T_{\text{mid-BOX}}$ and channel strains.

locity increases as the Ge content increases. The electron mobility increase is due to lower intervalley scattering resulting from a valley splitting[11].

3.3. The short-channel effect

The DIBL effect of SGOI nMOSFETs as a function of $T_{\text{mid-BOX}}$ and channel strain is shown in Fig. 8. DIBL is defined

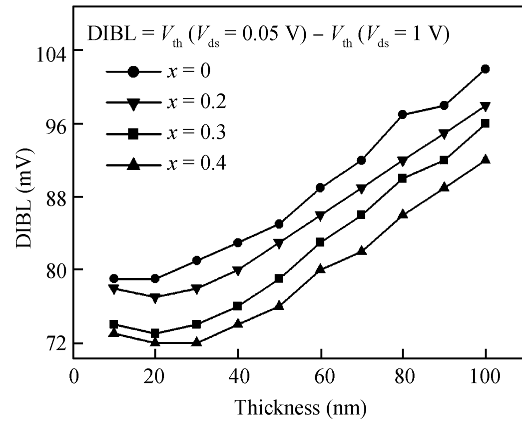

Fig. 8. DIBL of the SGOI versus BOX thickness.

as[21]

$$\text{DIBL} = V_{\text{T}}\,(V_{\text{ds}} = 0.05\,\text{V}) - V_{\text{T}}\,(V_{\text{ds}} = 1\,\text{V}), \tag{14}$$

where V_{T} is the threshold voltage. DIBL decreases when $T_{\text{mid-BOX}}$ varies from 10 to 20 nm. The electric field line coming from the drain region extends to the body through a thin BOX, which leads to an increase in body electrical potential, so the threshold voltage decreases. In contrast, DIBL increases when $T_{\text{mid-BOX}}$ changes from 20 to 100 nm. This can be explained as follows. When V_{ds} increases, the charge carriers can obtain enough energy and be swept across the drain-body depletion, which results in an increase in both the self-heating temperature and the impact ionization probability. Simultaneously, this leads to the generation of electron–hole pairs in the vicinity of the drain-body junction[22]. Holes created by impact ionization move toward the region of the source-body interface near the buried oxide layer. These holes will lower the potential barrier at the source-body junction. The higher the temperature, the greater the reduction in potential barrier. Hence, the threshold voltage decreases with increasing $T_{\text{mid-BOX}}$. Compared to the SGOI with a Ge content of 0, the DIBL effect is well suppressed in the SGOI with a range from 0.2 to 0.4. Because of a lower potential barrier for holes at the PN junction of the SiGe, holes generated by impact ionization are prone to flow across the source-body barrier, instead of accumulating in the float body region[23]. A thicker $T_{\text{mid-BOX}}$ can cause a larger DIBL. This is because the electric field from the drain regime penetrates into the channel region through the BOX, which will result in an increase in the subthreshold swing. In contrast, a thinner $T_{\text{mid-BOX}}$ decreases DIBL because the field penetrates all the way through the BOX to the substrate and does not extend to the channel[24, 25].

3.4. Off state current

Off state current for SGOI nMOSFETs as a function of $T_{\text{mid-BOX}}$ and channel strain is investigated in Fig. 9. The off state current improves as $T_{\text{mid-BOX}}$ increases. For FD-SOI, the subthreshold drain leakage current (V_{gs} = 0) can be modeled as[1]

$$I_{\text{OFF}} = \frac{W}{L}\mu C_{\text{G}}(m-1)\left(\frac{k_{\text{B}}T}{q}\right)^2 \exp\left(-\frac{qV_{\text{T}}}{mk_{\text{B}}T}\right), \tag{15}$$

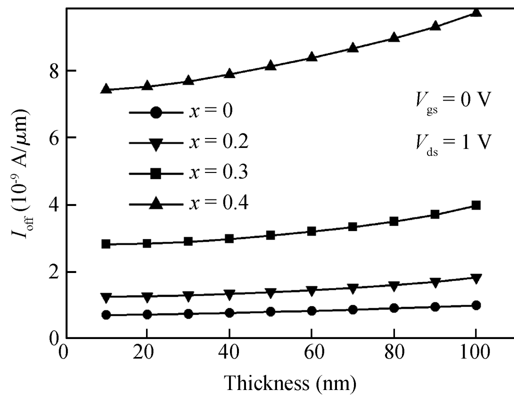

Fig. 9. Off state current of the SGOI versus BOX thickness.

where W is the device width, L is the channel length and m is the ideality factor which can be given as

$$m = 1 + \gamma \frac{C'}{C_G}, \quad (16)$$

where C_G is the gate-to-channel capacitance, C' is given as

$$C' = \frac{C_{SOI}}{C_{SOI} + C_{BOX}}, \quad (17)$$

where C' and γ account for the degradation of the subthreshold swing due to the short-channel effects. Using Eq. (15), one can obtain dependence of the sub-threshold current on temperature as

$$\frac{\partial I_{OFF}}{\partial T}\frac{1}{I_{OFF}} = \frac{\partial \mu}{\partial T}\frac{1}{\mu} + \frac{2}{T} - \frac{q}{mk_BT}\frac{\partial V_T}{\partial T} + \frac{qV_T}{mk_BT^2}. \quad (18)$$

Among these terms, the first is the temperature dependence of the carrier mobility. The second is the heating-induced degradation of the subthreshold slope. The third term is the contribution of temperature dependence of the threshold voltage. The last term indicates that the I_{OFF} increases with temperature due to the T^2dependence of the preexponential factor[1]. The first term is inclined to slightly decrease the temperature coefficient of I_{OFF}. In general, the sum of these four terms is larger than zero, and the off state current increases with increasing temperature. Therefore, a thicker $T_{mid\text{-}BOX}$ will enhance the off state current due to a higher self-heating temperature. In addition, for an SGOI with an identical structure, the off state current increases with an increasing channel strain. A higher channel strain further enhances the carrier mobility, raises the device temperature and reduces the threshold voltage. According to Eq. (15), all of these factors result in further improvement of the off state current.

3.5. Total capacitance

In view of the role of intrinsic delay in digital operation, a comparison of device structure capacitance C_{Total} of the device as a function of the Ge content x and $T_{mid\text{-}BOX}$ is shown in Fig. 10. The measuring frequency is set to 1 MHz. Figure 10 indicates that the capacitance of the device increases with increasing Ge content. The dielectric constant of the $Si_{1-x}Ge_x$ increases as the Ge content x increases[21], which contributes to the enhancement of the total capacitance. In addition, it can

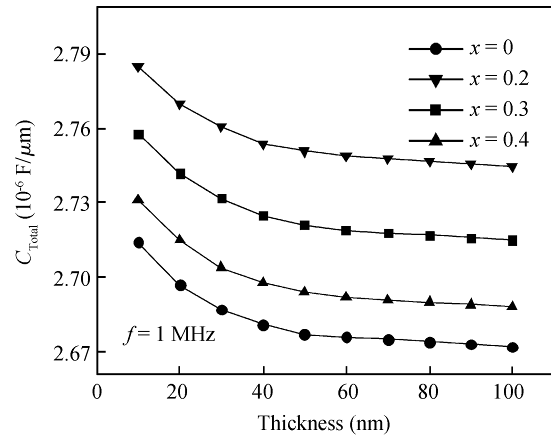

Fig. 10. Total capacitance C_{Total} versus BOX thickness.

be seen clearly, by and large, that C_{Total} decreases generally as $T_{mid\text{-}BOX}$ increases. However, the dependence of C_{Total} on $T_{mid\text{-}BOX}$ becomes weak when $T_{mid\text{-}BOX}$ is beyond 40 nm and the fluctuation of C_{Total} is only about 2% in the $T_{mid\text{-}BOX}$ range from 50 to 100 nm. Hence, the self-heating temperature can be reduced by eliminating moderately $T_{mid\text{-}BOX}$ while the device capacitance remains almost unchanged.

4. Conclusions

An extensive thermal and electrical study of SGOI nMOSFETs with a double step BOX has been performed using a numerical simulation. A low field mobility model is developed and verified. Self-heating effects and reduced thermal conductivity resulting from phonon boundary scattering in thin silicon film are taken into consideration. When $T_{mid\text{-}BOX}$ decreases from 100 to 10 nm, the off state current, output characteristics degradation, self-heating effect, mobility degradation and DIBL effect in SGOI MOSFETs can be well suppressed. In addition, SGOI nMOSFETs with high channel strain exhibit an enhanced performance compared to FD-SOI nMOSFETs. In conclusion, we propose that employing SGOI MOSFETs with a thinner BOX under the channel can enhance the overall performance and device reliability in the gate length of the nanoscale regime.

References

[1] Fiegna C, Yang Y, Sangiorgi E, et al. Analysis of self-heating effects in ultrathin-body SOI MOSFETs by device simulation. IEEE Trans Electron Devices, 2008, 55(1): 233

[2] http://www.synopsys.com/TOOLS/TCAD/Pages/strainedsilicon.aspx

[3] Mizuno T, Sugiyama N, Tezuka T, et al. (110) strained-SOI nMOSFETs with higher electron mobility. IEEE Trans Electron Devices, 2003, 24(4): 266

[4] Cheng Z Y, Pitera A J, Lee M L, et al. Fully depleted strained-SOI n and p-MOSFETs on bonded SGOI substrates and study of the SiGe/BOX interface. IEEE Trans Electron Devices, 2004, 25(3): 147

[5] Gu W Y, Liang R R, Zhang K, et al. Impact of <100> channel direction for the high mobility p-MOSFETs on biaxial strained

silicon. Journal of Semiconductors, 2008, 29(10): 1893
[6] Irisawa T, Numata T, Tezuka T. High-performance uniaxially strained SiGe-on-insulator pMOSFETs fabricated by lateral-strain relaxation technique. IEEE Trans Electron Devices, 2006, 53(11): 2809
[7] Jenkins K A, Rimand K. Measurement of the effect of self-heating in strained-silicon MOSFETs. IEEE Electron Device Lett, 2002, 23(6): 360
[8] Yazdani K E, Yang Y Z, Asheghi M. Ballistic phonon transport and self-heating effects in strained-silicon transistors. IEEE Trans Compon Packag Technol, 2006, 29(2): 254
[9] Liu W, Asheghi M. Thermal modeling of self-heating in strained-silicon MOSFETS. Proc IEEE ITHERM Conf, 2004, 2: 605
[10] Zhang Z X, Lin Q , Zhu M, et al. A new structure of SOI MOSFET for reducing self-heating effect. Ceramics Int, 2004, 30(7): 1289
[11] Kim S J, Shim T H, Choi K R, et al. Comparative study of self-heating effect on electron mobility in nanoscale strained silicon-on-insulator and strained silicon grown on relaxed SiGe-on-insulator n-metal–oxide–semiconductor field-effect transistors. Semicond Sci Technol, 2009, 24(3): 035014
[12] DESSIS-ISE Manual Ver. 10.0, ISE
[13] Lombardi C, Manzini S, Saporito A, et al. A physically based mobility model for numerical simulation of nonplanar devices. IEEE Trans Computer-Aided Design, 1988, 7(11): 1164
[14] Darwish M N, Lentz J L, Pinto M R, et al. An improved electron and hole mobility model for general purpose device simulation. IEEE Trans Electron Devices, 1997, 44(9): 1529
[15] Currie M T, Leitz, Langdo T A, et al. Carrier mobilities and process stability of strained Si n- and p-MOSFETs on SiGe virtual substrates. Vacuum Science Technology B, 2001, 19(6): 2268
[16] Roldán J B, Gámiz F. Simulation and modelling of transport properties in strained-Si and strained-Si/SiGe-on-insulator MOSFETs. Solid-State Electron, 2004, 48: 1347
[17] Masetti G, Severi M, Solmi S. Modeling of carrier mobility against carrier concentration in marsenic-, mphosphorus-, and boron-doped silicon. IEEE Trans Electron Devices, 1983, 30(7): 764
[18] Liu W, Asheghi M. Thermal conductivity measurements of ultrathin single crystal silicon layers. Trans ASME, J Heat Transf, 2006, 128(1):75
[19] Joachim H O, Yamaguchi Y, Ishikawa K, et al. Simulation and two-dimensional analytical modeling of subthreshold slope in ultrathin-film SOI MOSFET's down to 0.1 pm gate length. IEEE Trans Electron Devices, 1993, 40(10): 1812
[20] Lisa T Su, Chung J E, Antoniadis D A, et al. Measurement and modeling of self-heating in SOI nMOSFETs. IEEE Trans Electron Devices, 1994, 41(1): 69
[21] Venkataraman V, Nawal S, Kumar M J. Compact analytical threshold-voltage model of nanoscale fully depleted strained-Si on silicon germanium-on insulator (SGOI) MOSFETs. IEEE Trans Electron Devices, 2007, 54(3): 554
[22] Su P, Goto K, Sugii T, et al. Self-heating enhanced impact ionization in SOI MOSFETs. IEEE Int SOI Conf, 2001: 31
[23] Takagi S, Mizuno T, Tezuka T, et al. Channel structure design, fabrication and carrier transport properties of strained-Si/SiGe-on-insulator (strained-SOI) MOSFETs. IEDM Tech Dig, 2003: 57
[24] Kumar M J, Siva M. The ground plane in buried oxide for controlling short-channel effects in nano scale SOI MOSFETs. IEEE Trans Electron Devices, 2008, 55(6): 1554
[25] Balestra F, Cristoloveanu S. Special mechanisms in thin film SOI MOSFETs. 20th International Conferences on Microelectronics, 1995, 2: 623