Design of a passive UHF RFID tag for the ISO18000-6C protocol*

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Abstract: This paper presents a new fully integrated wide-range UHF passive RFID tag chip design that is compatible with the ISO18000-6C protocol. In order to reduce the die area, an ultra-low power CMOS voltage regulator without resistors and an area-efficient amplitude shift keying demodulator with a novel adaptive average generator are both adopted. A low power clock generator is designed to guarantee the accuracy of the clock under ±4%. As the clock gating technology is employed to reduce the power consumption of the baseband processor, the total power consumption of the tag is about 14 μW with a sensitivity of –9.5 dBm. The detection distance can reach about 5 m under 4 W effective isotropic radiated power. The whole tag is fabricated in TSMC 0.18 μm CMOS technology and the chip size is 880 × 880 μm^2.

Key words: ISO18000-6C; UHF RFID tag; voltage regulator; clock gating
DOI: 10.1088/1674-4926/32/5/055009 **EEACC:** 1205; 2570D

1. Introduction

Radio frequency identification (RFID) tags in the UHF range have garnered great attention as the need for larger amounts of data and longer operating ranges has increased[1]. UHF RFID operates in the frequency range from 860 to 960 MHz and is able to work as a middle-to-long-range communication link between a reader and tags. The commercial applications of UHF RFID are diverse, including intelligent transportation systems, supply-chain management, industrial automation traffic toll collections and logistics[2].

However, there are several practical issues to be resolved before its widespread application. Several passive RFID tag designs have been published in the literature[1−4]; however, most of them use a protocol much simpler than the ISO18000-6C protocol. The ISO18000-6C protocol is the most popular UHF RFID protocol. It can ensure communication between thousands of tags and single or multiple readers. Another important issue is the cost per tag. The cost is currently about $0.2. The fabrication process, chip area and yield are the most important factors affecting the production cost of a tag. Stability of voltage reference is the key factor, which has significant influence on yield. Bandgap reference circuits with CMOS-based vertical bipolar transistors[5, 6] or MOSFETs operating in the sub-threshold region[7] are conventionally used in CMOS LSIs. However, they require resistors with a high resistance of several hundred megaohms to achieve low-current, subthreshold operation. Such a high resistance needs a large die area and the resistor process variations are huge. This results in higher fabricating costs and lower yields.

To solve these problems, we have designed a fully integrated UHF passive RFID tag chip which is compatible with ISO18000-6C protocol. The following sections detail our device. We describe the system architecture, show the main blocks, including the rectifier, regulator, oscillator, demodulator and baseband processor, and present the measured results of the whole tag chip.

2. Tag chip architecture

Figure 1 shows the block diagram of the proposed tag IC design. It includes a RF/analog front-end, a baseband processor and an EEPROM. The antenna is the only external component of the tag. The rectifier converts RF signal power to DC for the power supply of all active circuits on the chip. Low threshold-voltage NMOSFETs are used as rectifying devices. The regulator generates a constant DC voltage independent of the power at the antenna. The oscillator generates a 1.28 MHz clock signal. The ASK demodulator translates the ASK modulated input signal into a digital signal. The modulator acts to mismatch the IC impedance with the antenna, thereby reflecting the incident power and signaling a data “high”. The baseband processor handles the protocol, including anti-collision features, the cyclic redundancy check (CRC), error handling, enabling and

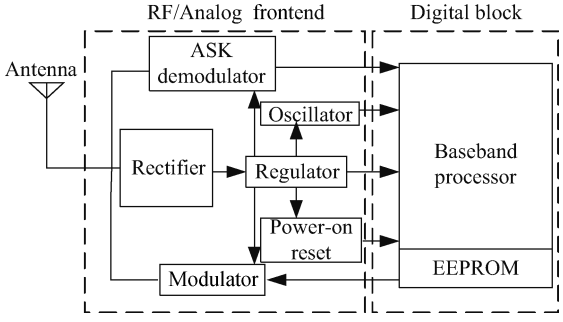

Fig. 1. Block diagram of the proposed UHF RFID tag.

* Project supported by the Guangdong Key Science and Technology Special Project of China (No. 2008A090300001).
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Received 16 August 2010, revised manuscript received 20 December 2010

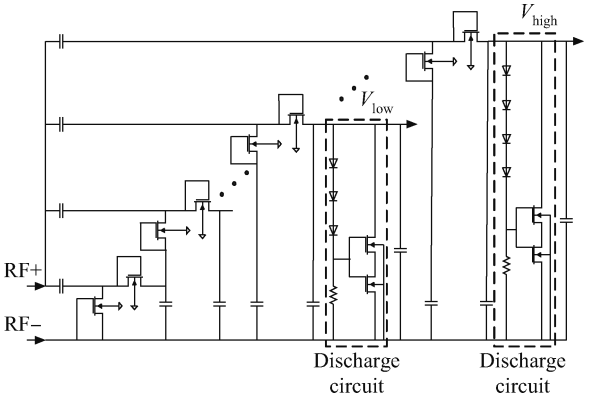


Fig. 2. Rectifier circuit base on Diode connected NMOS.

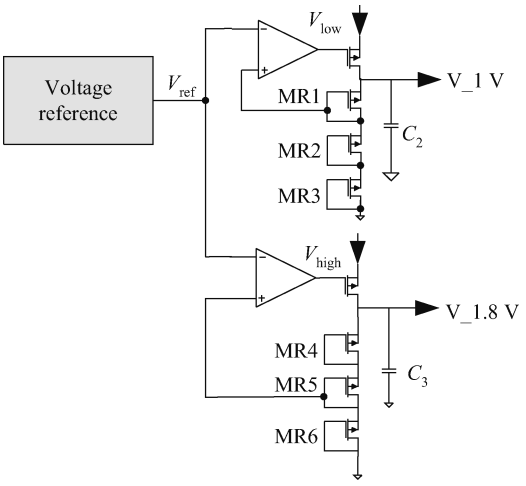


Fig. 3. Schematic of the proposed regulator.

disabling of analog circuits (power down, standby, power up), etc.

3. Building blocks

3.1. Rectifier

In this paper, the rectifier circuit uses the traditional Dickson rectifier structure. The diode-connected native NMOSFET is adopted to replace the Schottky barrier diode, as shown in Fig. 2. In this way, the manufacturing cost of the chip can be reduced by avoiding the process special requirements. The rectifier circuit consists of a multi-stage full-wave voltage cascade, discharge circuits and energy storage capacitors. The discharge circuit is added at the output of the rectifier in order to avoid voltage overdrive. The DC output voltage of an N-stage rectifier circuit can be approximately expressed as

$$V_{DC} = 2N(V_{RF} - V_{MOS}), \tag{1}$$

where N is the number of stages and one stage consists of a pair of diode-connected NMOSFETs. V_{RF} is the amplitude of the input RF signal and V_{MOS} is the voltage drop over per diode. According to Eq. (1), it is clear that with a constant V_{RF} and V_{MOS}, the larger N is, the higher the output dc voltage is. However, the simulation results show that the conversion efficiency will decrease when more stages are used. As a result, we must choose an appropriate N to achieve the optimal value of the efficiency and output voltage. We adopt the double-output design strategy proposed in Ref. [8]. V_{low} is generated by 7 stages and its value is about 1.3 V. V_{high}, it is about 2 V and an additional 4 stages are needed.

3.2. Regulator

The voltage regulator provides a stable power supply for the front-end and the other circuits. The rectifier output voltage will vary widely when changing the distance between tag and reader. As a result, an excellent power supply rejection ratio is needed in the voltage regulator design. A voltage regulator, shown in Fig. 3, is used in the tag design. The regulator circuit generates two outputs. One is the 1.8 V voltage required for the EEPROM, and the other is a 1 V voltage for other circuits. The error amplifiers are configured with differential amplifiers. To save on chip area, several diode-connected PMOS transistors play the role of a potential divider. The total quiescent current of the proposed voltage regulator is only 534 nA.

The voltage reference is shown in Fig. 4. It generates two voltages with opposite temperature coefficients and adds them to produce an output voltage with a near-zero temperature coefficient. The voltage reference consists of MOSFET circuits operated without resistors in the subthreshold region. The MOS resistor MR is operated in a strong-inversion, deep-triode region. All of the other voltage reference MOSFETs are operated in the sub-threshold region.

For $V_{DS} > 0.1$ V, the subthreshold drain current is represented by

$$I_D = KI_0 \exp\frac{V_{GS} - V_{TH}}{nV_T}, \tag{2}$$

where I_0 is the subthreshold characteristic current which can be regarded as a constant, K is the ratio of transistor's width and length, n ($= 1 + C_{js}/C_{ox}$) is the subthreshold slope factor[9], V_T is the thermal voltage and V_{TH} is the threshold voltage of a MOSFET.

The bias-current is equal to the current in MR and can be written as

$$I_B = K_{MR}\mu C_{ox}(V_{ref} - V_{TH})nV_T \ln(K_6/K_5). \tag{3}$$

The output of the reference source circuit is expressed as follows[9]:

$$\begin{aligned} V_{ref} &= V_{GS8} - V_{GS7} + V_{GS10} - V_{GS9} + V_{GS11} \\ &= V_{GS8} + nV_T \ln\frac{2K_7K_9}{K_{10}K_{11}} \\ &= V_{TH0} + T\left[\frac{kn}{q}\ln\frac{3I_B}{K_8I_0} + \frac{kn}{q}\ln\frac{2K_7K_9}{K_{10}K_{11}} - \kappa\right], \end{aligned} \tag{4}$$

where k is the Boltzmann constant, κ is the TC of V_{TH}, V_{TH0} is the threshold voltage at 0 K, T is the absolute temperature and q is the elementary charge. Therefore, the output voltage V_{ref} with a zero temperature coefficient can be obtained by adjusting the size of the transistors and is equal to V_{TH0}. In this design, the reference voltage is 725 mV at 27 ℃ with a temperature coefficient of 23 ppm/℃.

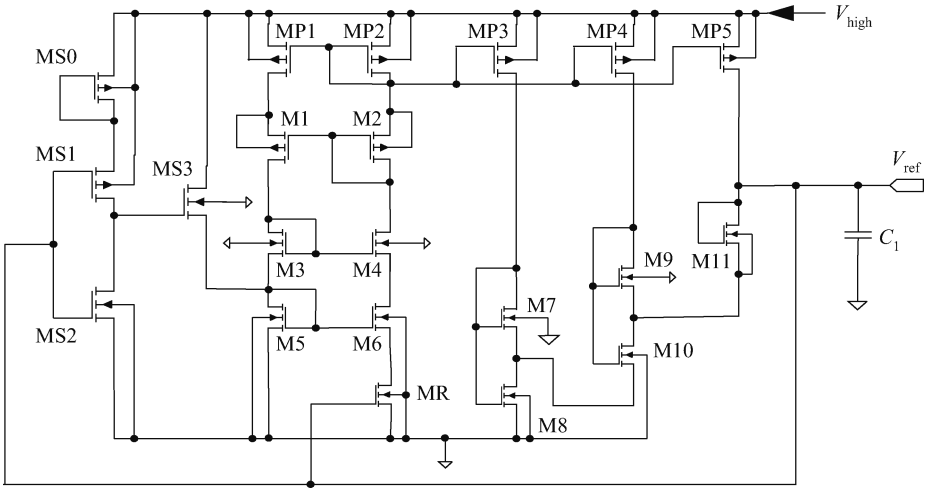


Fig. 4. Schematic of the proposed voltage reference.

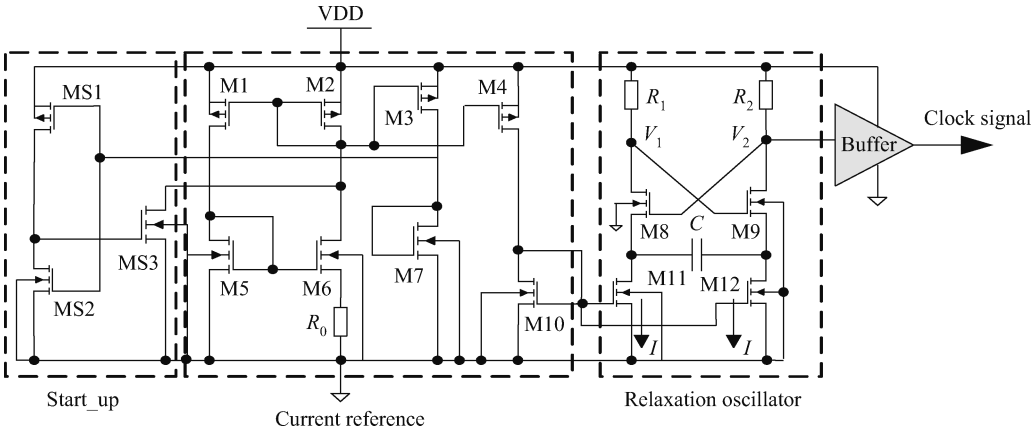


Fig. 5. Clock generation circuit.

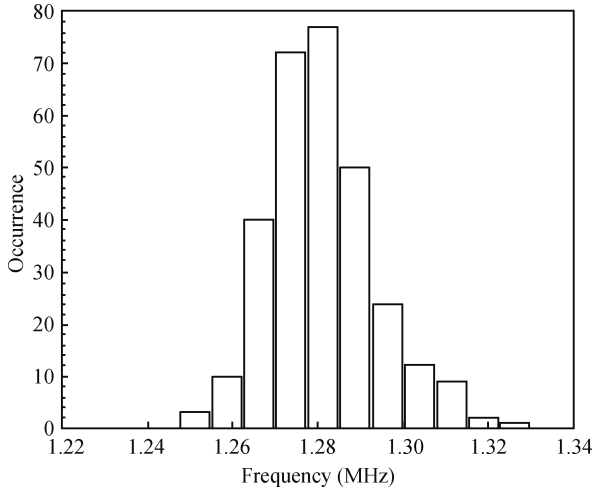


Fig. 6. Simulation of process variations for supply voltage 1 V.

3.3. Oscillator

In this paper, a relaxation oscillator (OSC), which is not sensitive to the process variation and supply voltage, is used. The oscillator, shown in Fig. 5, includes a start-up circuit, a bias current generating circuit, an oscillation circuit and a buffer. The output frequency of the oscillation is expressed as follows:

$$f = \frac{I}{2C\Delta V}, \tag{5}$$

$$\Delta V = 2IR - \left(V_{\rm TH} - nV_{\rm t}\ln\frac{I}{I_{\rm D}}\right) - \sqrt{\frac{4I}{K\left(\frac{W}{L}\right) + (2IR - V_{\rm TH})}}, \tag{6}$$

where C is the capacitance, I is the bias current and ΔV is the maximum voltage difference between V_1 and V_2. From Eqs. (5) and (6), the oscillator output frequency is closely related to the C, I, ΔV. The transistor M8 and M9 must be in the triode region in order to restrain the influence of the voltage change. The M11 and M12 transistors must be in the saturation region to ensure that the current I is accurate. The output buffer will shape the output waveform of the OSC into the standard square waveform and enhance drive capability. According to the ISO18000-6C protocol, a system clock of at least 1.28 MHz is needed and must meet the frequency tolerance specification (about ±10%). Figure 6 shows a Monte–Carlo analysis simulation of the clock generation circuit. The variation in range between the upper and lower limit is 1.25 to 1.33 MHz. So the

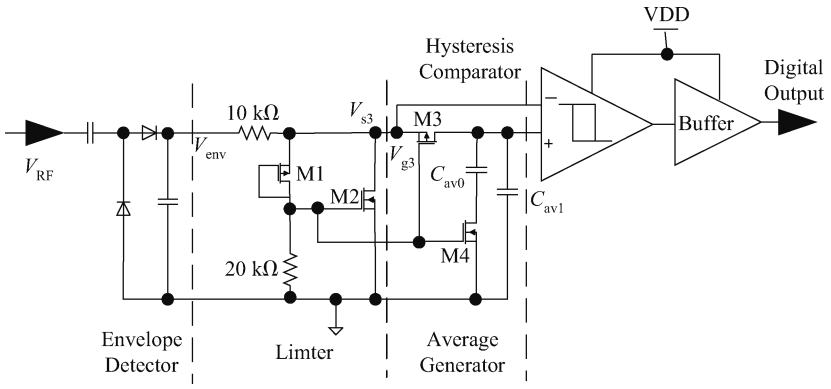


Fig. 7. ASK demodulator simplified schematic.

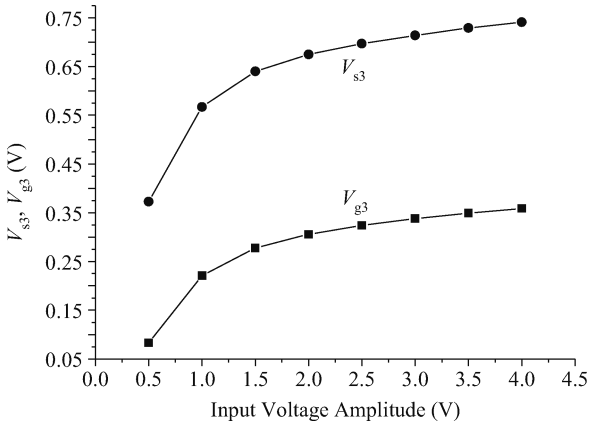


Fig. 8. Voltage of V_{s3} and V_{g3} versus input voltage amplitude.

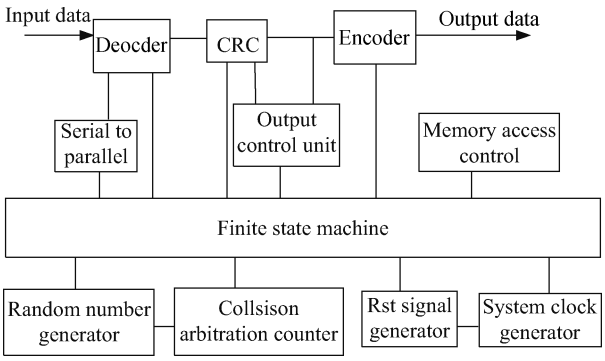


Fig. 9. Architecture of a baseband processor.

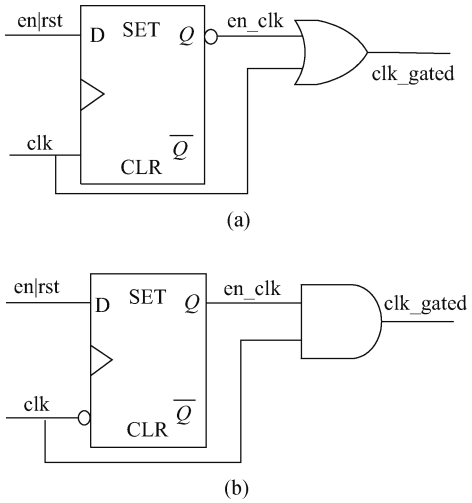


Fig. 10. Clock gating circuit. (a) Positive gating logic. (b) Negative gating logic.

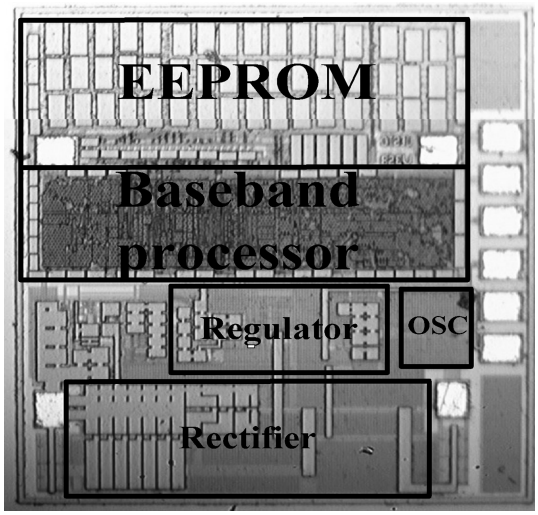


Fig. 11. Die micrograph.

maximum deviation from the nominal frequency (1.28 MHz) is about 4%. The typical power consumption value is 1.23 μW.

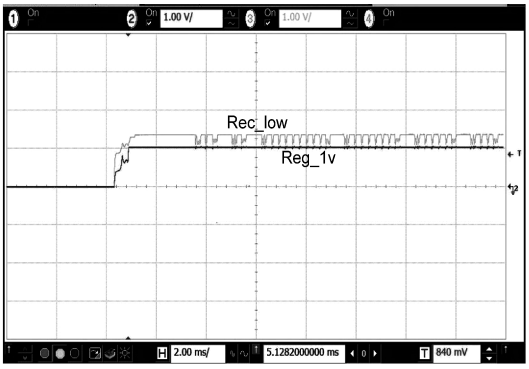
3.4. ASK demodulator

Figure 7 shows the architecture of the ASK demodulator. A single stage rectifier doubler is used to obtain the envelope of the input signal. Following the rectifier is a limiter that provides attenuation at high RF power levels. Finally, the hysteresis comparator compares the data envelope with an average of the data envelope to determine if the data is a "1" or a "0".

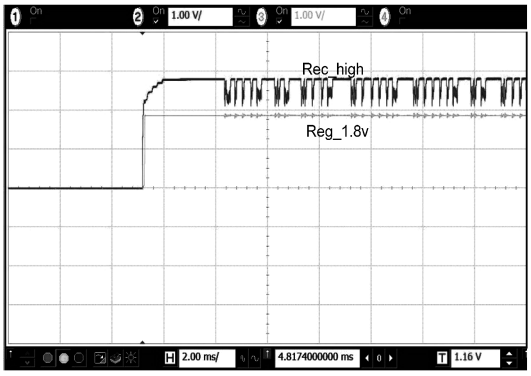
A giant resistor of several megaohms is conventionally used to obtain a stable average. However, such a high resistance needs a large die area. To save on chip area, a novel adaptive average generator is proposed. The gate voltage of M3 V_{g3} increases with the increase of V_{s3} so that the V_{GS} of M3 can remain stable to a certain extent, as shown in Fig. 8. At RF power high levels, M3's resistance decreases and M4 switches

Table 1. Result comparison.

Parameter	Ref. [3]	Ref. [4]	This work
Technology	0.35 μm CMOS with Schottky diode	0.35 μm CMOS FeRAM	Standard 0.18 μm CMOS
Power consumption (μW)	45	Not available	14
Typical working distance (m) (@ 4 W EIRP)	4.5	4.3	5
Die area (mm^2)	0.64	1.845	0.77
Commercial standard supported	Not available	ISO/IEC18000-6	ISO/IEC18000-6C



(a)



(b)

Fig. 12. Measured results of the rectifier and voltage regulator. (a) Waveform of their low output voltage. (b) Waveform of their high output voltage.

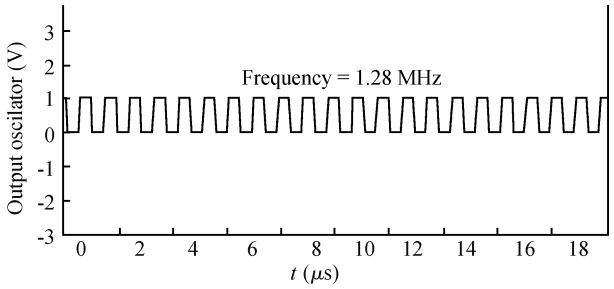
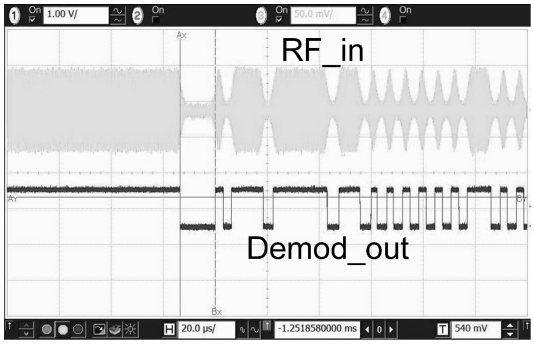


Fig. 13. Measured result of the clock generator.

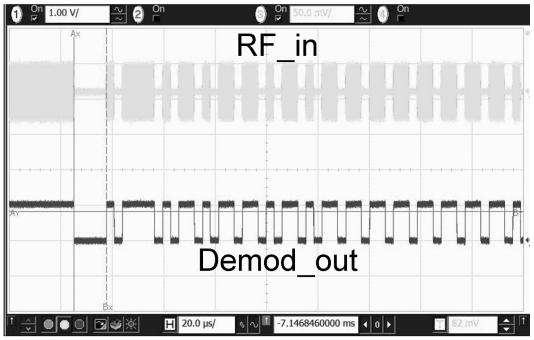
on, so that the RC time constant can remain high enough for the envelope signal.

3.5. Baseband processor

Figure 9 shows the architecture of the baseband processor. As the core unit of the chip, its power consumption accounts for a large proportion of the total power consumption. Therefore, low power design of the baseband processor is playing an increasingly important role. Clock gating technology is employed to reduce power consumption. Figure 10 shows the clock gating circuit. Each module in the digital block achieves asynchronous communication through the handshake signal and can be turned off by clock gating circuit when its communication is over. The simulation results of the power consumption with and without clock gating are 6.3126 and 12.9479, respectively. We can find that power consumption is reduced by about 36% with clock gating.



(a)



(b)

Fig. 14. Measured results of the ASK demodulator for (a) modulation depth of 80% and (b) modulation depth of 100%.

4. Measured results

The chip has been fabricated in a TSMC 0.18 μm CMOS process with an area of 880 × 880 μm^2. Figure 11 shows the fabricated RFID tag. The measured results of the rectifier and the voltage regulator are shown in Fig. 12 for a RF input power of –9.5 dBm. The two regulated voltages show a $\pm 3\sigma$ variation around 1 ± 0.1 V and 1.8 ± 0.2 V across the wafer and across temperature extremes (–25 to 85 ℃). Figure 13 is the

output of the relaxation oscillator. Figure 14 is the measured results of the ASK demodulator for modulation depths of 80% and 100%. The minimum input RF signal amplitude that can be correctly demodulated is 100 mV, the maximum input data rate is 160 kb/s. The power consumption of the digital block is 9.7 μW, which is larger than the simulation result. This is because the test pad drivers consume extra power. The total power consumption of the tag IC is 13.97 μW, and the sensitivity of the tag can reach –9.5 dBm. The detection distance is about 5 m with a 4 W EIRP reader transmit power. Table 1 compares the proposed RFID tag with the most closely related works.

5. Conclusion

This paper presents a low-power, cost-effective UHF-band passive RFID tag that is compatible with the ISO18000-6C protocol. Using a voltage regulator that only consists of MOSFETs, a stable clock generator, a novel area-efficient ASK demodulator and a low power baseband processor, the tag chip is characterized by low power, low cost and high reliability. According to the measured results, the tag can work smoothly at an operation distance of 5 m.

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