Organic thin film transistors with a $SiO_2/SiN_x/SiO_2$ composite insulator layer*

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Abstract: We have investigated a $SiO_2/SiN_x/SiO_2$ composite insulation layer structured gate dielectric for an organic thin film transistor (OTFT) with the purpose of improving the performance of the SiO_2 gate insulator. The $SiO_2/SiN_x/SiO_2$ composite insulation layer was prepared by magnetron sputtering. Compared with the same thickness of a SiO_2 insulation layer device, the $SiO_2/SiN_x/SiO_2$ composite insulation layer is an effective method of fabricating OTFT with improved electric characteristics and decreased leakage current. Electrical parameters such as carrier mobility by field effect measurement have been calculated. The performances of different insulating layer devices have been studied, and the results demonstrate that when the insulation layer thickness increases, the off-state current decreases.

Key words: organic thin film transistor; composite insulation layer; carrier mobility
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1. Introduction

In recent years, there has been considerable interest in organic-based thin film electronics for low-cost and large-area electronic application. Low-temperature deposition and solution processing can replace the more complicated processes involved in conventional Si technology. In addition, the mechanical flexibility of organic materials makes them naturally compatible with plastic substrates for lightweight and foldable products[1, 2]. But the operation mode of organic thin film transistor (OTFTs) cannot meet all of the requirements of applications. How to improve the performance of devices is still an important problem for researchers in the field of organic electronics. In recent years, SiN_x has often been used as an OTFT gate material for its good insulated quality. It is commonly used in large scale integrated circuits in 10^{15} Ω·cm resistivity. Compared with a SiO_2 dielectric constant (3–4), the SiN_x (6–10) is larger. In TFT devices, the larger the insulating dielectric constant, the smaller the thickness required of the insulation layer[3]. Thus, it increases the electric field of the semiconductor layer and reduces the device voltage, and increases the carrier mobility[4]. Because of the above advantages, SiN_x film is widely used to fabricate the TFT gate insulator. But the SiN_x film has its shortcomings, and the most pertinent point is that the interface state density between the SiN_x film and the active layer is great, when the device works the threshold voltage[5] will drift, which will reduce the stability of the thin-film transistors. So the TFT device output is not ideal with a single insulating layer of SiN_x film. We have fabricated a complex $SiO_2/SiN_x/SiO_2$, making the SiO_2 film contact the active layer, so as to avoid the threshold voltage drift. $SiO_2/SiN_x/SiO_2$ was prepared by magnetron sputtering[6], and the composite insulating layer can effectively fill the single SiN_x film defects.

2. Experiment and theory

The OTFT device structure used in this work is shown in Fig. 1. The composite insulator layer was prepared by magnetron sputtering on the ITO glass substrate, and the background vacuum was 1.1×10^{-3} Pa. The sputtering power was between 200–250 W, the deposition vacuum was about 1.2 Pa, and we controlled the thickness of the film by controlling the deposit time. CuPc thin films were prepared by vacuum deposition at a rate of 2 nm/min under a pressure of 6×10^{-4} Pa at room temperature, and the thickness of the resulting films was between 35 and 45 nm. OTFTs with a channel length $L = 0.035$ mm and a channel width $W = 5$ mm were fabricated by a mask. On top of this surface, gold was deposited through this mask to create the source (S) and drain (D) electrodes. In the experiments, the current–voltage characteristics were calculated by transistor-detector equipment, which we assembled. All experiments were carried out at room temperature.

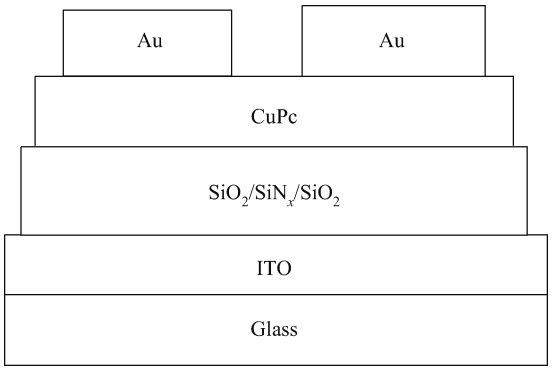

Fig. 1. Schematic structure of $SiO_2/SiN_x/SiO_2$ composite insulator layer thin film transistor.

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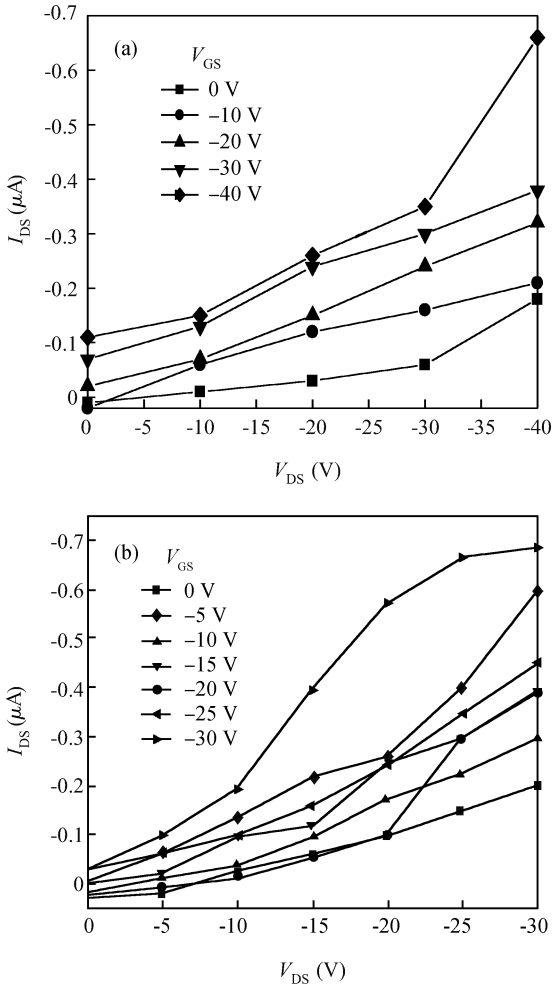

Fig. 2. Drain-current characteristics of (a) a SiO_2 OTFT and (b) a $SiO_2/SiN_x/SiO_2$ OTFT.

For inorganic and organic TFTs, the gate insulation layer capacitance per unit area is an important factor affecting these devices. The threshold voltage V_T and open state current I_{on}[7] are

$$V_T = V_s + V_{ms} - \frac{Q_{ss} + Q_B}{C_i}, \quad (1)$$

$$I_{on} = -\frac{W}{L}\mu_n C_i \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right], \quad (2)$$

where C_i is the gate insulator capacitance per unit area, W and L are the width and length of the channel, μ_n and μ_p are, respectively, the electron and hole mobility, V_s is the characterization of the active layer of an amorphous silicon (or polysilicon) thin film surface with a curved surface potential, V_{ms} is the voltage difference between the active layer and the gate, Q_{ss} is the fixed charge in the insulating layer, moving I_{on} and interface states (their equivalent to the surface state charge) generated by induction charge density, and Q_B for the depletion region is a saturated active layer surface charge density. Increasing C_i and decreasing Q_{ss} improve I_{on}, and $C_i = \varepsilon_o \varepsilon_S / d$ depends on the layer of silicon nitride film relative dielectric constant ε and thickness d; when ε is greater, d is smaller, and I_{on} is larger. However, the thickness of the insulating layer is limited, so it is often considered to maximize the dielectric constant ε to improve I_{on}. So improve the insulation strength of silicon nitride film, which can maximize ε.

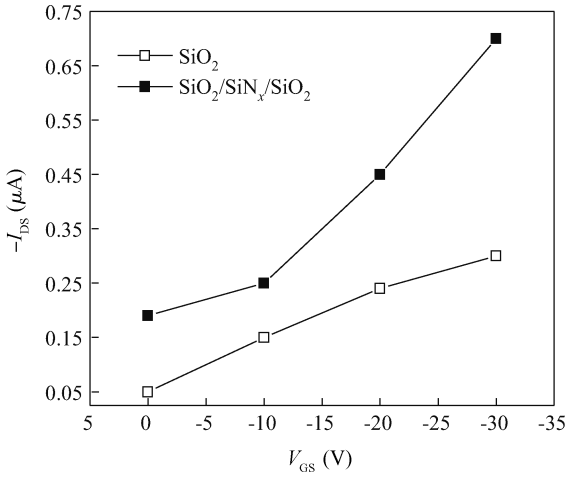

Fig. 3. Drain current–gate voltage curves of the SiO_2 insulation layer and the $SiO_2/SiN_x/SiO_2$ insulating layer devices (V_{DS} = −30 V).

We tested the $SiO_2/SiN_x/SiO_2$ composite insulation layer capacitance per unit area by using ITO as the electrode surface, with a ZL6 automatic LCR meter, aluminum electrodes below each corresponding to a composite insulating layer capacitance for measurement. For sputtering at different times to measure the capacitance of composite insulating layer, respectively. The composite film thickness was tested by a Korea ST2000-DLXn Apectra Thick STD-Auto device.

3. Results and discussion

In order to compare the device performance of a single insulation layer and a composite insulation layer, the following two components were prepared:

Device A: indium tin oxide (ITO)/SiO_2 (435 nm)/CuPc (35 nm)/Au; Device B: indium tin oxide (ITO)/($SiO_2/SiN_x/SiO_2$) (432 nm)/CuPc (35 nm)/Au.

Devices A and B are a SiO_2 insulation layer device and a $SiO_2/SiN_x/SiO_2$ composite insulation layer device. The SiO_2 thickness of device A is almost equal to the composite insulation thickness of device B. Figures 2(a) and 2(b) are the output characteristics of the two devices. We can see from the diagram that the composite insulating layer significantly reduced the leakage current of the device, because the composite insulation layer of the film effectively filled the SiN_x/SiO_2 layer of the pinhole and the other defect. Similarly, SiO_2 filled many SiN_x film layer defects, making the composite insulation layer resistivity larger. From Fig. 2, the composite insulation resistance rate is larger than the single layer of SiO_2. When the gate and the drain voltage increase by the same amount, the drain current of the composite insulation layer device is double that of the single SiO_2insulating layer devices and the carrier mobility is also high. This shows that the composite insulation layer improved the device performance.

Since the two devices are operating in the linear region, according to the linear region of the carrier mobility formula,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L}\mu C_i V_{DS}. \quad (3)$$

Here, g_m is the transconductance and V_{DS} is constant. The relationship between the channel current I_{DS} and the gate voltage V_{GS} is shown in Fig. 3, where the value of the slope curve is the transconductance g_m in size, calculate the value of mobility. When $V_{DS} = -30$ V, the mobility of the SiO_2 insulation layer device is 1.1×10^{-6} cm^2/(V·s) and the $SiO_2/SiN_x/SiO_2$ composite insulating layer device is 1.8×10^{-6} cm^2/(V·s). In our devices, the insulating layer thickness is about a few hundred nanometers and the gate bias usually reaches tens of volts, so the electric field to form a gate bias is 10^5 V/cm. In this case, the device carrier mobility by the electric field is large. A thick insulating layer can achieve further excellent insulation properties, reducing the device leakage current and increasing the device's ability to fight through, but it can also cause the device to reduce the carrier mobility, increasing the threshold voltage. A thin insulating layer can improve the device carrier mobility but also lead to increased device leakage current and a reduced ability to fight through. As the source and drain electrodes were prepared by vacuum deposition, the insulating layer property will be reduced by high temperature vacuum deposition of the source and drain electrodes.

Increasing the insulating layer thickness of the device would reduce its mobility and off-state current. The drain current caused by different factors include two aspects: one is due to the thickness of a thin insulating layer in the same gate leading to the semiconductor layer under a bias electric field enhancement, and the other is due to a thinner thickness lead insulation per unit area capacitance increase, which would result in saturation current. When the insulating layer is thick, the gate leakage current is relatively small, and this will not cause closure of the current increase. As the composite insulation layer between the gate and the source of the leakage current is relatively large, the device saturation region is not obvious, and it is mainly caused by the sputtering process.

4. Conclusion

In conclusion, we fabricated a $SiO_2/SiN_x/SiO_2$ composite insulating organic thin film transistor. A composite insulating layer was prepared by magnetron sputtering. Compared to a single SiO_2 insulation layer, composite insulating layer devices showed improved carrier mobility and increased breakdown voltage. With different thicknesses of composite insulating layer device performance, the devices were obtained by comparing the rate of carrier mobility performance and the off-state current. Reducing the insulation thickness can increase the electric field strength substantially and improve the OTFT performance. However, the lower thickness of the insulating layer can cause a larger off-state current.

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