Body-contact self-bias effect in partially depleted SOI-CMOS and alternatives to suppress floating body effect

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Abstract: As SOI-CMOS technology nodes reach the tens of nanometer regime, body-contacts become more and more ineffective to suppress the floating body effect. In this paper, self-bias effect as the cause for this failure is analyzed and discussed in depth with respect to different structures and conditions. Other alternative approaches to suppressing the floating body effect are also introduced and discussed.

Key words: partially depleted SOI-CMOS; floating body effect; hot-carriers; kink-effect; gate oxide tunneling
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1. Introduction

Floating body effect (FBE) is an inherent property in partial depleted (PD) SOI-CMOS (especially in nMOS) devices. Taking an nMOSFET as example, in most common cases the FBE is caused by the hot-carrier generation due to multiplication in the channel pinch-off region near the drain terminal when the device is operating under saturation conditions. As a result, the electrons from the hot-carriers will merge into the inversion channel flowing to the drain, becoming part of the I_{DS}. On the other hand, the holes from the hot-carriers will flow into the grounded p-substrate to form the substrate current I_{SUB} if the device is not made on SOI substrate. However, in the case of SOI-CMOS, these hot-holes have no path to go out of the floating body and they accumulate in the non-depleted floating-body region under the depletion layer and raise the potential of the body and thus lower the V_T of the nMOS device that causes the I_{DS} to increase. Hot carrier multiplication in silicon MOSFET needs certain minimum voltage to trigger which is corresponding to the Si band-gap of 1.12 eV, that means the hot-carrier related FBE can occur only when the V_{DS} is higher than 1.12 V, and explains why the I_{DS} increase looks quite abrupt as Kinks in the higher V_{DS} region. Multiplication factor is about two orders lower in the case of pMOS devices and the FBE in SOI-pMOS devices can usually be neglected as long as it is related to hot-carriers. Therefore nMOS device is mainly discussed in this paper and FBE in pMOS device is only dealt with for the cases of gate-tunneling related FBE.

FBE is harmful in many SOI-CMOS applications, especially in mixed-signal and radiation-hard areas. The most common and standard way to suppress hot-carrier related FBE is using body-contact (BC) for SOI-nMOS devices to make a path out for those hot-holes. For an easier way to design the body-contacts, T-gate or H-gate are the most commonly used structures and are actually of the same type, and the latter is just for wider nMOSFET's so as to let the holes to flow out in both directions. Figure 1 shows a top-view of a typical T-gate SOI-nMOSFET that allows for a converse p^+ region beyond the T-gate top side where body-contacts can be made. In this case, the so called floating body is actually the narrow and thin low-doped p-type (p-) layer between the source (S) and drain (D) and underneath the depletion layer below the poly-gate. Figure 2 shows a closer picture of this floating body in view of a cross-section of the device. It can be seen that for the SOI-nMOS transistor operating under saturation, there is a depletion layer with its maximum thickness between the inversed channel and the neutral floating body. The thickness of this depletion layer is W_{MAX} which can be described by Eq. (1) below with a uniform doping condition of N_A of the p-type floating body.

$$W_{MAX} = \sqrt{\frac{4\varepsilon_s kT \ln \dfrac{N_A}{n_i}}{q^2 N_A}}. \tag{1}$$

Figure 3 gives the curves derived from Eq. (1). Those holes that cause FBE actually accumulate in the region below the W_{MAX}. As SOI-CMOS technology nodes approaching tens of

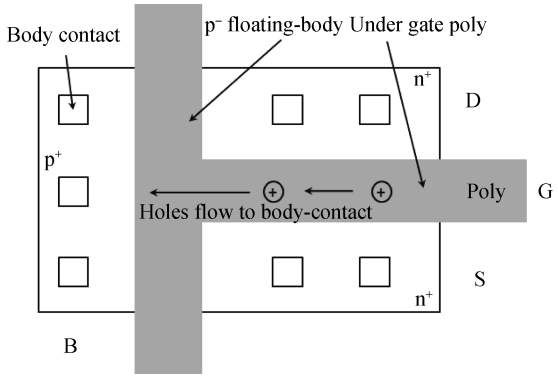

Fig. 1. Top view of a T-gate BC structure.

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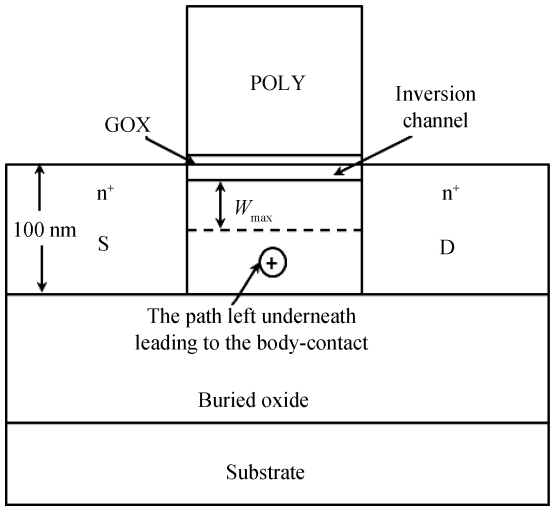

Fig. 2. Cross-section view of an SOI nMOS device. To simplify analysis, LDD is omitted.

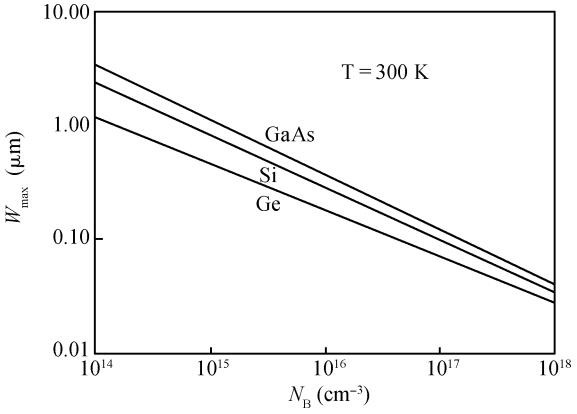

Fig. 3. Curves of W_{MAX} versus N_B.

nanometers, this floating body becomes thinner and narrower (L_G), and the path for holes to reach the body-contact thus becomes longer (W_G) and I_{SUB} flowing to the body-contact will result more voltage drop along the path. As long as the resistance of this path gets high enough, body-contact will no longer work. To give a quantitative picture of how high this resistance can be, let's look into an example of the 0.13 μm SOI-CMOS technology which is under development in our lab of Grace Semiconductor Manufacturing Corporation (GSMC). The top Si thickness is 100 nm, and the V_T implantation is 3×10^{12} cm^{-2} of boron with energy of 13 keV, suppose 80% of the implanted boron is kept within this 100 nm top silicon. Using a uniform approximation the doping concentration is about 2×10^{17} cm^{-3} and it can be found from the curves of Fig. 3 the corresponding W_{MAX} is 60 nm and the resistivity of the floating body is about 0.12 Ω·cm. Taking account of the thickness of the floating body of 40 nm, the sheet resistance of this layer is as high as 300 kΩ. The path length is the W_G of the transistor, even for narrow transistors the series resistance of the floating body can reach 1 MΩ or higher, let alone those wide ones with huge W_G. So it is not surprising that most body-contacts become ineffective under such circumstances.

The T-gate in Fig. 4 with a notched active area is an improved design from that in Fig. 1 in order to reduce the drain leakage current caused by the body-contact p^+ region. The p^+ area for body contact should be shielded from nLDD implants and shares the same pLDD of pMOSFET's. It should be noted that part of the top side of the T-gate poly will be p^+ rather than n^+ and this would impact the depletion depth underneath, however the path for hole to flow to the body-contacts is still intact. Figure 5 shows an old structure of body-contacts in which the p^+ areas are made inside the source region of the SOI-nMOSFET. This design is still used in some big size design but for the case of very short channel the overlay of p-plus lithography makes it unfeasible. In addition, this approach reduces the I_{DS} capability.

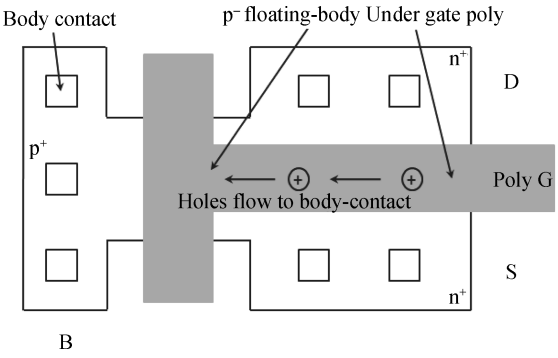

Fig. 4. Improved T-gate for body-contacts.

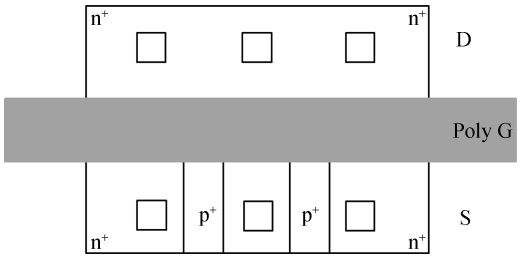

Fig. 5. Body-contacts in the source.

2. Alternative approaches besides body-contact

As an alternative to the body-contact, dual-gate structure in Fig. 6 has been reported long ago that it can effectively suppress the hot-carrier related kink-effect[1, 2]. The dual-gate in fact is using a split-gate to behave like a single gate, only to use an additional n^+ reach-through region in between the dual-gate to separate the body into two parts, and the upper part of the transistor (the service transistor) suffers all the hot-carriers and floating body effect and protects the lower part, the master transistor, free from hot-carrier and floating body effect and thus keeps its V_T intact. As a result, the overall characteristics of the dual-gate device are kink free. One advantage of this structure is that, it is always kink-free effective regardless of either the width or the length of the gate, nor the top-Si thickness. Therefore some designers are interested to use dual-gate to replace body-contact, especially in the case of wide devices.

However, in our SOI-CMOS development, it was found that the dual-gate structure becomes ineffective in the cases when the GOX gets thinner below 20 Å because of the charge

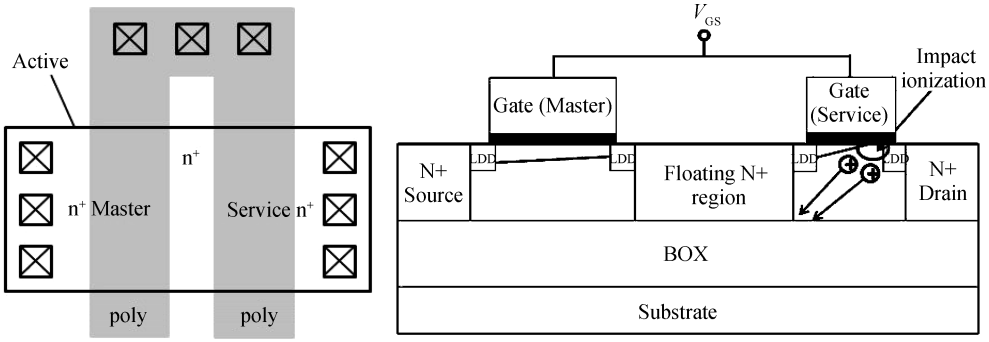

Fig. 6. Layouts of and cross-section of dual-gate PD SOI nMOSFET.

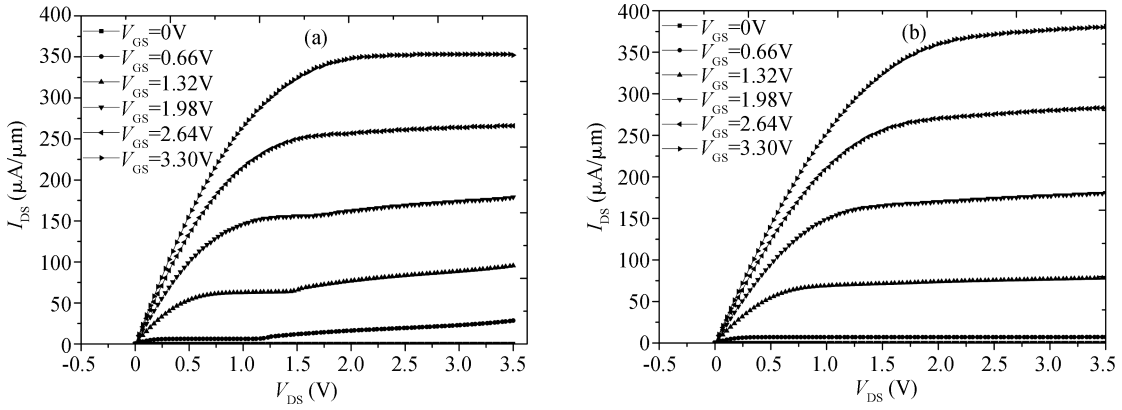

Fig. 7. I_D–V_D characteristics of 70 Å GOX single SOI nMOSFET (a) with W/L = 10/1.0 μm and (b) the kink-free dual-gate of $W/L_M/L_S$ = 10/0.75/0.25 μm.

into the floating body via direct tunneling through the GOX. That means the dual-gate can successfully eliminate the hot-carrier impact which occurs when the V_{DS} is above 1.12 V, but cannot eliminate the charges tunneling from the gate to the body which can occur even when the V_{DS} is as low as 0.6 V. In fact, the tunneling is determined by the V_G rather than V_{DS}, as long as $V_G > V_T$, such gate-induced kink occurs. Moreover, such gate-induced FBE also occurs in SOI-pMOSFET in which the hot-carrier related FBE can be neglected. Fortunately, it was found in the measurement that such gate-induced FBE can also be suppressed by slightly increasing the gate-length of the master transistor L_{GM}, because this kink is actually associated with the parasitic bipolar effect in which the tunneling charges from the gate to the body partly behaves like the base current I_B that was magnified by the lateral NPN bipolar structure (multiplied by β). Therefore as long as the gate length of the master transistor L_{GM} increases, that is, the W_B of the lateral n–p–n increases and β decreases, the FBE (thus the kink) is eliminated, and measurement shows that this is independent of the service transistor gate-length L_{GS}.

2.1. Experiments

PD SOI-MOSFET's were fabricated in the 0.13 μm SOI-CMOS process using shallow trench isolation, an 18 Å nitrided gate oxide is used for core devices and 70 Å nitrided gate oxide is used for 0.35 μm I/O devices, with 130 nm polysilicon gate and 65 nm wide nitride spacers. Process was performed on 200 mm diameter UNIBOND SOI wafers with 100 nm thick top Si and 145 nm thick buried oxide. For comparison, both normal single gate and dual-gate MOSFET's are used with a transistor width of 10 μm and different channel lengths to investigate the kink effect.

2.2. Results and discussion

Figure 7 illustrates the I_D–V_D characteristics of 70 Å GOX SOI-nMOSFET, showing single device with kink and dual-gate device with kink-free, proving that the dual-gate structure is very effective in kink-effect suppression for 70 Å GOX SOI-nMOSFET.

Unlike the 70 Å GOX devices, Figure 8 indicates that kink still occurs in the I_D–V_D curve of dual-gate 18 Å GOX nMOSFET if the channel length of the master device is smaller than 1 μm and when the LG of the master device is 2 μm, the kink is much less.

Figure 9 shows the gate-tunneling induced FBE occurring in SOI-pMOSFET when GOX is below 20 Å, where kink still occurs in the dual-gate devices with channel length of the master device smaller than 0.35 μm and disappears when master device channel length is larger than 0.35 μm.

3. Discussion

In the case of very thin GOX below 20 Å when gate-tunneling occurs[3−5], the nMOSFET's in the dual-gate can be regarded as a parasitic lateral NPN bipolar transistor shown in

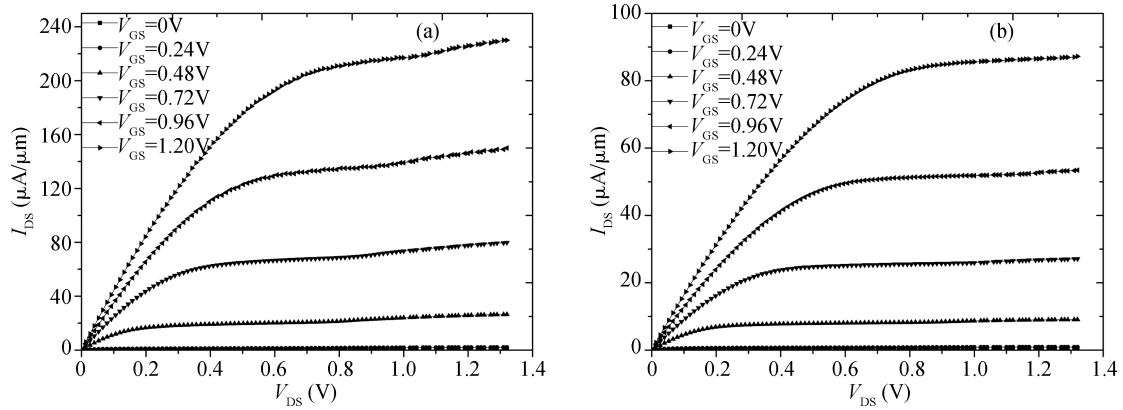

Fig. 8. I_D–V_D characteristics of 18 Å GOX SOI nMOSFET with dual-gate (a) of $W/L_M/L_S$ = 10/0.35/0.13 μm and (b) of $W/L_M/L_S$ = 10/2/0.13 μm.

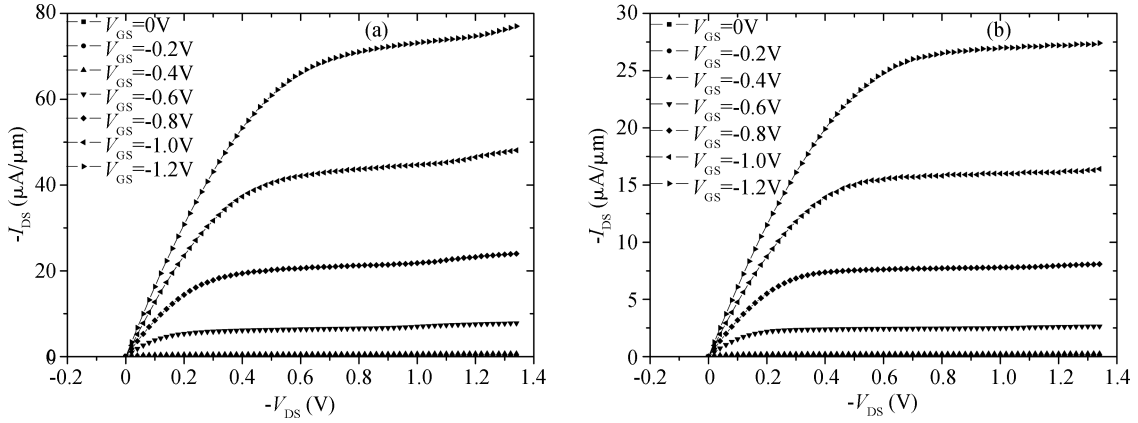

Fig. 9. I_D–V_D characteristics of 18 Å GOX SOI pMOSFET with dual-gate (a) of $W/L_M/L_S$ = 10/0.25/0.13 μm which shows kink and (b) of $W/L_M/L_S$ = 10/1/0.13 μm which is kink-free.

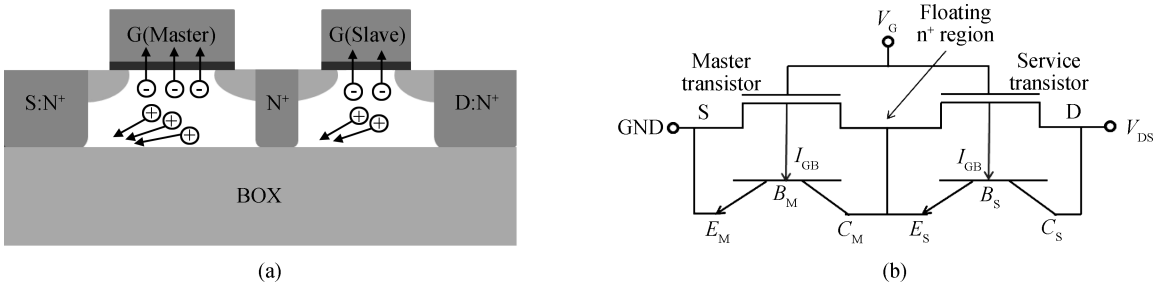

Fig. 10. (a) Cross section tunneling gate nMOSFET with dual-gate design and (b) its equivalent circuit.

Fig. 10 with its equivalent circuit on the right. In this configuration the source (S) can be considered as the emitter of the lateral parasitic bipolar NPN device of the master transistor and drain can be considered as the collector of the parasitic bipolar device of the service transistor. The floating n^+ region behaves both as the collector of the parasitic bipolar transistor of the master transistor and the emitter of the parasitic bipolar transistor of the service transistor, respectively. The both bodies can be considered as the base of the parasitic NPN bipolar transistor. The tunneling current behaves like the base current I_B that can be magnified by the lateral NPN bipolar structure (multiplied by β). The parasitic bipolar effect enhances the I_{DS} which causes the appearance of the kink in the dual-gate nMOSFETs with short channel length. As the channel length of the master transistor increases, that is, W_B of the parasitic lateral bipolar increases and β decreases. The I_{DS} contributed by the parasitic bipolar effect is eliminated so the kink disappears. The parasitic bipolar of master transistor is usually dominant. For SOI-pMOSFET with tunneling GOX, the dual-gate structure can be regarded to above in a similar way as parasitic lateral PNP bipolar transistor and the mechanism is the same.

4. Conclusion

In this study, the limitation of body-contact to suppress FBE in SOI-CMOS devices is explained in detail with quantita-

tive examples. Dual-gate structure is introduced as an alternative to using body-contacts for hot-carrier related FBE. It is also demonstrated that kink effect still occurs in dual-gate structures for both nMOSFET's and pMOSFET's when gate oxide is below 20 Å due to direct tunneling mechanisms and parasitic lateral bipolar effect. However, FBE can be suppressed as long as the gate length of the master transistor of the dual-gate is increased.

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