A low spur, low jitter 10-GHz phase-locked loop in 0.13-μm CMOS technology*

Mei Niansong(梅年松)†, Sun Yu(孙瑜), Lu Bo(陆波), Pan Yaohua(潘姚华), Huang Yumei(黄煜梅)†, and Hong Zhiliang(洪志良)

State Key Laboratory of ASIC & Systems, Fudan University, Shanghai 201203, China

Abstract: This paper presents a 10-GHz low spur and low jitter phase-locked loop (PLL). An improved low phase noise VCO and a dynamic phase frequency detector with a short delay reset time are employed to reduce the noise of the PLL. We also discuss the methodology to optimize the high frequency prescaler's noise and the charge pump's current mismatch. The chip was fabricated in a SMIC 0.13-μm RF CMOS process with a 1.2-V power supply. The measured integrated RMS jitter is 757 fs (1 kHz to 10 MHz); the phase noise is –89 and –118.1 dBc/Hz at 10 kHz and 1 MHz frequency offset, respectively; and the reference frequency spur is below –77 dBc. The chip size is 0.32 mm^2 and the power consumption is 30.6 mW.

Key words: phase-locked loop; VCO; charge pump; current mismatch

DOI: 10.1088/1674-4926/32/3/035004 **EEACC:** 2570

1. Introduction

With the fast growing demands of the wireless communication systems market, the wireless transceiver has received much attention in recent years. The phase-locked loop (PLL) is a key building block for clock generation in wireless transceiver systems. Recently, various circuit techniques to reduce jitter and suppression spur techniques of PLLs were reported in Refs. [1–3]. In Ref. [1], a fully differential charge pump (CP) and an active loop filter are used for the reduction of the CP current mismatch. Two loop filters will inevitably increase the chip area, and a 311 MHz reference clock is needed. In Ref. [2], two CP circuits are needed to suppress the spur. A special circuit is needed to reduce the spur in Ref. [3].

This paper presents the design of a low jitter PLL with low spur targeting for 802.11a/b/g applications. The PLL employs an improved VCO with a lower phase noise technique without increasing the chip area. Moreover, the key factors governing the PLL's spur and phase noises are addressed and a methodology to optimize their performances is proposed.

2. Conception and implementation

The block diagram of the PLL aimed at a 802.11a/b/g zero-IF transceiver system is shown in Fig. 1. The maximum operating frequency of the PLL is 11.61 GHz to meet the 802.11a system application. A first divider-by-2 provides the in-phase and quadrature (IQ) signals for the 802.11a system; a second divider provides the IQ signals for a 802.11b/g. To minimize noise injection, the digital and analog power and ground are separated. The jitter of the PLL is caused by the noise of its sub-blocks, such as the CP and the VCO. The out-band phase noise of the PLL is dominated by the VCO while the in-band noise is mainly contributed by the CP and the PFD[4]. In addition, the VCO and the CP are the sources of the spur. Therefore, the high performance VCO and CP are the key factors in the low jitter and spur.

2.1. VCO

The performance of the VCO will directly affect the PLL's phase noise and spur. To meet the specification of the multimode system, an ultra-wide tuning range VCO with a frequency of 9.0 to 12 GHz is required. Considering the chip area, only a single VCO is used to realize the ultra-wide tuning range. In order to reduce the phase noise of the VCO, this paper uses a tail-current source with source degeneration to substitute the conventional tail-current source, as shown in Fig. 2. According to Hajimiri theory, the phase noise of the VCO can be expressed as[5]

$$L(\Delta\omega) = 10\lg\left(\frac{\dfrac{\overline{I_{\rm n}^2}}{\Delta f}}{q_{\rm max}^2}\frac{\Gamma_{\rm rms}^2}{2\Delta\omega^2}\right), \tag{1}$$

where $\Gamma_{\rm rms}$ is the value of the impulse sensitivity function (ISF) associated with that noise source; and $q_{\rm max}$ is the maximum charge displacement across the capacitor on the drain of the tail current; and $\frac{\overline{I_{\rm n}^2}}{\Delta f}$ is the power spectral density of the parallel current noise (including not only the M3 and M4 transistor noise contribution but also the noise contribution from the tail-current source transistors M1 and M2). From the above analysis, the smaller noise of the tail-current transistor can achieve a better phase noise.

For the tail-current source transistor, the impulse sensitivity function (ISF) associated with the tail-current source has a fundamental frequency that is double the oscillation frequency. Due to this frequency doubling, the Fourier coefficients of the ISF at odd harmonics of ω_0 is zero, and therefore the noise of the tail-current source in the vicinity of the odd harmonics of ω_0 has no effect on the differential noise current, and the up-conversion of the $1/f$ noise is the most significant remaining noise component of the noisy tail current[6]. Equations (2) and (3) are the equivalent output flicker noise of the tail-current

* Project supported by the National High Technology Research and Development Program of China (No. 2009AA011605).

† Corresponding author. Email: meiniansong@fudan.edu.cn, yumeihuang@fudan.edu.cn

Received 19 August 2010, revised manuscript received 16 September 2010

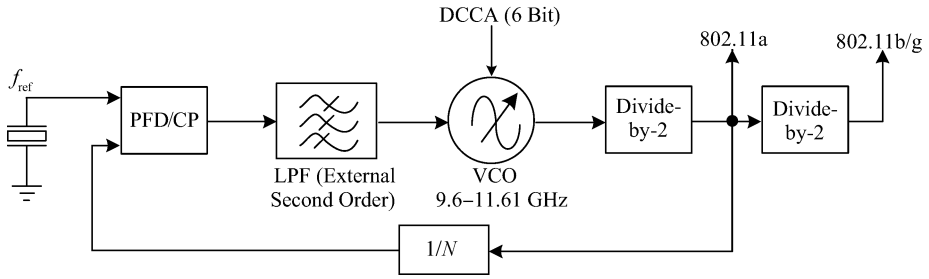

Fig. 1. Block diagram of the integer-N PLL.

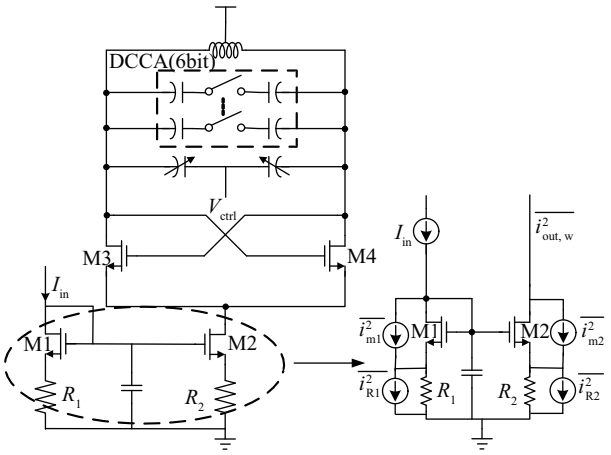

Fig. 2. Block diagram of the VCO core.

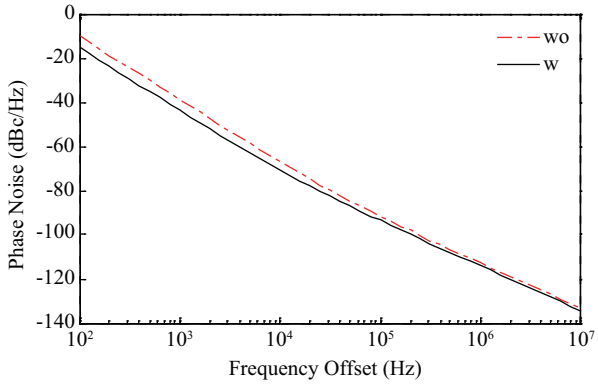

Fig. 3. Phase noise of the VCO with/without source degeneration.

source with a negative feedback resistor $\overline{i^2_{out,w,1/f}}$ and without a negative feedback resistor $\overline{i^2_{out,w0,1/f}}$, respectively,

$$\overline{i^2_{out,w0,1/f}} = \left(\frac{1}{1+g_{m2}R_2}\right)^2 \left[\overline{i^2_{m2,1/f}} + B^2\overline{i^2_{m2,2/f}}\right], \quad (2)$$

$$\overline{i^2_{out,w0,2/f}} = \overline{i^2_{m1,1/f}} + B^2\overline{i^2_{m2,2/f}}, \quad (3)$$

where B is the current mirror ratio, g_{m2} is the transconductance of transistor and M2, $\overline{i^2_{m1,1/f}}$ and $\overline{i^2_{m2,1/f}}$ are the equivalent output flicker noise of the transistors M1 and M2.

According to Eqs. (2) and (3), the flicker noise of the current source with source degeneration is reduced by the feedback factor $g_{m2}R_2$. However, large R_2 will force the transistor into the linear region, thereby worsening the phase noise VCO. So careful design is needed. The VCO gain K_{VCO} will affect the spur of the PLL, and the relationship between the spur and the VCO gain K_{VCO} is given by[2]

$$\frac{A_{sput}}{A_{carrier}} = \frac{1}{2}\frac{K_{VCO}V_m}{2\pi f_{ref}}, \quad (4)$$

where V_m is the amplitude of the ripple and f_{ref} is the reference. From Eq. (4), the amplitude of the spur is proportional to the gain of the VCO, so a smaller K_{VCO} will achieve better spur performance. Thus, a 6-bit digital controlled capacitor array (DCCA) is adopted to cover the wide frequency range while maintaining a lower VCO frequency tuning gain in this architecture. Figure 3 shows the phase noise simulation results (VCO worked at 10.322 GHz). The figure shows that the improved VCO has good phase noise; the phase noise with/without source degeneration is –70.37/–66.6 dBc/Hz, –113.9/–112.4 dBc/Hz at 10 kHz and 1 MHz frequency offset, respectively.

2.2. Prescaler

A high frequency prescaler is one of the key blocks in the PLL. Generally, it works at the highest frequency of the system and consumes a significant portion of the total power, and its phase noise will affect the frequency synthesizer's phase noise directly. To meet the specification of the PLL, the prescaler needs to be able to operate properly from 8 to 13 GHz, and maintain low phase noise. A high speed broadband prescaler with a balanced dynamic load is shown in Fig. 4[7]. The key factor limiting the speed of the prescaler is the output RC constant in tracking mode. The internal signal swing and the current leakage in the latching mode are the two factors that would limit the operating frequency range. In this architecture, a complementary driven PMOS transistor is used as a load to increase the speed and operating frequency range of the prescaler. On the other hand, in order to enhance the sensitivity of the prescaler, the self-oscillator frequency f_{SO} of the prescaler has to be slightly higher than the half of the input frequency f_{in}[8]. The first stage prescaler contributes the out-band phase noise of the PLL. The phase noise of the divider can be written as[9]

$$L(\overline{\omega}_m) = \frac{2\pi^2 f_{out}^2}{I_B/C_L^2} S_V^{folded}(\omega_m), \quad (5)$$

where $S_V^{folded}(\omega_m)$ is the PSD of the output voltage noise folded in the Nyquist band from 0 to $\frac{\omega_{out}}{2}$ and $\frac{I_B}{C_L}$ is the slope of the output voltage at the zero crossing.

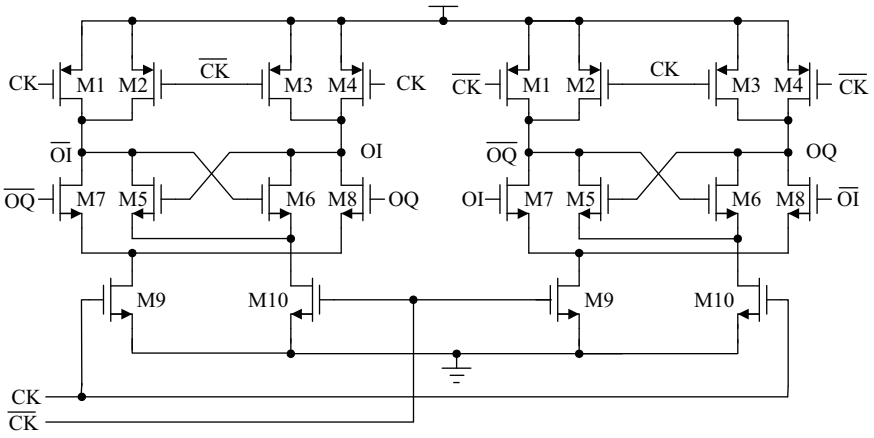

Fig. 4. Block diagram of the prescaler.

According to Eq. (5), a small internal parasitic capacitor of the output ($C_{\rm L}$) or large current ($I_{\rm B}$) achieves low phase noise. Increasing the current will reduce the phase noise, but the power consumption will increase as well.

2.3. PFD and charge pump

The non-ideal characteristics of the CP and the PFD severely deteriorate the PLL's in-band phase noise and spur. The amount of the reference spur in the 3rd-order PLL is approximately written by[9]

$$P_{\rm r} = 20\lg\frac{\sqrt{2}\dfrac{I_{\rm CP}R}{2\pi}\phi_\epsilon K_{\rm VCO}}{2f_{\rm ref}} - 20\lg\frac{f_{\rm ref}}{f_{\rm p1}}\ \ {\rm dBc}, \qquad (6)$$

where R and $f_{\rm p1}$ are the resistance and the pole frequency in the loop filter, respectively, and ϕ_ϵ is the phase offset caused by the CP and the PFD.

From Eq. (6), the spur is proportional to the phase offset and the loop bandwidth. One intuitive approach is to adopt a small loop bandwidth, but this will increase the setting time and the chip area. Another method is to reduce the phase offset. Figures 5 and 6 show the structures of the CP and the PFD, respectively[10, 11]. The phase offset is mainly caused by the charge pump's current mismatch. In order to reduce the spur, various papers have mainly focused on discussing the CP's static current mismatch and ignored the CP's dynamic current mismatch[10, 12]. The amount of the phase error caused by the static current mismatch is given by

$$|\phi_{\varepsilon,\rm static}| = 2\pi\frac{T_{\rm on,static}}{T_{\rm ref}}\frac{\Delta I}{I_{\rm static}}, \qquad (7)$$

where $T_{\rm on,static}$ is the turn on time when the CP works on static, $\frac{\Delta I}{I_{\rm static}}$ is the mismatch of the static current and $T_{\rm ref}$ is the reference clock period for the PFD. A rail-to-rail error amplifier is used in Fig. 5 to achieve a perfect static current match. The simulation results show that the static current deviation of the CP does not exceed 1% over the output voltage from 0.3 to 0.8 V.

Compared with a traditional PFD, the dynamic phase frequency detector has a very short reset time. The simulation results show that the static turn on time is less than 100 ps when the loop is locked. For example, let us assume $I_{\rm CP} = 80\ \mu$A,

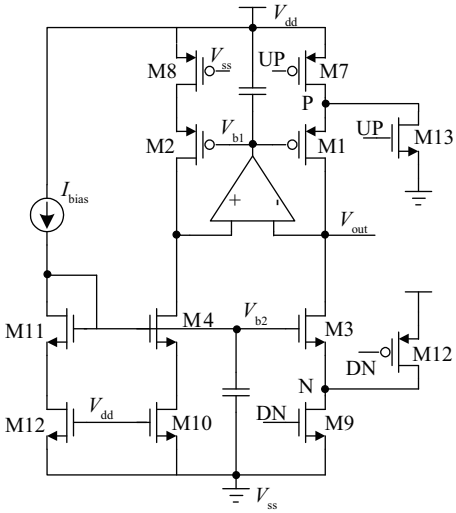

Fig. 5. Block diagram of the charge pump.

$K_{\rm VCO} = \frac{350\ {\rm MHz}}{V}$, $\frac{\Delta I}{I_{\rm static}} = 1\ \%$, $T_{\rm on,static} = 100$ ps, $R = 27\ {\rm k}\Omega$ and $T_{\rm ref} = 100$ ns, substituting these values into Eqs. (6) and (7). The spur caused by the static current mismatch is about –93 dBc. From the above calculation, the static phase offset contribution to the spur is very small; the system spurious is mainly caused by a dynamic current mismatch.

The amount of the phase error caused by a dynamic current mismatch can be expressed as

$$\phi_{\varepsilon,\rm dynamic} = 2\pi f_{\rm ref}\frac{\Delta{\rm dynamic}}{I_{\rm static}}, \qquad (8)$$

where

$$\Delta Q_{\rm dynamic} = \max\left\{\left|\int_0^{{\rm IT_r}} I_{\rm M3}(t){\rm d}t - \int_0^{{\rm IT_r}} I_{\rm M1}(t){\rm d}t\right|, \left|\int_0^{{\rm IT_f}} I_{\rm M3}(t){\rm d}t - \int_0^{{\rm IT_r}} I_{\rm M1}(t){\rm d}t\right|\right\}. \qquad (9)$$

According to Eqs. (8) and (9), the effective dynamic phase error is related to the dynamic response of the current and the dynamic time. The dynamic current mismatch is caused by the different electronic characteristic of the PMOS and NMOS

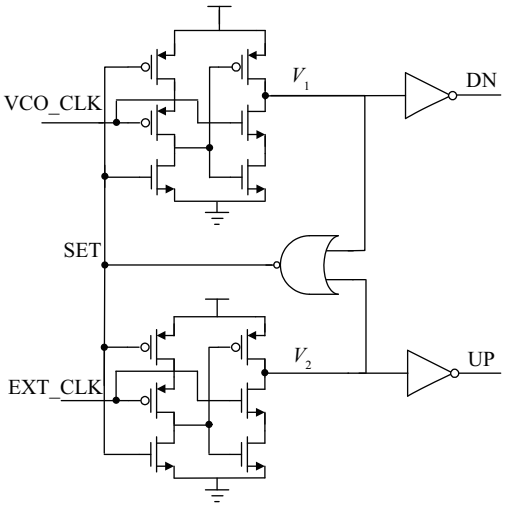

Fig. 6. Block diagram of the PFD.

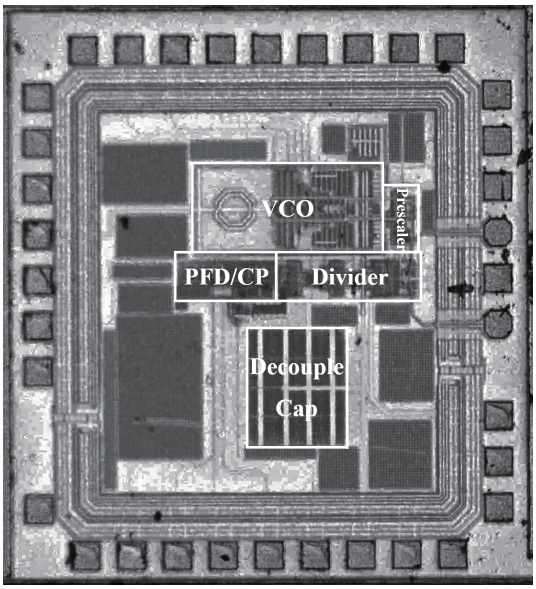

Fig. 7. Chip micrograph of the PLL.

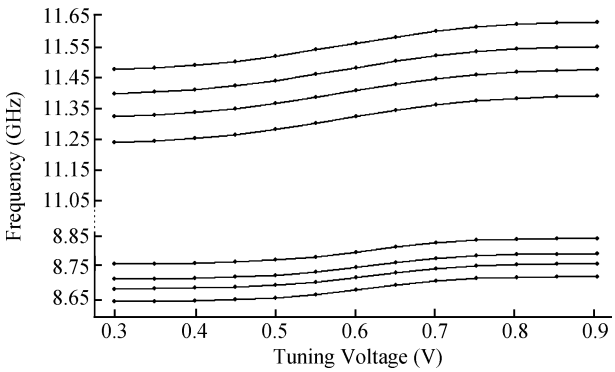

Fig. 8. Measuring the tuning range of the VCO.

transistor (such as the electron mobility and the threshold voltage). The current of M1 and M3 is asymmetric during the dynamic time. There are two methods to reduce the dynamic phase error. First, properly choose the size of the transistor M7, M9, M12 and M13 to reduce the charge and discharge duration of the N and P point (charge time decision by transistor M7, M12, and discharge time decision by M9 and M13). Second, properly adjust the voltage of V_{b1} and V_{b2} to reduce the mismatch of the dynamic current.

On the other hand, the CP contributes the majority of the in-band noise of the PLL[4]. The CP's equivalent output noise power not only corresponds to the noise of the CP but also depends on the PFD on-time under PLL locked status. The equivalent output noise power $\overline{i^2_{n,out}}(j\overline{\omega})$ can be expressed as

$$\overline{i^2_{n,out}}(j\overline{\omega}) = \overline{i^2_{n,cp}}(j\overline{\omega}) * S_{on}(\omega), \tag{10}$$

where $\overline{i^2_{n,out}}(j\overline{\omega})$ is the noise power of the CP, * is a convolution operator and $S_{on}(\omega)$ is the Fourier function of the PFDs on-time under PLL locked status.

$$S_{on}(\omega) = \sum_{-\infty}^{-\infty} \alpha_n^2 \delta(\omega - \omega_0), \tag{11}$$

where $n\overline{\omega}_0$ is the harmonic angular frequency, α_n is the Fourier coefficient and

$$\alpha_n = \frac{\sin\dfrac{n\pi T_{on} f_{ref}}{2}}{n\pi}. \tag{12}$$

.

From Eqs. (10) and (11), reduction of the noise of the CP and the PFD on-time under PLL locked status is good to reduce the in-band phase noise.

3. Experimental results

The circuit has been integrated into 0.13 μm CMOS technology. Figure 7 shows the chip micrograph. The core of the PLL occupies an area of 0.32 mm^2. The measured output range of the ultra-band VCO is plotted in Fig. 8. The VCO output frequency ranges from 8.65 to 11.62 GHz with a good overlap between adjacent characteristics.

Constrained by the testing environment, all test results are achieved from a divide-by-2 circuit. Figure 9 shows the spectrum of the PLL locked to a 10MHz reference clock at the 5.12 GHz output. The reference spurs are –77.5 dBc. The phase noise performance of the PLL is shown in Fig. 10. The spot phase noise is –89 dBc/Hz and –118 dBc/Hz offset from the carrier frequency of 10 kHz and 1 MHz, respectively. The integrated RMS jitter over the measured band (1 kHz–10 MHz) is 757 fs. Table 1 shows a performance summary and comparison of the frequency synthesizer with others in the literature.

4. Conclusions

This paper introduces a design of a low phase noise and low spur 10 GHz clock generator in 0.13 μm CMOS technology. A low phase noise and a charge pump with a minimal dynamic current mismatch were adopted to reduce the phase noise and the spurious level of the PLL. According to the testing results, the integrated RMS jitter is 757 fs and the spur is –77.5 dBc. Only one VCO was used for wideband application.

Table 1. Performance summary and comparison.

Parameter	Ref. [1]	Ref. [13]	Ref. [14]	This work
Process (μm CMOS)	0.12	0.18	0.13	0.13
Power consumption (mW)	35	34	34	30.6
Ref. freq. (MHz)	311	20	N. A	10
Output frequency (GHz)	3.11	10	5.2	5.12
RMS jitter (ps)	0.86	N. A	0.81	0.76
Phase noise @ 1 MHz (dBC/Hz)	–113	–102	–117	–118.1
Ref. spur (dBc)	N.A	< -48	N.A	–77.5
VCO range (GHz)	N.A	8.67–10.12	4.4–5.5	8.6–11.65
Supply voltage (V)	1.5	1.8	1.2	1.2

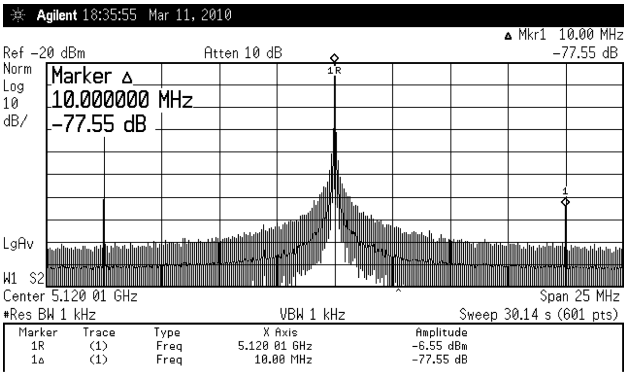

Fig. 9. PLL output spectrum (after divider).

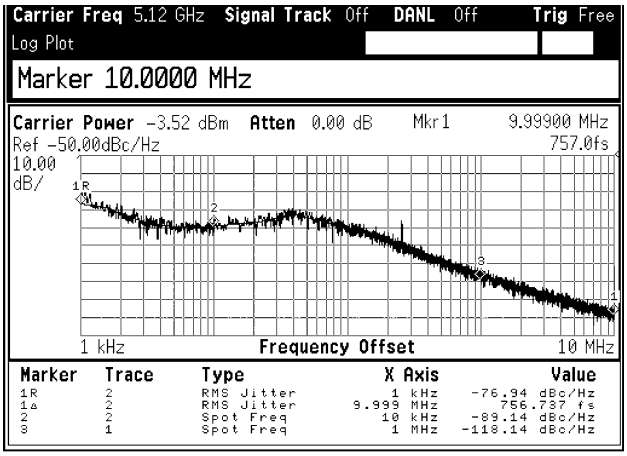

Fig. 10. PLL phase noise (after divider).

Except for the low pass filter, the synthesizer is completely integrated. The size of the core is about 0.32 mm^2. A 2nd order passive loop filter is adopted. The total value of the capacitor is 211 pF and the resister is 27 kΩ, which is easy to integrate.

References

[1] Dalt N D, Sandner C A. A subpico-second jitter PLL for clock generation in 0.12-μm digital CMOS. IEEE J Solid-State circuits, 2003, 38(7): 1275

[2] Kuo C Y, Chang J Y, Liu S I. A Spur-reduction technique for a 5-GHz Frequency synthesizer. IEEE Trans Circuits Syst I: Regul Pap, 2006, 53(3): 526

[3] Liang C F, Chen H H, Liu S L. Spur-suppression techniques for frequency synthesizer. IEEE Trans Circuits Syst I: Regul Pap, 2007, 54(8): 653

[4] Riley T A D, Filiol N M, Du Q H, et al. Techniques for in-band phase noise reduction in delta sigma synthesizer. IEEE Trans Circuits Syst II: Analog and Digital Signal Processing, 2003, 50(11): 794

[5] Hajimiri A, Lee T H. A general theory of phase noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(5): 179

[6] Hajimiri A, Lee T H. Design issues in CMOS differential LC oscillators. IEEE J Solid-State Circuits, 1999, 34(5): 717

[7] Lei Y, Koukab A, Declercq M. Design and optimization of CMOS prescaler. Research in Microelectronics and Electronics, 2005, 1: 129

[8] Singh U, Green M. Dynamics of the high-frequency CMOS dividers. IEEE International Symposium on Circuits and Systems, 2002, 5: 421

[9] Levantino S, Romano L, Pellerano S, et al. Phase noise in digital frequency dividers. IEEE J Solid-State circuits, 2004, 39(5): 775

[10] Lee J S, Keel M S, Lim S, et al. Charge pump with perfect current matching characteristics in phased-locked loops. IEEE Electron Lett, 2000, 36: 1907

[11] Kim S, Lee K, Moon Y, et al. A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL. IEEE J Solid-State Circuits, 1994, 32(5): 691

[12] Hwang M S, Kim J, Jeong D K. Reduction of pump current mismatch in charge-pump PLL. IEEE Electron Lett, 2009, 45(3): 135

[13] Lin T H, Lai Y J. An agile VCO frequency calibration technique for a 10-GHz CMOS PLL. IEEE J Solid-State Circuits, 2007, 42(2): 340

[14] Chuen T C, Chen W H., Huang D R. A 0.13 μm CMOS $\Delta\Sigma$ fractional-N synthesizer for WiMAX application. Microwave Integrated Circuits Conference, 2009: 543