A millimeter wave large-signal model of GaAs planar Schottky varactor diodes*

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Abstract: A millimeter wave large-signal model of GaAs planar Schottky varactor diodes based on a physical analysis is presented. The model consists of nonlinear resistances and capacitances of the junction region and external parasitic parameters. By analyzing the characteristics of the diode under reverse and forward bias, an extraction procedure of all of the parameters is addressed. To validate the newly proposed model, the PSVDs were fabricated based on a planar process and were measured using an automatic network analyzer. Measurement shows that the model exactly represents the behavior of GaAs PSVDs under a wide bias condition from –10 to 0.6 V and for frequencies up to 40 GHz.

Key words: GaAs; PSVDs; large-signal model; parameter extraction

DOI: 10.1088/1674-4926/32/3/034002 **EEACC:** 1350H; 2520D; 2570

1. Introduction

In the sphere of monolithic microwave integrated circuits, the design of nonlinear circuits, such as a voltage controlled oscillator[1], a phase shifter[2] and nonlinear transmission lines[3−6], is an important issue. Planar Schottky varactor diodes (PSVDs) are commonly used in nonlinear circuits. Here, the varactor diode was realized using wet etching to form a mesa structure. Unlike the surface channel varactor[7], these diodes do not require air bridges. As a result, PSVDs are less expensive to produce than surface channel varactor diodes. However, PSVDs have not been widely used due to the inaccurate microwave frequency of large signal models.

The large signal model is a nonlinear model of the device, which developed nonlinearity, such as nonlinear resistance and capacitance, characterized by the I–V and C–V equations. In addition, the parasitics from the geometry of the device are included. Therefore, the large signal model is closely related to the fabrication process and the layout design of the device. The accuracy of the large signal model depends on the exactitude of the characteristic parameters, such as the nonlinear elements under each bias, extracted by the measured S parameters under corresponding bias. Lucyszyn[8] presented a large signal model of a Schottky diode based on the process of the MESFET. However, it is not suitable for the planar Schottky diode process, which is used in our paper.

In this paper, a new millimeter wave large signal model of the planar Schottky varactor diode is presented. The model consists of nonlinear reverse and forward bias intrinsic elements and extrinsic parasitic elements, which are determined by DC and S parameters measurement. The result is a large signal model, which is accurate, well into the millimetric frequency range, with a reverse bias of –10 V and a forward bias of 0.6 V applied.

2. Large-signal model of the PSVD

The schematic diagram of the PSVD with equivalent electrical components is shown in Fig. 1. When the diode is forward biased and is driven above the build-in voltage (V_{bi}), the forward current is increased exponentially. The junction region can be represented by a resistance (R_j) dependent on the voltage. When it is reversely biased, the depletion region of the barrier layer becomes wider and the barrier becomes higher, so the reverse current is very small. The junction region behaves as a capacitance (C_j) dependent on the reverse voltage.

The large-signal model of the PSVD is shown in Fig. 2. C_j and R_j represent the junction capacitance and resistance, respectively. R_s represents the parasitic series resistance. As shown in Fig. 1, this consists of three parts: R_p, the ohmic contact resistance; R_d, the equivalent resistance of the undepletion resistance; and R_N, the parasitic resistance of the n^+ layer. R_p and R_N are independent of the voltage. Since the width of the undepletion region of the active layer is modulated by the volt-

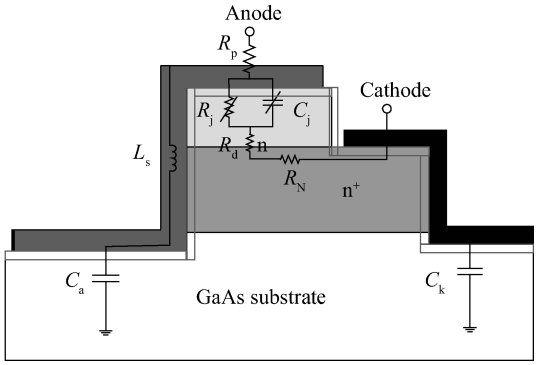

Fig. 1. Schematic diagram of the PSVD with equivalent electrical components.

* Project supported by the National Natural Science Foundation of China (No. 60806024).

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Received 19 August 2010, revised manuscript received 12 October 2010

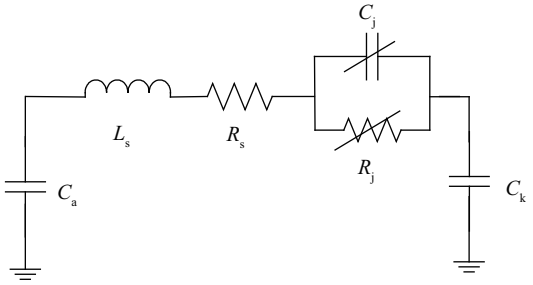

Fig. 2. Large-signal model of the PSVD.

age, the R_d varies with the bias. However, the absolute values and the variation range of the R_d are small. In this paper, it is considered constant to applied voltage without prejudice to the accuracy of our model. We use R_s to represent the summation of R_p, R_d and R_N. L_s represents the parasitic inductance of the anode and cathode electrodes. C_a and C_k are the parasitic and bias-independent capacitances of the anode to ground and the cathode to ground, respectively.

For reverse and forward bias, when the value of the applied voltage was below the build-in voltage V_{bi}, the junction region of the diode can be seen as a parallel plate capacitor. With the reverse bias increasing, the depletion region in the active layer slowly extends vertically down the buffer layer (n^+ layer). As a result, the capacitance decreases, which can provides a large tuning capacitance ratio. The capacitance can be written as[9]

$$C_j = \frac{C_{j0}}{\left(1 + \left|\frac{V}{V_{bi}}\right|\right)^M}, \tag{1}$$

where C_{j0} is the zero-bias diode capacitance, V_{bi} is the built-in voltage, and M is the grading coefficient, and its ideal values is 0.5 for the uniform doping under the junction. However, lateral depletion towards the cathode electrodes is usually considered, so M always deviates from its original value.

For the forward bias above the built-in voltage, the junction region of the diode can be seen as a variable resistance. The current of the diode can be defined as

$$I = I_s\left(\exp\frac{qV}{nKT} - 1\right), \tag{2}$$

where I_s is the current of the saturation of the diode, n is the non-ideality factor, K is Boltzmann constant and V is the applied voltage.

3. Extraction of parameters

3.1. Extraction of parasitic and junction capacitances

The junction nonlinear resistance can be neglected for the bias lower than the built-in voltage V_{bi}. The influences of the parasitic resistances R_s and inductances L_s can be ignored for lower frequencies. As a result, the imaginary parts of the Y parameters can be written as

$$\mathrm{Im}\,(Y_{11}) = \omega\left(C_a + C_j\right), \tag{3}$$

$$-\mathrm{Im}\,(Y_{12}) = -\mathrm{Im}\,(Y_{21}) = \omega C_j, \tag{4}$$

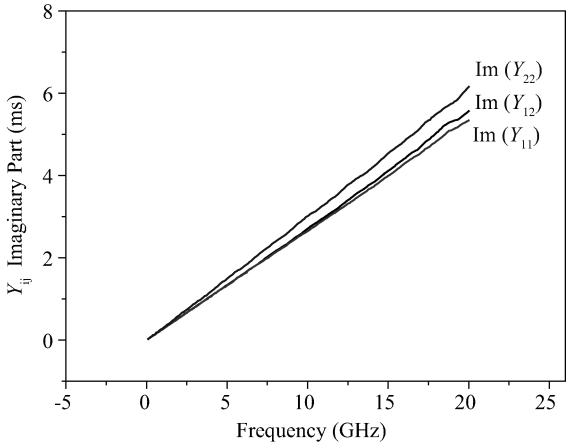

Fig. 3. Evolution of the Y parameters' imaginary parts versus frequencies, voltage = –10 V.

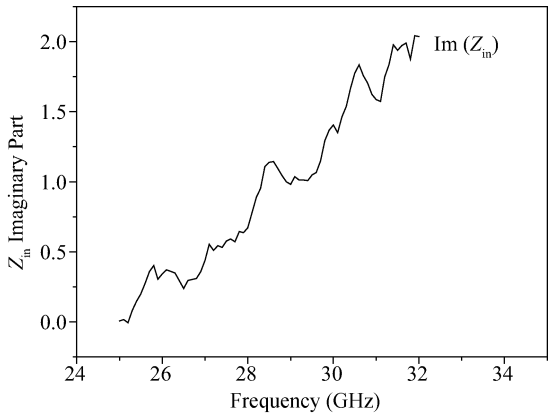

Fig. 4. Evolution of the Z_{in} parameters' imaginary parts versus frequencies, voltage = 0.7 V.

$$\mathrm{Im}\,(Y_{22}) = \omega\left(C_k + C_j\right). \tag{5}$$

The expressions have shown that the imaginary parts of the Y parameters increase linearly versus frequency. As shown in Fig. 3, the theoretical expressions (3)–(5) are in quite good agreement with experimental findings. To obtain these figures, the S parameters of the device were measured using the Agilent E8363B network analyzer and then transformed into Y parameters using the well-known translation formulas after de-embedding. These figures show a linear evolution of the Y parameter's imaginary parts. However, the plots of the Y_{12} and Y_{11} are almost coincident, so it is difficult to extract the values of the C_a from the plots. The C_a can be deduced from the C_k by multiplying by the area ratio of the cathode pad to anode pad. It is easily verified that the two (C_a and C_k) capacitances are independent of the bias when the voltage is lower than the built-in voltage V_{bi}. Varying the applied voltage, the characteristics of the junction capacitances C_j versus the bias can be obtained. Then the parameters C_{j0}, V_{bi} and M in Eq. (1) can be determined from the curves of the junction capacitance versus the bias.

3.2. Extraction of the resistances and inductances

When the diode is driven above the built-in voltage V_{bi}, the forward current increases exponentially and the junction resistance decreases dramatically. The junction capacitance C_j can be negligible compared with the junction resistance R_j. At low frequencies (< 2 GHz), the parasitic capacitances C_a and C_k and the parasitic inductance have little influence on the diode, so the diode is purely resistance, so we have[10]

$$Z_{in} = R_s + R_j. \tag{6}$$

The characteristics of the R_j versus voltage can be obtained by the DC measurement of the diode, then the values of the R_s can be calculated by Eq. (6). Extending the frequency range at the same bias, the influence of the inductance cannot be neglected anymore, so we have

$$\mathrm{Im}(Z_{in}) = \omega L_s. \tag{7}$$

L_s can be determined from Eq. (7). As shown in Fig. 4, the imaginary parts of the experimental Z_{in} parameters biased at 0.7 V increase linearly versus frequencies from 25 to 30 GHz, which is in quite good agreement with Eq. (7).

4. Experimental results

The GaAs epilayers were grown by molecular beam epitaxy (MBE) on a GaAs semi-insulating substrate, which consisted of a 1-μm-thick conductivity buried n^+-type layer and a 0.6-μm-thick n-type active layer. The dopant in the epilayers was silicon. To begin the process, a 0.7-μm-thick mesa was formed from the active layer to the n^+-type layer by wet etching using a solution of $H_3PO_4/H_2O_2/H_2O$. The ohmic contacts were then defined by lift-off of e-beam evaporated Ni/Ge/Au/Ge/Ni/Au followed by annealing. After annealing, the Schottky contacts were defined by lift-off of e-beam evaporated Ti/Pt/Au. Using the solution of $H_3PO_4/H_2O_2/H_2O$, wet etching removed the GaAs materials from the n^+-type layer to the substrate layer surrounding the ohmic contact regions, thus isolating the devices. The whole surface of the wafer was then passivated by depositing 3000-Å-thick silicon nitride. Using reactive ion etching, windows were opened over the metal contacts. Finally, the pads and fingers were electroplated to connect to Schottky or ohmic metal contacts.

The isolation between devices was formed by the mesa, which was etched into the semi-insulation substrate layer. So the low parasitical capacitances and resistances can be obtained. The diode with the area of 160 μm^2 was designed and fabricated. This is the diode that we used to verify our model. A photo of the device is shown in Fig. 5.

The DC characteristics of the diode were measured using an HP 4155 semiconductor parameter analyzer. The measured I–V characteristics biased from –0.5 to 1 V are shown in Fig. 6. The extracted I_s and n are 1.71×10^{-15} A and 1.05, respectively.

The S-parameters were measured from 0.1 to 40 GHz at discrete bias points from –10 to 0.6 V using a probe station and an Agilent PNA E8363B automatic network analyzer. The S parameters were de-embedded then transferred into Y parameters. Using the imaginary parts of the Y parameters at zero bias for frequencies from 0.1 to 20 GHz and following the procedure described above, C_a and C_k were derived. These parasitic parameters were calculated to be 1 and 6.8 fF. Varying the reverse bias, the characteristics of C_j versus the bias from –10 to 0.6 V were obtained, as shown in Fig. 7. By fitting the curves, the parameters C_{j0}, V_{bi} and M described in Eq. (1) were calculated to be C_{j0} = 124 fF, V_{bi} = 0.73 V and M = 0.4.

The input impedances of the Schottky diode biased above

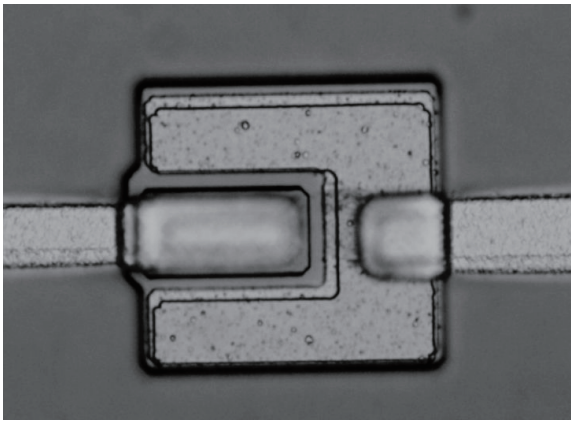

Fig. 5. Photo of the PSVD chip.

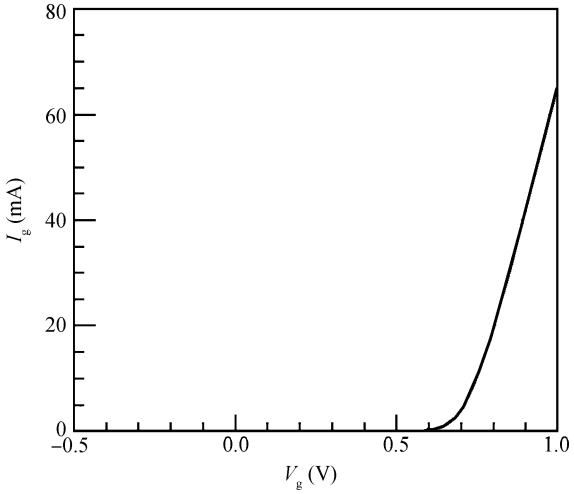

Fig. 6. The measured current characteristics of the diodes.

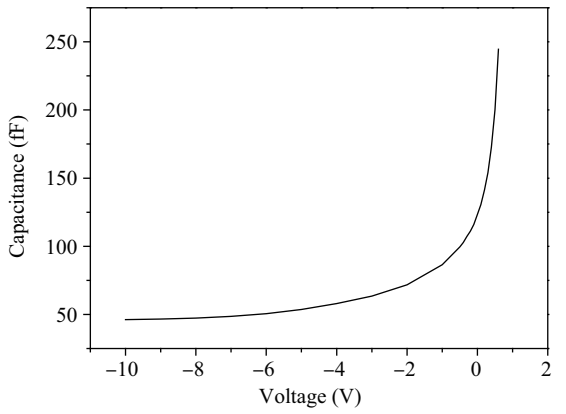

Fig. 7. Characteristic of the C_j versus bias from –10 to 0.6 V.

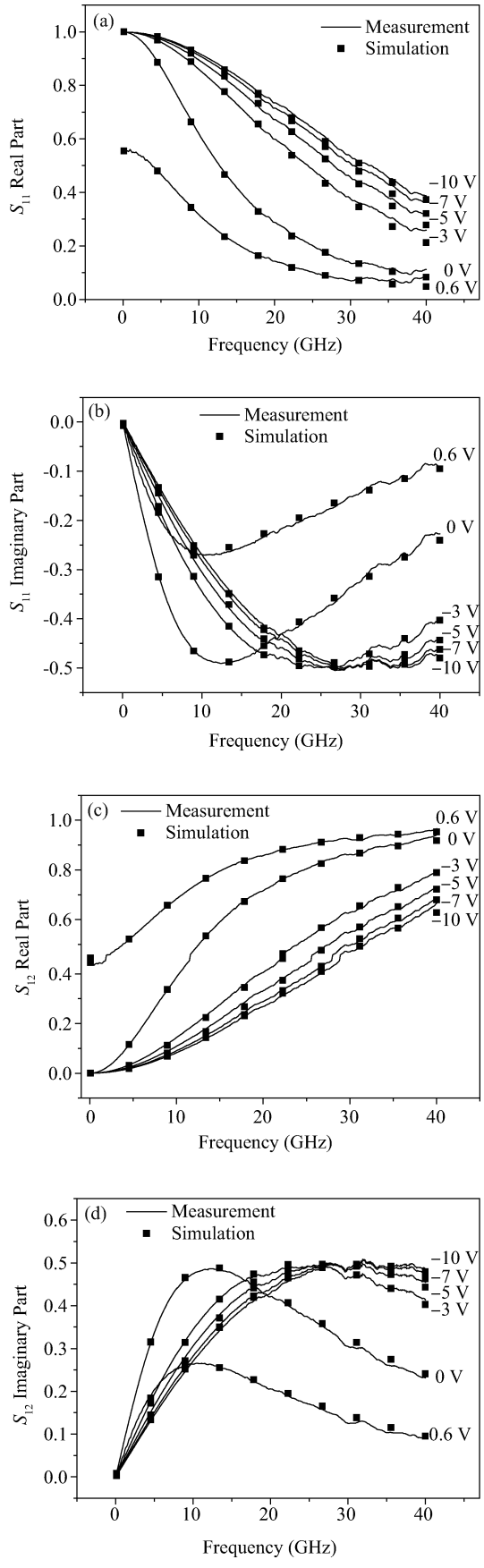

Fig. 8. Comparison of the measured and simulated S-parameters of the PSVD under voltage from –10 to 0.6 V. (a) Real parts of the S_{11}. (b) Imaginary parts of the S_{11}. (c) Real parts of the S_{12}. (d) Imaginary parts of the S_{12}.

Table 1. Parameters of the equivalent circuit model of the PSVD.

Name	Description	Value
C_a	Anode pad to ground parasitic capacitance	1 fF
C_k	Cathode pad to ground parasitic capacitance	6.8 fF
R_s	Series parasitic resistance	0.58 Ω
L_s	Series parasitic inductance	24 pH
C_{j0}	Zero-bias junction capacitance	124 fF
V_{bi}	build-in voltage	0.73 V
M	grading coefficient	0.4
I_s	Saturation current of the diode	1.71×10^{-15} A
n	Non-ideal factor	1.05

V_{bi} in the low frequency limit is described by Eq. (6), hence the R_s can be determined. Then, we can extract L_s from the input impedance over a wide frequency band at the same bias. The parameters R_s and L_s have been found to be 0.58 Ω and 24 pH. All of the model parameters are shown in Table 1 for the diode with an area of 160 μm^2. The symbolically defined device (SDD) tools in the advance design system (ADS) from Agilent were used to define the nonlinear components of the diode, C_j and R_j.

In order to validate the model, the large-signal model with the extracted parameters was simulated in ADS from 0.1 to 40 GHz. Comparison between simulation and measurement revealed that the developed model agrees closely with experimental measurement over a wide range of frequency and under a wide operation bias range from –10 to 0.6 V, as shown in Fig. 8.

5. Conclusions

A millimeter wave large-signal model of the PSVD has been presented. The model consists of nonlinear components, R_j and C_j, and parasitic parameters, C_a, C_k, R_s and L_s. The characteristics of the junction region of the diode under reverse and forward bias have been analyzed. The process of parameter extraction is convenient to manipulate. All of the parameters can be determined from DC and S parameter measurement results. Excellent agreements are found between experimental measurement and model simulation under a wide operation bias range from –10 V to 0.6V and for frequencies up to 40 GHz.

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