A 4th-order reconfigurable analog baseband filter for software-defined radio applications*

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Abstract: This paper presents a 4th-order reconfigurable analog baseband filter for software-defined radios. The design exploits an active-RC low pass filter (LPF) structure with digital assistant, which is flexible for tunability of filter characteristics, such as cut-off frequency, selectivity, type, noise, gain and power. A novel reconfigurable operational amplifier is proposed to realize the optimization of noise and scalability of power dissipation. The chip was fabricated in an SMIC 0.13 μm CMOS process. The main filter and frequency calibration circuit occupy 1.8 $\times$ 0.8 mm^2 and 0.48 $\times$ 0.25 mm^2 areas, respectively. The measurement results indicate that the filter provides Butterworth and Chebyshev responses with a wide frequency tuning range from 280 kHz to 15 MHz and a gain range from 0 to 18 dB. An IIP3 of 29 dBm is achieved under a 1.2 V power supply. The input inferred noise density varies from 41 to 133 nV/$\sqrt{\text{Hz}}$ according to a given standard, and the power consumptions are 5.46 mW for low band (from 280 kHz to 3 MHz) and 8.74 mW for high band (from 3 to 15 MHz) mode.

Key words: reconfigurable; software-defined radio; baseband filter; digital assistant; high linearity

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1. Introduction

The rapid development of wireless communication systems has introduced a multitude of standards, such as GSM, Bluetooth, TD-SCDMA, WCDMA, DVB, WLAN, and LTE. Since cost and power consumption have been the most important factors considering prize and battery duration, a single mobile handset that can support a lot of existing and emerging wireless standards will be more desirable for consumers.

A software-defined radio (SDR) transceiver is one of the best solutions to implement such a mobile handset under these power and cost limitations[1, 2]. Based on a single hardware platform, the SDR transceiver can be reconfigurable and flexible to comply with multi-standard requirements just by reprogramming the software.

A reconfigurable analog baseband filter with a digital assistant is required to separate the desired signal from the unwanted ones (blockers) in the SDR receiver. In order to support multiple standards, the characteristics of the baseband filter (i.e. cut-off frequency, selectivity, type, noise, gain and power) should be adjusted to fulfill the demand of a specific standard, because each standard has a different signal bandwidth and modulation scheme.

In recent years, some attempts at a reconfigurable filter have been made for multi-mode applications[5, 6]. A fully reconfigurable filter architecture that employs sub-blocker (resistors, capacitors and op-amplifiers) arrays and a digital assistant was proved to be the best candidate to implement a baseband filter for SDR applications. However, filter implementations based on the identical op-amplifiers[5] still suffer much from the flick noise for narrow-bandwidth applications. Another filter solution based on op-amplifier arrays[6] achieve a high level of flexibility, but the stringent requirements of flick noise and mismatch still need a large amount of silicon area and power consumption.

Here, to overcome the difficulties mentioned above, a novel programmable operational amplifier is proposed to optimize noise and power consumption. A 4th-order baseband filter with improved reconfigurable architecture is implemented to achieve a higher level of flexibility for SDR receiver.

2. System requirements for SDR baseband filter

In order to comply with the signal bandwidths from the GSM to WLAN 802.11a/b/g, the cut-off frequency of the baseband filter should cover a wide frequency range. Furthermore, there are many different data rates even for a specific standard, so the cut-off frequencies of the baseband filter should be abundant to support all of the data rates and channel bandwidths in the SDR receiver.

According to the requirements of many wireless standards, the baseband filter needs to handle a lot of strong out-of-band blockers that have been amplified by the RF front-end. Therefore, the baseband filter is required to achieve a high linearity performance even under the worst-case conditions. Though a G_{m}–C filter has some flexible degree in frequency tuning, poor linearity is still a limitation factor even some linearization techniques have been employed under low supply voltage[3, 4]. An active-RC filter is a better choice because of its intrinsic high linearity advantage compared to the G_{m}–C filter.

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Table 1. Specification requirement for an analog baseband filter in SDR direct-conversion receiver.

Standard	Cut-off freq. (MHz)	Min. stop-band attenuation (dB)	In-band integrated noise (μV_{rms})	IIP3 (dBm)	Gain (dB)
GSM	0.28	30 @ 0.44 MHz	68	20.4	0–18
Bluetooth	0.6	28 @ 1.2 MHz	72	17.8	0–18
TD-SCDMA	0.84	38 @ 3.2 MHz	78	19.6	0–18
WCDMA	2.2	35 @ 8 MHz	82	22.2	0–18
DVB-H	4	38 @ 16 MHz	120	18	0–18
LTE	10	40 @ 40 MHz	142	17.4	0–18
WLAN a/b/g	11	42 @ 44 MHz	148	21.5	0–18

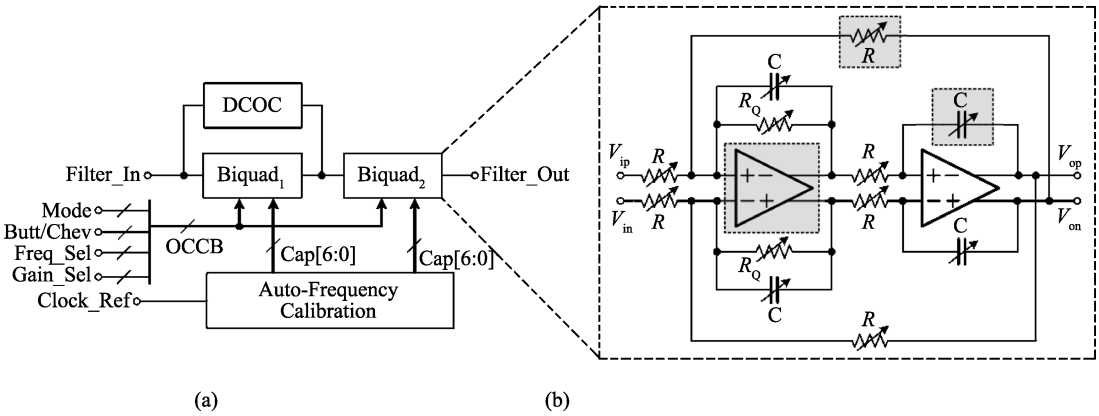

Fig. 1. (a) Filter top-level architecture. (b) Biquad.

Since each standard has a different modulation scheme and adjacent channel selectivity (ACS), the selectivity and phase response of the baseband filter should be reprogrammed according to the given standard. For example, WLAN which adopts 64QAM modulation requires a more linear phase response. In contrast, WCDMA employs QPSK and needs sharper stop-band attenuation. In this work, we combine two different filter types of Butterworth and Chebyshev into the same circuit without increasing the power consumption.

In order to optimize noise and maximize the dynamic range, a previous amplifier (pre-amp) that provides course gain tuning is usually placed in front of the baseband filter in traditional receiver architecture. For area saving and power efficiency, the pre-amp can be replaced by a baseband filter in the SDR receiver.

As shown in Table 1, a link budget analysis for SDR zero-IF and low-IF receivers has been made and the specification requirements for the analog baseband filter are given. In this design, the maximum cut-off frequency of 15 MHz is selected in order to cover emerging applications in future.

3. Filter circuits design

3.1. Filter top-level design

To achieve a higher level of performance flexibility, an improved reconfigurable filter architecture is proposed based on other existing architectures[5]. As show in Fig. 1(a), filter top-level architecture mainly consists of a cascade of two biquad stages. Since the first biquad stage provides variable gain amplification (VGA), a DC offset compensation (DCOC) circuit is needed to maintain the stability of the filter output DC voltage. The performance of the proposed filter can be reconfigured through an on-chip control bus (OCCB), i.e. filter transfer function, cut-off frequency, gain, and power consumption, as shown in Fig. 1(a). To compensate the variation of cut-frequency due to process, voltage and temperature (PVT), an automatic frequency calibration (AFC) circuit is also given in this design. As shown in Fig. 1(b), a Tow–Thomas biquad is adopted due to its insensitivity to the value drift of passive components.

3.2. Novel reconfigurable operational amplifier design

The baseband filter often consumes a considerable portion of power budget, so power optimization needs to be taken into consideration. Power dissipation can be reduced when the filter's bandwidth is switched to a low frequency, because the cut-off frequency of the active-RC filter should be proportional to the GBW of the operational amplifier to maintain the stability and reduce enhancement of the quality factor[5]. In zero-IF and low-IF receivers, low bandwidth standards, such as GSM, suffer much from flick noise, while the noise of high bandwidth ones is mainly determined by the KT/C noise. The most effective way to reduce flick noise is to increase the transistors' size. However, parasitic parameters of transistors limit the highest GBW of the operational amplifier. Many compromises have been made in other work [5, 6].

To overcome these difficulties mentioned above, we show a novel reconfigurable operational amplifier architecture to optimize noise and power consumption in this paper. As shown in Fig. 2(a), each reconfigurable operational amplifier consists of two switchable Miller op-amps (SOA) which are connected in parallel, only one of them being switched on simultaneously by configuring the control code "mode". As illustrated in Fig. 2(b), the "low band" mode is defined as the cut-off fre-

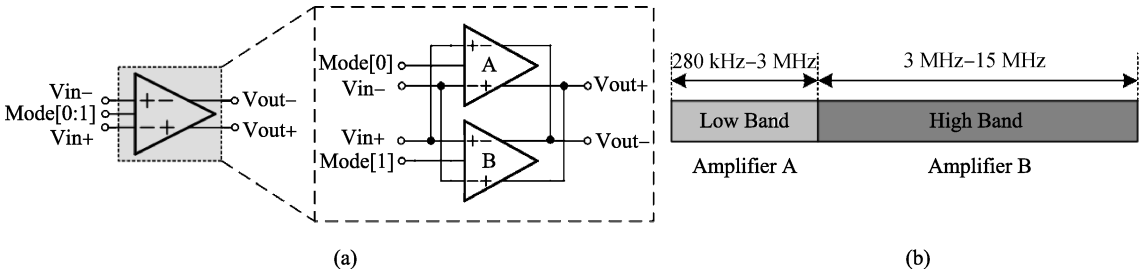

Fig. 2. (a) Top view of reconfigurable operational amplifier. (b) Different cut-off frequency ranges relative to reconfigurable amplifiers.

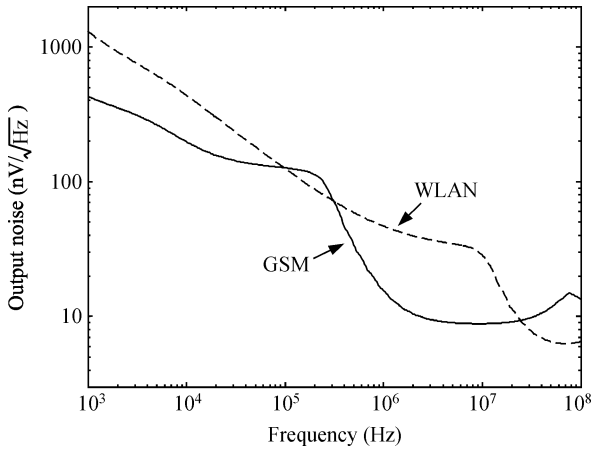

Fig. 3. Noise simulation results of the filter for GSM and WLAN 11 MHz.

quency range from 280 kHz to 3 MHz and employs amplifier A. These standards which locate at the low band domain suffer much from flick noise, so amplifier A is designed to optimize the flick noise by increasing the transistors' size and achieving an appropriate GBW of 120 MHz. The "high band" mode covers the range from 3 to 15 MHz and adopts amplifier B, so the GBW of amplifier B is chosen as several times larger than amplifier A, i.e. 600 MHz. Since power dissipation is proportional to the op-amp's GBW, the optimization of noise and scalability of power consumption can be achieved by switching on/off one of the SOAs. Figure 3 shows the simulation results of the filter output noise for the GSM and WLAN standard while the baseband filter operates at low band and high band mode, respectively. Compared to WLAN, low frequency noise in GSM mode has been reduced considerably.

A schematic of a switchable Miller op-amp is shown in Fig. 4[6]. The architecture of the SOA, which comes from a typical Miller compensation two-stage op-amp, can be turned on/off by configuring a single control bit "mode". For example, when the control bit "mode" is set to 1, all of the MOS switches open and the SOA operates just like a conventional Miller op-amp. In contrast, all of the gates of the PMOS and NMOS are connected to VDD and ground, respectively, then the SOA is switched off and doesn't consume any power.

3.3. Gain adjustment and DC offset compensation

Compared to other filter architectures[5, 6], we embed variable gain adjustment into filter architecture in order to minimize the area and power consumption. As shown in Fig. 5, variable gain amplification is built into the first biquad stage. The gain of the Tow–Thomas biquad can be described as

$$\text{Gain} = \frac{R}{R_{\text{in}}}. \tag{1}$$

According to the equation above, a gain range of 0 to 18 dB with a coarse step of 6 dB can be implemented by modifying the ratio between resistances of R and R_{in}.

As shown in Fig. 5, an integrator is added into a feedback loop to sense and eliminate the DC offset voltage at the output of the first biquad stage[7]. The DC offset compensation feedback loop can be considered as a high pass filter (HPF). The cut-off frequency of the HPF, which should be low enough to avoid filtering desired signals, is determined by the time constant of the integrator and the ratio between the resistances of R and R_2, as described as

$$f_{\text{HPF}} = \frac{R}{R_2}\frac{1}{2\pi R_1 C}. \tag{2}$$

In order to keep the cut-off frequency constant, a switch resistor array R_2 is configured with the same control code as R. The capacitor array C is the same as the ones used in the biquad, adjusted by AFC to maintain an accuracy frequency characteristic. To achieve a cut-off frequency of 6 kHz, radio of R/R_2 is set to 0.1 and $R_1 = 166\,\text{k}\Omega$ and $C = 16$ pF are chosen in this work. Compared to capacitor C, the area consumption of resistance R_1 implemented with high resistivity poly-silicon resistors is still acceptable.

3.4. Cut-off frequency and filter type selection

In a Software-Defined Radio receiver, the system requirements specify that the cut-off frequency of the baseband filter should cover a wide range from 280 kHz up to 15 MHz. Considering the trade-off between cost (silicon area) and accuracy (component size), a binary-weighted switched resistor array is implemented to maximize the range of RC time constant using finite control bits, as shown in Fig. 6. If we define the maximum and minimum cut-off frequency as $f_{\max}$ and $f_{\min}$, respectively, the minimum number of control bits to cover the required frequency range is shown as

$$\text{Nr} = \log_2 \frac{f_{\max}}{f_{\min}}, \tag{3}$$

$$R_{\text{Basic}} = \frac{1 - 2^{-\text{Nr}}}{\pi C_{\text{com}} f_{\max}}, \tag{4}$$

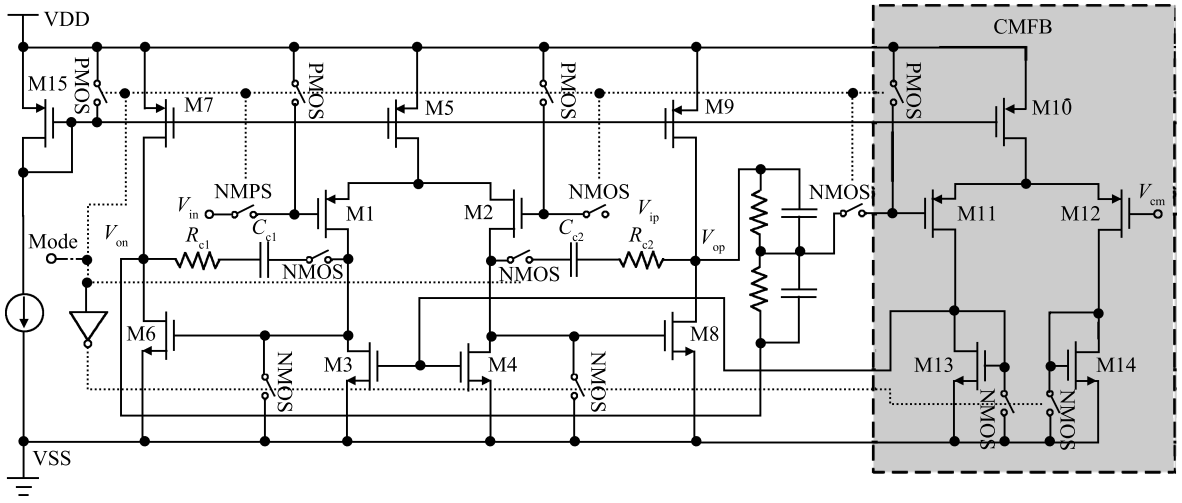

Fig. 4. Schematic of a switchable Miller op-amp (SOA).

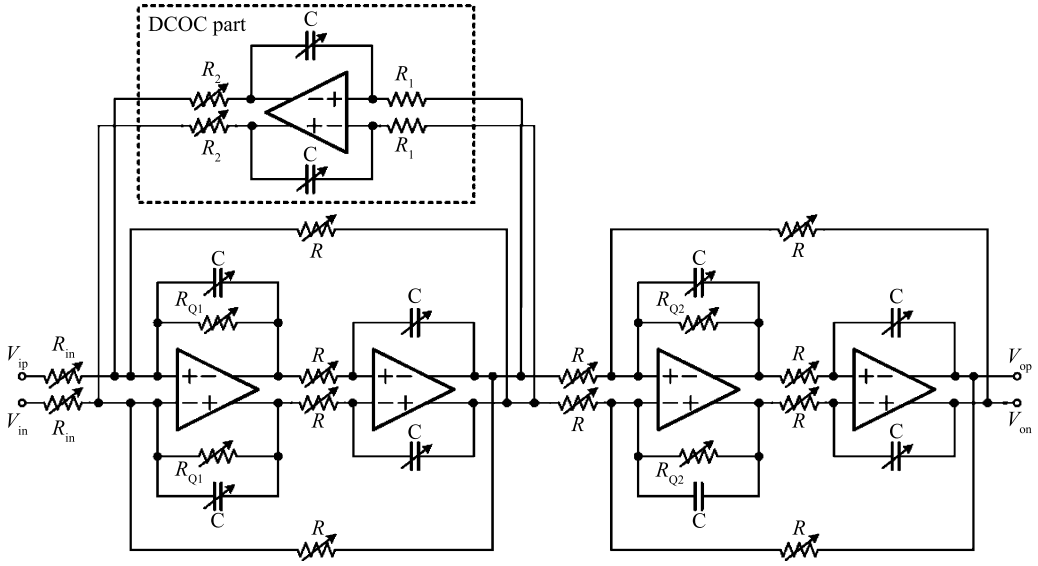

Fig. 5. DC offset compensation circuits.

where C_{com} is the nominal value of the capacitor array configured by AFC. For example, for C_{com} = 16 pF, f_{min} = 280 kHz and f_{max} = 15 MHz, we can get Nr = 6 and $R_{basic} \approx 1.3\,\text{k}\Omega$. For a specific setting, the actual value of the switched resistor array can be given by

The value of the minimum resistor is determined by the maximum cut-off frequency f_{max} as

$$R_{array} = \left(\sum_{k=0}^{Nr-1} \frac{Freq\_Sel_k}{R_{basic} 2^k} \right)^{-1}, \tag{5}$$

where $Freq\_Sel_k$ is a digital control word. And the cut-off frequency of the baseband filter can be shown as

$$f_{cut\text{-}off} = \frac{1}{2\pi R_{array} C_{nom}} = \frac{n \cdot 2^{1-Nr}}{2\pi R_{basic} C_{nom}}, \tag{6}$$

where n is an integer in the range [1, (2^{Nr}– 1)]. For example, for Nr = 6, we can get 63 different cut-off frequencies which cover the range from 280 kHz up to 15 MHz, since the digital control word of all "0"s is invalid. As shown in Fig. 6, the filter type (Butterworth and Chebyshev) can be selected with control bits Butt/Chev. R_{basic} for Butterworth/Chebyshev are R_{Butt} and R_{chev}, respectively.

3.5. Auto-frequency calibration circuit design

Since the process variation of on-chip R/C can be ± 20%, an auto-frequency calibration circuit is a necessary part for the active-RC filter in order to guarantee an accurate frequency response. Compared to a master-slave frequency calibration scheme based on PLL, a simple auto-frequency calibration circuit is more attractive in cost saving and power efficiency, as shown in Fig. 7[8]. High DC gain of the error-amplifier ensures a voltage V_R equal to the reference voltage V_{ref}. The error-amplifier exploits a single stage amplifier structure and the feedback loop illustrated in Fig. 7 contains two adjacent poles. In order to ensure the stability of the feedback loop, a compensation capacitor C_c is added to split the adjacent poles. For area saving, capacitor C_c can be implemented by a MOS-capacitor.

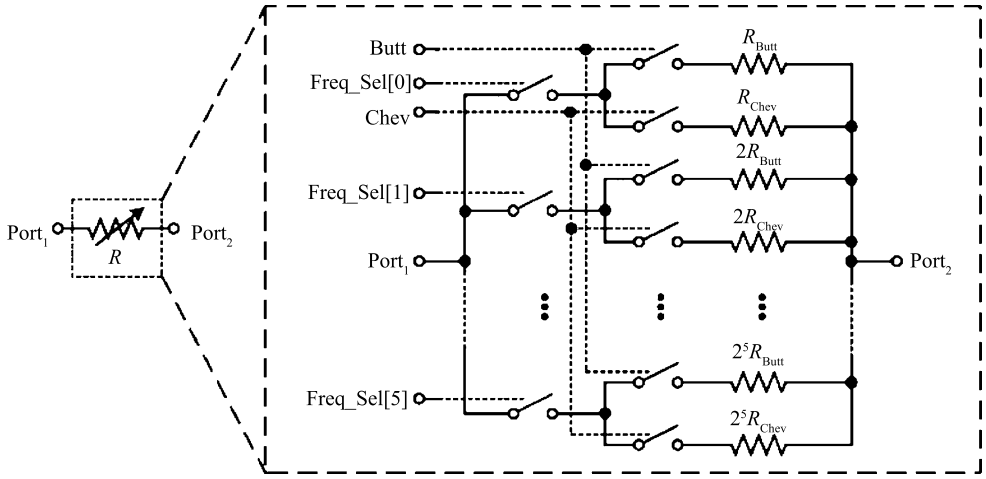

Fig. 6. Switched resistor array for cut-frequency and filter type selection.

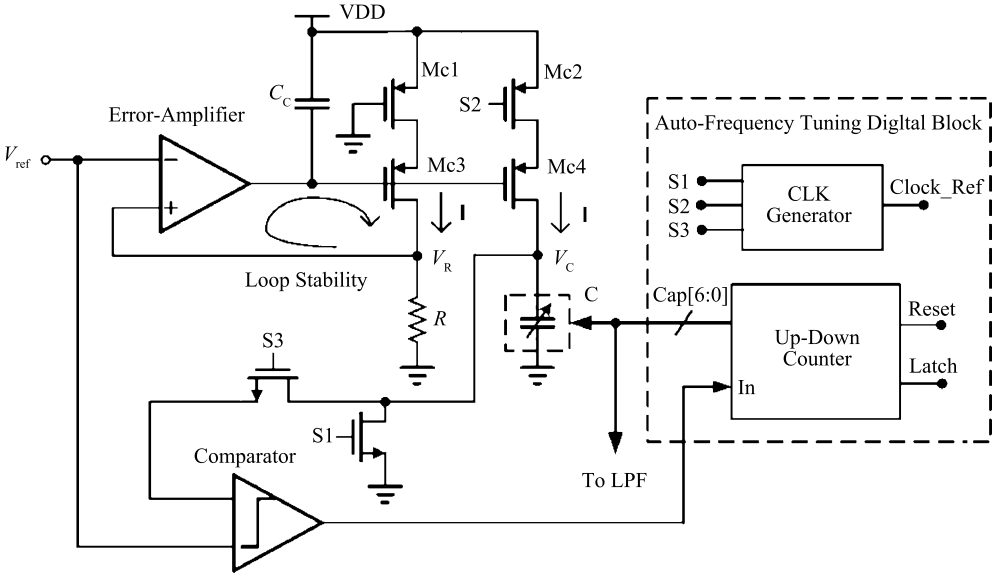

Fig. 7. Automatic frequency calibration circuit.

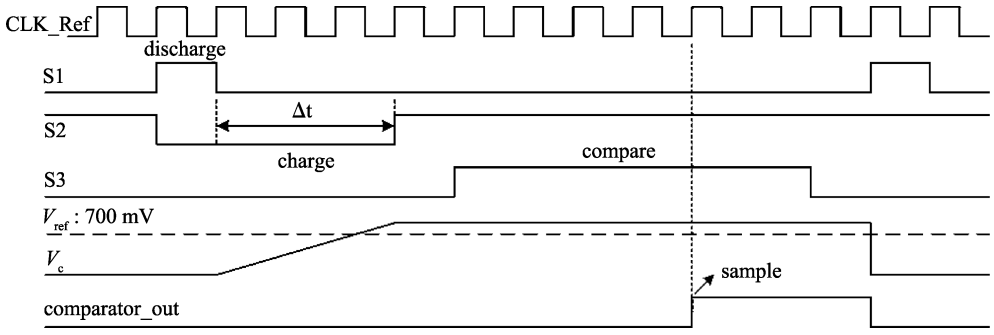

Fig. 8. Switch timing sequence diagram.

The current through resistor R can be given by

$$I = \frac{V_{\text{ref}}}{R}. \tag{7}$$

Figure 8 illustrates the switch timing sequence in detail. When the switch S1 turns on, the electrical quantity of the capacitor array C is discharged to zero. While S1 turns off and S2 turns on, C is charged by a replicate current and the whole charge duration lasts for a time of Δt, which is equal to several periods of reference clock. The voltage of C can be described as

$$V_{\text{c}} = \frac{Q}{C} = \frac{V_{\text{ref}}\Delta t}{RC}. \tag{8}$$

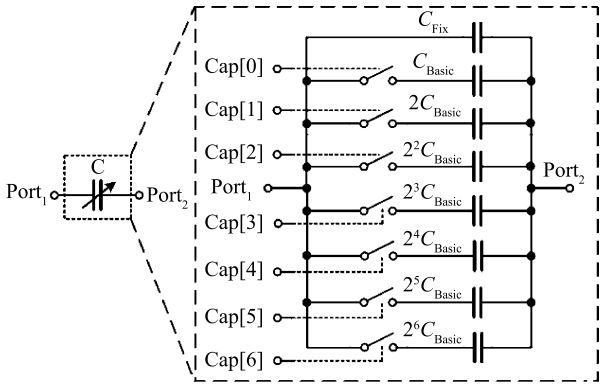

Fig. 9. Capacitor array for automatic frequency calibration.

Then switch S3 closes, and the comparison result between V_c and V_{ref} is sampled by an up-down counter. When V_c is larger than V_{ref}, the capacitance of C adjusted by the up-down counter is increased. In contrast, the capacitance of C is reduced. An optimal binary search algorithm is adopted to shorten the calibration time. The comparison process is finished when $V_c = V_{ref}$ and the RC time constant is given by

$$RC = \Delta t. \tag{9}$$

In order to ensure calibration accuracy, the cascode transistors Mc3 and Mc4 are designed to the same size. When switch S2 closes, the transistor Mc2 can be used as a linear resistor. In order to achieve good matching, the gate of the replicate transistor Mc1 is grounded.

Figure 9 illustrates a binary-weight capacitor array controlled by a automatic frequency calibration circuit. Once we define ξ as the variation of RC time constant, we can calculate the minimum and maximum capacitance by

$$C_{min} = C_{Fix} = \frac{C_{nom}}{1+\xi}, \tag{10}$$

$$C_{max} = C_{Fix} + (2^{Nc}-1)C_{Basic} = \frac{C_{com}}{1-\xi}, \tag{11}$$

where C_{com} is the nominal value of the capacitor array. From Eqs. (8) and (9), the unit capacitance C_{basic} is described as

$$C_{basic} = \frac{1}{2^{Nc}-1}\left(\frac{C_{com}}{1-\xi} - C_{Fix}\right) = \frac{C_{com}}{2^{Nc}-1}\frac{2\xi}{1-\xi^2}. \tag{12}$$

The relative error between the discrete capacitance value C_{array} and the nominal capacitance C_{com} is shown as

$$\varepsilon_{max} = \pm\frac{1}{2}\frac{C_{basic}}{C_{nom}} = \pm\frac{1}{2^{Nc}-1}\frac{\xi}{1-\xi^2}. \tag{13}$$

In order to compensate the variation ξ, the minimum number of control bits is given by

$$Nc = \log_2\left|\frac{\xi}{\varepsilon_{max}(1-\xi^2)} + 1\right|. \tag{14}$$

For $\xi = 40\%$ and $C_{com} = 16$ pF, we can get Nc = 7 and C_{Basic} = 120 fF. In order to minimize the distortion due to the nonlinearity of the switches, all of the sources of the MOS switches are connected to the inputs of the op-amps where the voltage swing is close to zero.

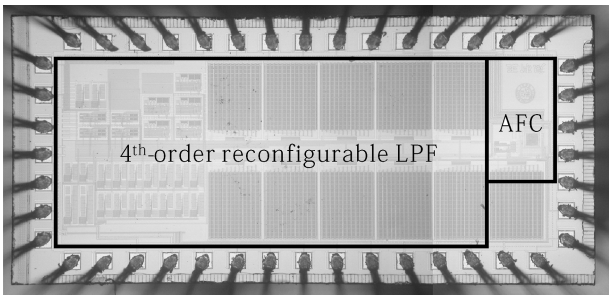

Fig. 10. Chip microphotograph.

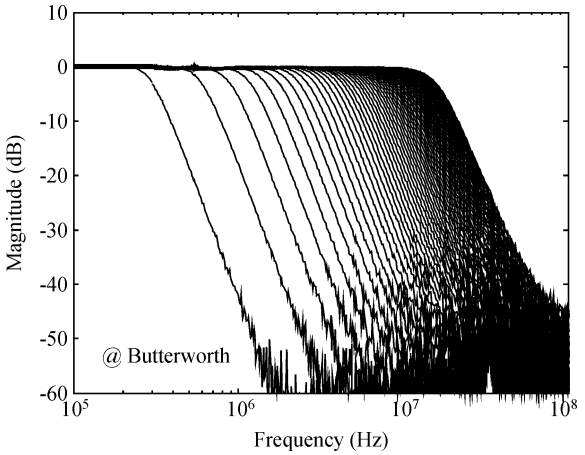

Fig. 11. Measured magnitude responses.

4. Measurement results

The proposed filter was fabricated in an SMIC 0.13 μm CMOS process with a 1.2 V supply voltage. The chip microphotograph is shown in Fig. 10, where a filter core circuit occupies an area of 1.8 × 0.8 mm^2 and the AFC occupies 0.48 × 0.25 mm^2. The integrated capacitors and resistors were implemented with floating MIM capacitors and high resistivity poly-silicon resistors, respectively.

Figure 11 illustrates the measured magnitude responses in 63 possible combinations of cut-off frequencies, which cover a wide range from 280 kHz up to 15 MHz. The power consumption is 5.46 mW for low band mode and 8.74 mW for high band mode.

As shown in Fig. 12, the performance of the gain adjustment indicates that the proposed circuit can provide a gain range from 0 to 18 dB with a coarse step of 6 dB. As shown in Fig. 13, two typical filter types of Butterworth and Chebyshev can be selected. According to the given standard, the filter can be switched from Butterworth to Chebyshev for steeper stopband attenuation or from Chebyshev to Butterworth for a more linear phase response.

An in-band IM3 of –64.8 dB is obtained for the WLAN standard when the input powers of two tones (at 5 and 6 MHz) are –9.8 dBm, as shown in Fig. 14. Measured results of the in-band IIP3 are shown in Fig. 15. The IIP3 of 24.5 dBm for the WLAN is obtained with two tones' frequencies of 5 and 6 MHz. For WCDMA, the IIP3 of 29 dBm is obtained with two tones' frequencies of 700 and 800 kHz. Considering that the

Table 2. Performance summary.

Parameter		Value
Technology		SMIC 0.13 μm CMOS
Supply voltage		1.2 V
Filter order		4th order
Filter type		Butterworth & Chebyshev
Cut-off frequency range		0.28–15 MHz
Gain range		0–18 dB
Gain step		6 dB
Input referred noise density		41–133 nV/$\sqrt{\text{Hz}}$
Integrated noise	GSM	62 μVrms (from 20 to 220 kHz)
	WLAN	136 μVrms (from 0.02 to 11 MHz)
In-band IM3		–64.8 dB @ –9.8 dBm (f_1 = 5 MHz, f_2 = 6 MHz)
In-band IIP3		29 dBm @ WCDMA (f_1 = 700 kHz, f_2 = 800 kHz)
		24.5 dBm @ WLAN 11 MHz (f_1 = 5 MHz, f_2 = 6 MHz)
Calibration accuracy		3%
Power consumption	Low band	5.46 mW
	High band	8.74 mW
Die area	Filter core	1.8 × 0.8 mm^2
	AFC	0.48 × 0.25 mm^2

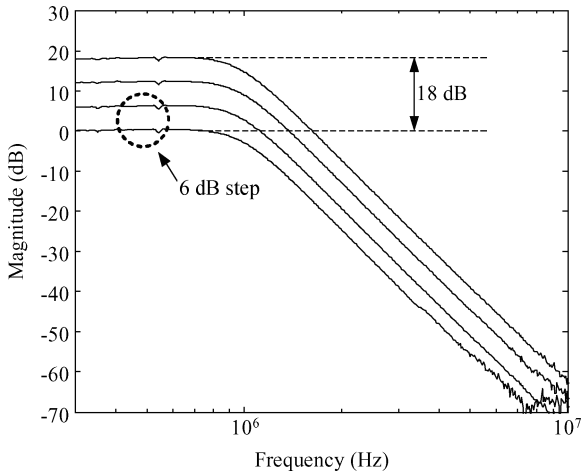

Fig. 12. Gain adjustment.

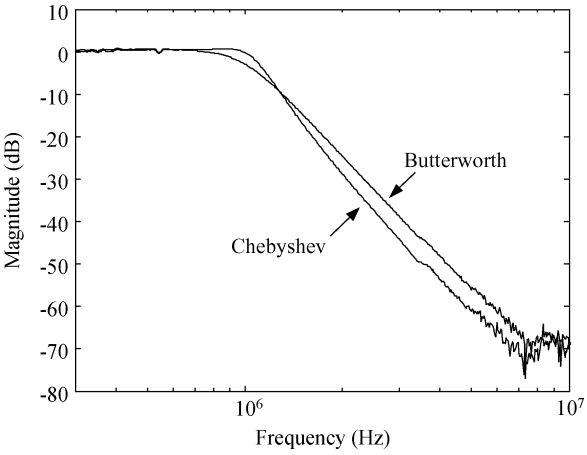

Fig. 13. Filter type selection.

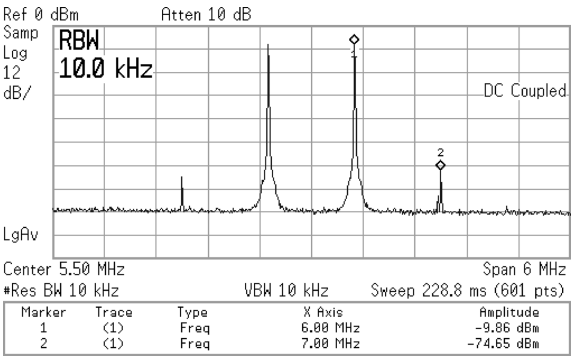

Fig. 14. Measured in-band IM3 for WLAN.

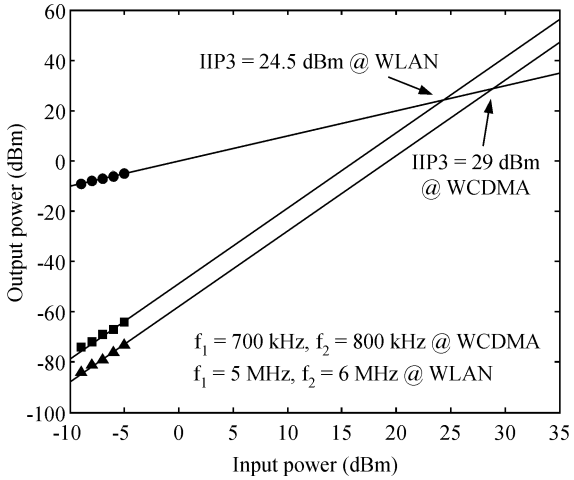

Fig. 15. Measured in-band IIP3.

supply voltage is limited to 1.2 V, an IIP3 of 29 dBm indicates that the proposed design achieves a high linearity performance.

For the GSM standard, the input integrated in-band noise is only 62 μVrms, while the filter operates at low-band mode and consumes 5.46 mW. For the WLAN standard, the input integrated in-band noise is 136 μVrms and the ripple around the cut-off frequency is negligible, while the filter operates at High Band mode and consumes 8.74 mW. Table 2 shows the measured results of the proposed filter, and Table 3 gives the comparison results between this work and several recently pub-

Table 3. Comparison with recently published works.

Reference	Process	Topology	Order	V_{dd} (V)	Power/Pole (mW/pole)	$f_{cut\text{-}off}$ range (MHz)	Noise ($nV/\sqrt{Hz}$)	IIP3 (dBm)
Ref. [9]	CMOS 0.12 μm	Active-RC	5/3	1.2	0.92	5, 10	85, 143	18.5–21.3
Ref. [10]	CMOS 0.13 μm	Active-RC	5	1.5	2.25	19.7	30	18.3
Ref. [11]	CMOS 0.18 μm	$G_m - C$	3	1.0	0.52–0.64	0.135–2.2	65	16.3–20.1
This work	CMOS 0.13 μm	Active-RC	4	1.2	1.36/2.18	0.28–15	41–133	24.5–29

lished works.

5. Conclusion

This paper presents a feasible solution to implement an analog baseband filter for software-defined radio. In order to realize the optimization of noise and scalability of power consumption, a novel reconfigurable operational amplifier is proposed. A 4th-order active-RC low-pass filter with a multiple variety of characteristics has been fabricated in a SMIC CMOS 0.13 μm process with a 1.2 V voltage supply. Complete experimental results are provided to confirm the validity of the proposed filter, which is suitable to be implemented in zero-IF and low-IF receivers for SDR applications.

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