A resistorless CMOS current reference with temperature compensation*

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Abstract: A resistorless CMOS current reference is presented. Temperature compensation is achieved by subtracting two sub-currents with different positive temperature coefficients. The circuit has been implemented with a Chartered 0.35 μm CMOS process. The output current is 1.5 μA, and the circuit works properly with a supply voltage down to 2 V. Measurement results show that the temperature coefficient is 98 ppm/℃, and the line regulation is 0.45%/V. The occupied chip area is 0.065 mm^2.

Key words: current reference; resistorless; temperature compensation
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1. Introduction

A current reference is an essential building block in almost all analog and mixed-signal systems as a bias for various circuits, such as amplifiers, oscillators, filters, and so on. It is therefore desirable to generate a precise reference current which is insensitive to the variations of ambience temperature and supply voltage. Practically, temperature compensation of a current reference is a difficult task. The early solutions use the square term of thermal voltage ($V_T = kT/q$) to partially compensate for the temperature characteristic of carrier mobility[1, 2]. Unfortunately, the output current is pseudo constant and exhibits a large temperature coefficient. As a result, various temperature compensation techniques have been proposed in recent years[3–7]. However, all of these solutions are based on on-chip resistors. Usually, the resistivity of an on-chip resistor may vary with the technology, and its temperature coefficient (TC) is also not well defined[2]. This problem greatly deteriorates the temperature characteristic of the output current. Consequently, a temperature compensation scheme without resistors is preferred.

In this paper, a novel resistorless CMOS current reference is presented. Based on the weighted difference between two temperature-dependent sub-currents, good temperature compensation of the output current is achieved. The proposed circuit has been fabricated with a Chartered 0.35 μm CMOS process. The measured temperature coefficient is 98 ppm/℃ over a temperature range from –10 to 100 ℃, and the occupied chip area is 0.065 mm^2.

2. The proposed current reference

2.1. Operation principle

The proposed circuit is based on the observation that the TC of most traditional CMOS current references, though the output currents are still temperature dependent, is very stable, and can be precisely expressed[1, 2]. As a result, by properly making the weighted difference between two temperature dependent sub-currents, good temperature compensation can be achieved. This operation principle is briefly illustrated in Fig. 1, wherein I_{REF1} and I_{REF2} are two traditional pseudo constant reference currents with different TCs, TC1 and TC2 (TC1 < TC2), respectively. As can be seen, the output current I_{REF} will exhibit zero TC by properly choosing the multiplication factor M. The detailed analysis and circuit implementation will be explained in the following sections.

2.2. Circuit implementation

Figure 2 shows the detailed transistor level circuit of the proposed current reference. Two pseudo constant CMOS current references[1] ('N-type core' and 'P-type core') generate the sub-currents I_{REF1} and I_{REF2}, wherein different types of core devices (M7–M10 and M17–M20) are utilized to produce different TCs. The devices in the shadow regions are biased in weak inversion, while all of the other devices are in strong inversion. Since the two current generators are theoretically identical, only the 'N-type core' circuit is taken for analysis here. From Fig. 2 it can be easily derived that

$$V_{GS1} + V_{GS7} - V_{GS8} + V_{GS9} - V_{GS10} - V_{GS2} = 0. \quad (1)$$

Ignoring the channel length modulation effect for simplicity, the V_{GS} of a MOSFET in strong and weak inversion can be expressed as[8]

$$V_{GS,Strong} = V_{TH} + \sqrt{\frac{2I_{DS}}{\mu C_{ox} S}}, \quad (2)$$

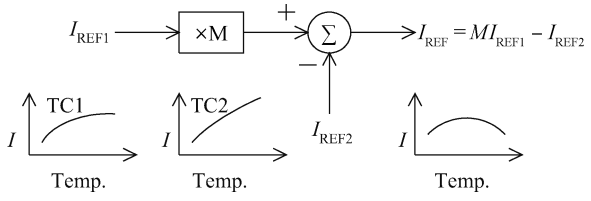

Fig. 1. Operation principle of the proposed current reference.

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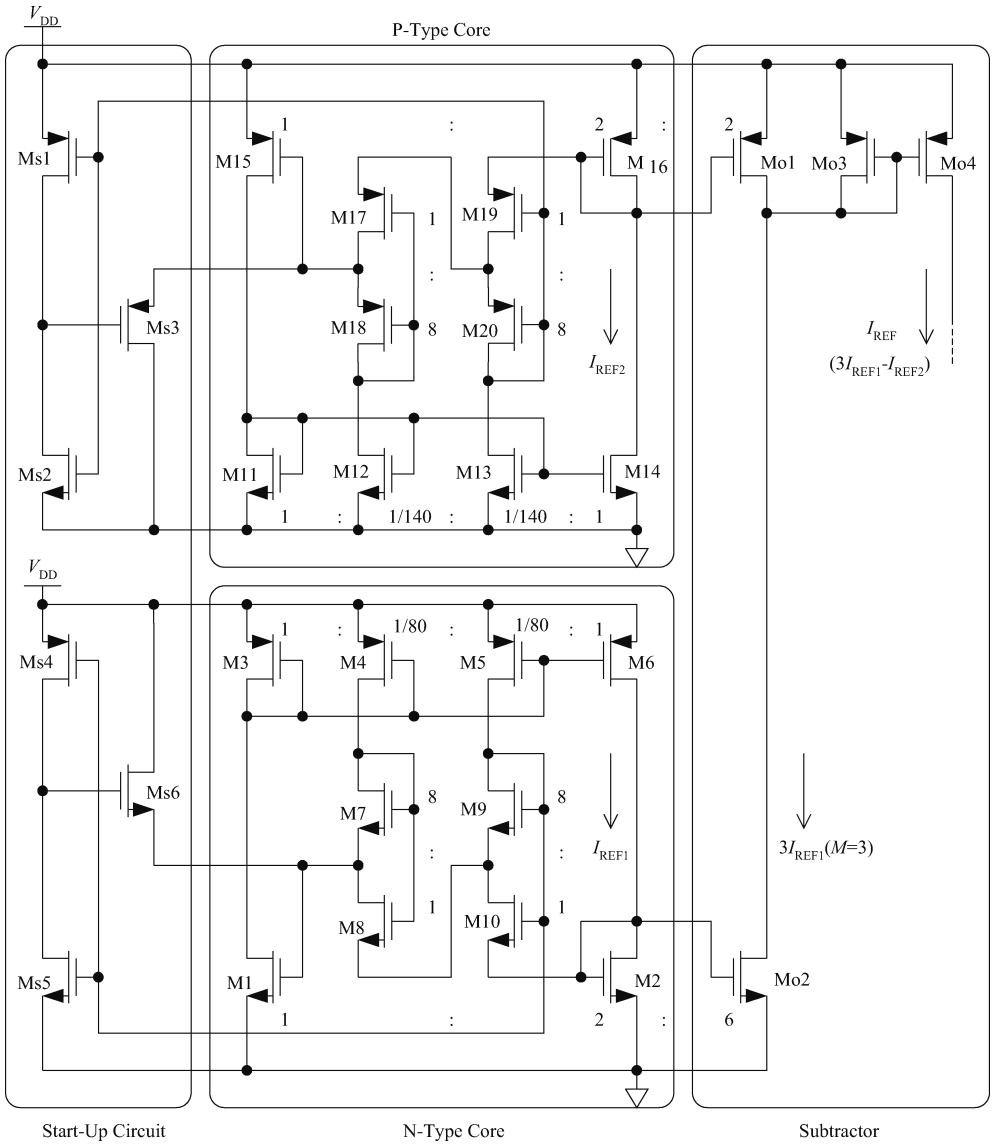

Fig. 2. Transistor level implementation of the proposed current reference.

$$V_{\mathrm{GS,Weak}} = V_{\mathrm{TH}} + nV_{\mathrm{T}} \ln \frac{I_{\mathrm{DS}}}{\mu C_{\mathrm{ox}} V_{\mathrm{T}}^2 S}, \tag{3}$$

where S represents the aspect ratio of MOSFET, n is the sub-threshold sloping factor, and V_{T} is the thermal voltage. In the 'N-type core' circuit, M1–M2 operate in strong inversion, while M7–M10 in weak inversion. Assuming $I_{\mathrm{DS1}} = I_{\mathrm{DS2}} = I_{\mathrm{REF1}}$, substituting Eqs. (2) and (3) into Eq. (1), we derive

$$I_{\mathrm{REF1}} = \frac{\mu_{\mathrm{n}} C_{\mathrm{ox}} n^2 V_{\mathrm{T}}^2}{2} \left(\frac{\sqrt{S_2} - \sqrt{S_1}}{\sqrt{S_1 S_2}} \ln \frac{S_7 S_9}{S_8 S_{10}} \right)^2. \tag{4}$$

Generally, the carrier mobility μ_{n} and thermal voltage V_{T} are temperature dependent and can be expressed as

$$\mu_{\mathrm{n}} = \mu_{\mathrm{n0}} (T/T_0)^{-K_{\mu_{\mathrm{n}}}}, \tag{5}$$

$$V_{\mathrm{T}} = kT/q = V_{\mathrm{T0}} (T/T_0), \tag{6}$$

where T_0 is the room temperature, V_{T0} is the thermal voltage at T_0, μ_{n0} is the carrier mobility at T_0, and $K_{\mu\mathrm{n}}$ is the temperature coefficient of μ_{n}. Substitute Eqs. (5) and (6) into Eq. (4), I_{REF1} can be written as

$$\begin{aligned} I_{\mathrm{REF1}} &= \frac{\mu_{\mathrm{n0}} C_{\mathrm{ox}} n^2 V_{\mathrm{T0}}^2}{2} \\ &\quad \times \left(\frac{\sqrt{S_1 S_2}}{\sqrt{S_2} - \sqrt{S_1}} \ln \frac{S_7 S_9}{S_8 S_{10}} \right)^2 \left(\frac{T}{T_0} \right)^{2 - K_{\mu_{\mathrm{n}}}} \\ &= I_{\mathrm{REF10}} \left(\frac{T}{T_0} \right)^{2 - K_{\mu_{\mathrm{n}}}}. \end{aligned} \tag{7}$$

It can be clearly seen that I_{REF1} is temperature dependent. Usually, $K_{\mu\mathrm{n}}$ is provided by the foundry and is around 1.5. Therefore, I_{REF1} has a positive TC. With similar analysis, I_{REF2} can also be derived as

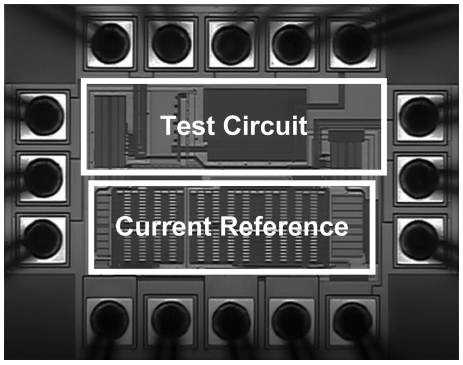

Fig. 3. Die photograph of the proposed current reference.

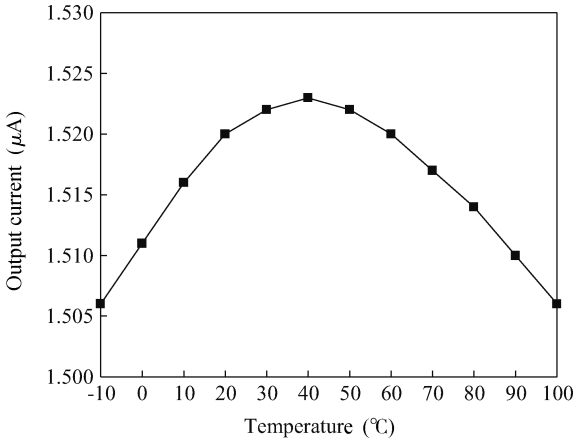

Fig. 4. Measured temperature characteristic of output current.

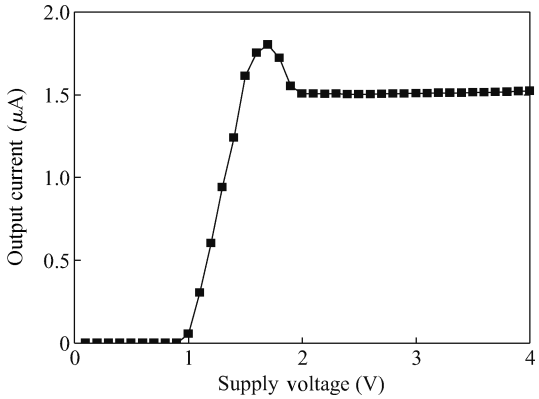

Fig. 5. Measured line regulation of output current.

$$I_{\mathrm{REF2}} = \frac{\mu_{\mathrm{p0}} C_{\mathrm{ox}} n^2 V_{\mathrm{T0}}^2}{2} \times \left(\frac{\sqrt{S_{15}S_{16}}}{\sqrt{S_{16}} - \sqrt{S_{15}}} \ln \frac{S_{18}S_{20}}{S_{17}S_{19}} \right)^2 \left(\frac{T}{T_0} \right)^{2-K_{\mu_{\mathrm{p}}}} = I_{\mathrm{REF20}} \left(\frac{T}{T_0} \right)^{2-K_{\mu_{\mathrm{p}}}}. \quad (8)$$

As a result, the output current is $I_{\mathrm{REF}} = M I_{\mathrm{REF1}} - I_{\mathrm{REF2}}$. Substituting Eqs. (7)–(8), and differentiating the equation with respect to temperature, the TC of the output current at the temperature concerned T_{REF} can be derived as

$$\left. \frac{\mathrm{d}I_{\mathrm{REF}}}{\mathrm{d}T} \right|_{T=T_{\mathrm{REF}}} = M I_{\mathrm{REF10}} (2 - K_{\mu_{\mathrm{n}}}) \left(\frac{T_{\mathrm{REF}}}{T_0} \right)^{1-K_{\mu_{\mathrm{n}}}} - I_{\mathrm{REF20}} (2 - K_{\mu_{\mathrm{p}}}) \left(\frac{T_{\mathrm{REF}}}{T_0} \right)^{1-K_{\mu_{\mathrm{p}}}}. \quad (9)$$

Equating (9) to zero, temperature compensation can be achieved by satisfying

$$M = \frac{\mu_{\mathrm{p0}}(2 - K_{\mu_{\mathrm{p}}})}{\mu_{\mathrm{n0}}(2 - K_{\mu_{\mathrm{n}}})} \left(\frac{\frac{\sqrt{S_{15}S_{16}}}{\sqrt{S_{16}} - \sqrt{S_{15}}} \ln \frac{S_{18}S_{20}}{S_{17}S_{19}}}{\frac{\sqrt{S_1S_2}}{\sqrt{S_2} - \sqrt{S_1}} \ln \frac{S_7S_9}{S_8S_10}} \right)^2 \times \left(\frac{T_{\mathrm{REF}}}{T_0} \right)^{K_{\mu_{\mathrm{n}}} - K_{\mu_{\mathrm{p}}}}. \quad (10)$$

2.3. Design consideration

The value of M and the dimension ratios of important MOSFETs are given in Fig. 2. In this design, it is very important for M7–M10 and M17–M20 to be biased in weak inversion, and M1–M2 and M15–M16 in strong inversion. Since the temperature characteristic of the output current is absolutely based on the I_{DS} expressions in these regions, as analyzed before. Large current error during fabrication greatly degrades the TC performance of the output current. In order to limit the current error within 5%, the following conditions have to be met during the design[2, 9],

$$\begin{cases} I_{\mathrm{DS}} < 0.005 \mu C_{\mathrm{ox}} S V_{\mathrm{T}}^2, & \text{for weak inversion,} \\ I_{\mathrm{DS}} > 15 \mu C_{\mathrm{ox}} S V_T^2, & \text{for strong inversion.} \end{cases} \quad (11)$$

Another important issue is the deviations of process parameters, such as C_{ox}, n, and mobility, which may influence the accuracy of the output current. However, the effective gain factor $n^2 \mu_{\mathrm{n0}} C_{\mathrm{ox}}$ ($n^2 \mu_{\mathrm{p0}} C_{\mathrm{ox}}$) of a MOSFET in a standard CMOS technology is very reproducible if the transistors are drawn with large dimensions[1, 2]. Consequently, a minimum dimension of 10 μm is chosen in this design, which also helps to improve the matching property of the devices.

3. Experimental results

The proposed circuits were fabricated with a Chartered 0.35 μm CMOS process ($K_{\mu\mathrm{n}}$ = 1.724 and $K_{\mu\mathrm{p}}$ = 1.49). The die photograph is shown in Fig. 3, and the occupied chip area without the test circuit is 0.065 mm^2. This area is restricted by the minimum dimension of MOSFETs, which is set to be 10 μm in this design to improve the matching property of the devices. The proposed circuit provides an output current of 1.5 μA, and the whole current draw from the supply voltage is 6.8 μA. Ten samples were tested, and the maximum output deviation was 6% under a 3.3 V power supply at room temperature. The measured temperature characteristic of the output

Table 1. Performance comparison between this work and the literature.

	This work	Sansen[1]	Bendali[4]	Yoo[5]	Serrano[6]	Zhao[7]
Technology	0.35 μm CMOS	3 μm CMOS	0.18 μm CMOS	0.25 μm CMOS	0.5 μm CMOS	0.5 μm CMOS
I_{OUT} (μA)	1.5	0.774	144	10.45	16–50	27.7
I_{SUPPLY} (μA)	6.8	2	N/A	70	N/A	N/A
V_{DD} (V)	> 2	> 3.5	> 1.0	> 1.1	> 2.3	> 2.5
TC (ppm/℃)	98	375	185	720	130	290
T range (℃)	−10 to 100	0–80	0–100	0 –120	0–80	−20 to 110
Supply regulation (%/V)	0.45	0.015	N/A	0.17	1	N/A
Area (mm^2)	0.065	0.2	0.12	0.002	0.06	0.023

current is shown in Fig. 4, and the TC is 98 ppm/℃ with the temperature varying from – 10 to 100 ℃. Figure 5 shows the measured output current against the supply voltage. It can be seen that the minimal supply voltage is about 2 V, and the supply regulation is 0.45%/V with the supply voltage varying from 2 to 4 V. It should be noted that a peak current exists at the supply voltage around 1.7 V. This is because the output current is a weighted difference between two sub-currents. During this supply range, I_{REF1} is already generated by the 'N-type core' circuit, while the 'P-type core' circuit has not fully started due to the larger threshold voltage of P-MOSFETs with respect to that of N-MOSFETs. After the supply voltage rises above 2 V, both of the core circuits work properly, and the output current returns to the normal value. The performance comparison between this work and previously published current references is given in Table 1. Thanks to the proposed resistor-less structure and temperature compensation scheme, the problem with the large variations in on-chip resistor and its temperature characteristic is eliminated. Consequently, the proposed current reference achieves the lowest temperature coefficient.

4. Conclusion

A resistorless CMOS current reference has been designed using a Chartered 0.35 μm CMOS process. Temperature compensation is achieved by making a weighted difference between two temperature dependent sub-currents, and the measured temperature coefficient is 98 ppm/℃. The minimal supply voltage is 2 V and the line regulation is 0.45%/V. The chip area is 0.065 mm^2.

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