A robust and simple two-mode digital calibration technique for pipelined ADC*

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Abstract: This paper presents a two-mode digital calibration technique for pipelined analog-to-digital converters (ADC). The proposed calibration eliminates the errors of residual difference voltage induced by capacitor mismatch of pseudorandom (PN) sequence injection capacitors at the ADC initialization, while applies digital background calibration to continuously compensate the interstage gain errors in ADC normal operation. The presented technique not only reduces the complexity of analog circuit by eliminating the implementation of PN sequence with accurate amplitude in analog domain, but also improves the performance of digital background calibration by minimizing the sensitivity of calibration accuracy to sub-ADC errors. The use of opamps with low DC gains in normal operation makes the proposed design more compatible with future nanometer CMOS technology. The prototype of a 12-bit 40-MS/s pipelined ADC with the two-mode digital calibration is implemented in 0.18-μm CMOS process. Adopting a simple telescopic opamp with a DC gain of 58-dB in the first stage, the measured SFDR and SNDR within the first Nyquist zone reach 80-dB and 66-dB, respectively. With the calibration, the maximum integral nonlinearity (INL) of the ADC reduces from 4.75-LSB to 0.65-LSB, while the ADC core consumes 82-mW at 3.3-V power supply.

Key words: analog-to-digital converter; pipelined ADC; background calibration; finite DC gains of opamps; capacitor mismatch; pseudorandom noise sequence

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1. Introduction

In the design of a pipelined analog-to-digital converter (ADC), the linearity is primarily degraded by the interstage gain errors, among which the two most important and common sources are capacitor mismatches and finite DC gain of residue amplifiers. To reduce gain errors, one approach is to build high-gain amplifiers using techniques such as multistage topologies and/or gain boosting[1, 2]. This approach increases the complexity of analog circuit design and is limited by the restrictive stability conditions or voltage headroom requirements, especially at a high speed. Another approach, followed in this paper, is to calibrate the pipeline stages for gain errors. Among the calibration schemes, digital background calibration[3−9] is the most attractive technique, because it does not interrupt ADC's normal operation while tracks supply and temperature variations.

In most cases, digital background calibration technique is implemented by injecting a pseudorandom (PN) sequence into ADCs with the input signal, estimating the circuit non-ideal parameters carried by the PN sequence, and correcting the digital output. In previous designs, there are three main methods of PN injection. One approach is to split the sampling capacitors and inject the PN sequence through one of them. It increases the complexity of the analog layout and capacitor parasitics[3, 4], especially in multi-bit topologies[4], which are widely used in high resolution pipelined ADCs. Another solution is to randomize the sub-ADC thresholds/references[5, 6] or insert dither logic before sub-DAC[7]. Both techniques either increase the number of comparators[5, 6], or require 1-bit redundancy in the following stage[7], and their calibration accuracies are sensitive to the sub-ADC errors[5−7]. A third technique is to inject the PN sequence through an extra capacitor connected to the sub-DAC[8, 9]. This method requires implementing a scaled pseudorandom noise sequence with a very accurately known magnitude in the analog domain[10]. In currently available designs, this issue is resolved by adding a slow-but-accurate sigma-delta ADC[9].

In this paper, a two-mode digital calibration technique is applied to enhance the ADC performance and to simplify the analog circuit implementation. The PN sequence is injected through an extra-DAC to make the accuracy of digital background calibration insensitive to sub-ADC errors, including capacitor offsets and sub-ADC reference voltage variation. The amplitude of the PN sequence is measured at the ADC initialization and stored in ROM for ADC normal operation, when digital background calibration is applied to continuously compensate the interstage gain errors. In the proposed design, the implementation of PN sequence with accurate amplitude in analog domain is replaced by measuring the amplitude of the PN sequence at the ADC initialization, which reduces the complexity of analog circuit and saves the power and area. Compared with the previous designs, the presented work adds only a pair of gain-boosters to the opamp at ADC initialization rather than adding a slow-but-accurate sigma-delta ADC in normal operation[9]. With the proposed technique, opamps with low

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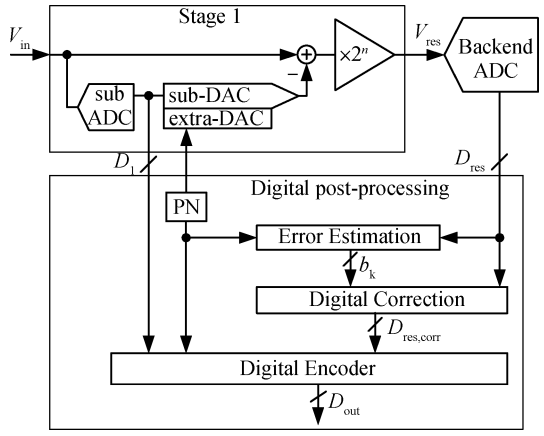

Fig. 1. The background calibration architecture of pipelined ADC.

DC gains are sufficient for ADC normal operation, which is compatible with future CMOS technology, since the reduced characteristic dimension and intrinsic gain of MOSFET bring more difficulty to implement opamps with high DC gains[11].

The presented calibration is employed in a 12-bit 40-MS/s prototype pipelined ADC. When the calibration is applied, the SFDR and SNDR improve by 16-dB and 14-dB, respectively. Using a booster-free single stage telescopic opamp with a DC gain of 58-dB in the first stage, the measured SFDR and SNDR with a 19.1-MHz input at full sampling rate are 80-dB and 66-dB, respectively.

2. Proposed calibration technique

In a pipelined ADC, the analog residue voltage of each stage can be expressed as

$$V_{\text{ref}} = G_{\text{A}}(V_{\text{in}} - DV_{\text{ref}}) = G_{\text{A}}Q_{\text{R}}, \tag{1}$$

where G_{A} is the ideal interstage gain, V_{in} is the stage input voltage, D is the stage digital output, V_{ref} is the ADC reference, and Q_{R} is the stage quantization noise. Finite DC gain of the opamp and mismatch between the sampling and feedback capacitors in an n-effective-bit stage induce interstage gain errors and change G_{A} from the ideal value of 2^n to

$$g_{\text{A}} = 2^n(b_1 + b_2Q_{\text{R}} + b_3Q_{\text{R}}^2 + \cdots), \tag{2}$$

where g_{A} is the actual interstage gain and b_1–b_3 represent the coefficients of Talyor expansion, in which b_2 can be omitted for a fully differential architecture.

Figure 1 illustrates the architecture of digital background calibration in pipelined ADC. For simplicity, only the first stage under digital background calibration is considered. The calibration scheme statistically extracts the interstage gain errors from residual difference voltages (H_1) at the same input location between the two randomly switching modes as in Ref. [6] and calculates the corrected digital residue from the following equation.

$$D_{\text{res,corr}} = \frac{1}{b_1}(D_{\text{res}} - e[D_{\text{res}}, p_3)], \tag{3}$$

where D_{res} is the actual digital residual of the stage, D_{res}, corr is the corrected digital residual and p_3 is the extracted calibration

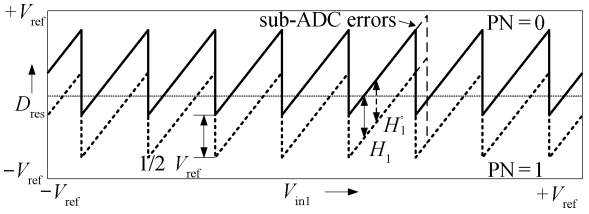

Fig. 2. Two modes of transfer.

parameter for correcting the third-order interstage gain nonlinearity. Function $e(D_{\text{res}}, p_3)$ is expressed as in Eq. (4), which can be implemented in hardware by a 2-dimensional look-up table for simplicity[7].

$$e(D_{\text{res}}, p_3) = D_{\text{res}} - 2p_3\cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{D_{\text{res}}}{\frac{2}{3}p_3}\right)\right]. \tag{4}$$

The two transfer modes are implemented in the first stage and controlled by a PN sequence, as shown in Fig. 2.

The most significant advantage of the proposed calibration is that the PN injection scheme ensures the insensitivity of calibration accuracy to sub-ADC errors and avoids complex implementation in the analog domain.

2.1. Insensitivity to sub-ADC errors

Sub-ADC errors, including comparator offsets and the input-signal-dependent sub-ADC reference voltage variations, tend to worsen the accuracy of calibration[4−7]. In digital background calibration, the error estimation block calculates circuit errors from two digital residue voltages generated with different values of PN sequence. If the digital residues for comparison are generated from different ranges of ADC input or transferred through different comparators in the first stage, the sub-ADC errors of the stage will become PN-sequence-dependent and induce errors. Take correlation-based and statistics-based calibration adopting duplicated capacitors to inject PN sequence for example. For correlation-based calibration[4], the estimated interstage gain error is obtained by correlating the digital output of the back-end ADC with the same PN sequence. As derived from Ref. [10], the estimated interstage gain is

$$\overline{g}_{\text{A}} = g_{\text{A}} + P_{\text{A}} \otimes (g_{\text{A}}Q_{\text{R}} - O_{\text{N}})/(P_{\text{A}} \otimes P'_{\text{N}}), \tag{5}$$

where P_{N} is the PN sequence, $\otimes$ represents the correlation operator, and O_{N} is the thermal noise and the quantization noise of the back-end ADC. Since P_{N} is uncorrelated with O_{N}, their correlation products will approach zero as the length of PN sequence increases. However, Q_{R} contains a portion of sub-ADC errors which is correlated with PN sequence. The PN-dependent sub-ADC errors can neither be eliminated by correlation, nor be distinguished from the actual interstage gain. In existing statistics-based calibrations[5−7], as indicated in Fig. 3, the PN-dependent sub-ADC errors make the extraction of residual difference at different input locations and therefore induce errors. In Ref. [5], the errors induced by sub-ADC

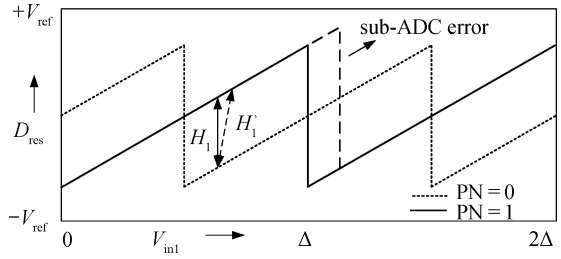

Fig. 3. Sub-ADC errors worsen calibration accuracy.

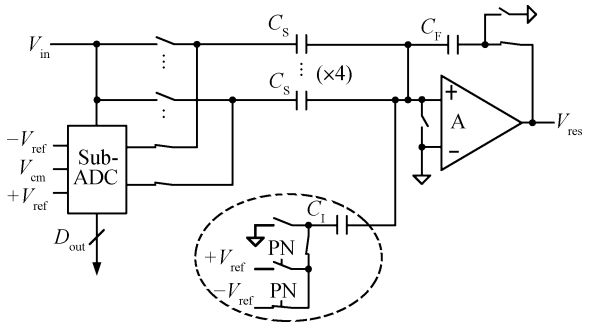

Fig. 4. Implementation of PN sequence injection in the first stage.

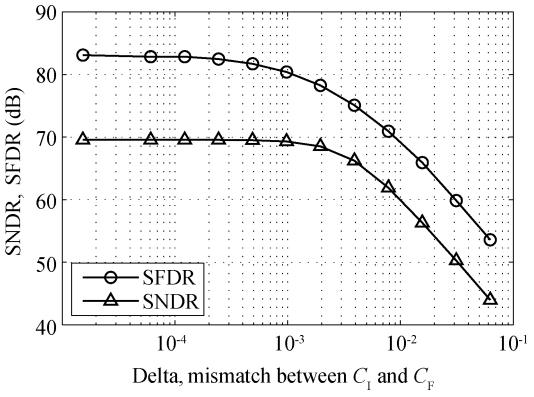

Fig. 5. Simulated ADC performance versus. mismatch of $C_{\rm I}$ and $C_{\rm F}$.

are especially estimated and compensated. In the proposed statistics-based calibration scheme, as shown in Fig. 2, the two transfer modes share the same comparators and range of input signals, thus suffer identical sub-ADC errors, while maintaining the extraction of residual difference at the same input location and avoiding calibration errors.

2.2. Avoiding accurate implementation of $C_{\rm I}$ /$C_{\rm F}$

As indicated in Fig. 4, PN sequence is injected through an extra capacitor $C_{\rm I}$ connected to the opamp input node. During the track phase, the input signal is sampled on capacitors $C_{\rm S}$. During the hold phase, PN sequence is injected through capacitor $C_{\rm I}$ and randomly shifts the transfer curve by the value of $\pm V'_{\rm ref}(C_{\rm I}/C_{\rm F})$, respectively. The size of the feedback capacitor $C_{\rm F}$ is equal to that of $C_{\rm S}$.

In existing designs, the ratio of PN injection capacitor $C_{\rm I}$ to feedback capacitor $C_{\rm F}$ is always set to 1/4[8, 9] to prevent the stage outputs from exceeding the $\pm V_{\rm ref}$ full-scale bounds with PN sequence injection, and to maintain some tolerance on sub-ADC errors. Furthermore, the output range of amplifier is in theory suppressed to within $(-3/4 \cdot V_{\rm ref}, 3/4 \cdot V_{\rm ref})$, which reduces the third-order gain compression error of the stage and improves the ADC linearity.

In digital background calibration, interstage gain errors induced by finite DC gain of opamp is compensated by digital calibration technique by Eq. (3), and calibration parameters b_1 and p_3 are calculated through the ratio of the measured actual value of residual difference voltage h_1 to the reference value of it. In practice, the residual difference voltage is implemented in analog domain, and the imprecision of implementation brings an error term to the reference value of residual difference, which is expressed as $H_1 = k(1 + \delta)$, where k is the design value of $C_{\rm I}/C_{\rm F}$ and δ is the mismatch of $C_{\rm I}$ and $C_{\rm F}$ in the proposed design. In ADC normal operation, the error δ is modulated on calibration parameters b_1 and p_3, which deteriorates the accuracy of digital background calibration. For a pipelined ADC with a total resolution of N-bits and an n-bit first stage, δ should be less than $2^{-(N-n)}$ to guarantee the ADC resolution. The simulated ADC performance versus mismatch of $C_{\rm I}$ and $C_{\rm F}$ is shown in Fig. 5. The simulation is taken on a 12-bit pipelined ADC with a 2-effective-bit first stage under calibration, with circuit nonidealities considered. As indicated in Fig. 5, the ADC maintains 12-bit performance when mismatch between $C_{\rm I}$ and $C_{\rm F}$ is less than or equal to 2^{-10}. When the capacitor mismatch is greater than 2^{-10}, the ADC performance rapidly degrades as the capacitor mismatch increases.

Since the size of $C_{\rm I}$ is 1/4 of $C_{\rm F}$, mismatch between $C_{\rm I}$ and $C_{\rm F}$ is twice of that between $C_{\rm S}$ and $C_{\rm F}$. As described above, mismatch between $C_{\rm I}$ and $C_{\rm F}$ introduces error to the reference value of residual difference voltage $H_1 = 1/4 \cdot (1 + \delta)$. In order to guarantee the calibration accuracy, one approach is to increase the size of $C_{\rm I}$ as well as $C_{\rm F}$ and $C_{\rm S}$ proportionally. This method increases power and area consumption. Another way is to adopt complex circuit techniques, for example, by adding a slow-but-accurate sigma-delta ADC[9]. The problem is that it evidently increases the complexity of analog circuit. Besides, since the incoherence of $C_{\rm I}$ and $C_{\rm F}$ will induce inevitable systematic mismatch, careful layout of $C_{\rm I}$ and $C_{\rm F}$ is required to maintain an excellent capacitor matching accuracy, which increases the layout complexity and parasitics.

In the proposed calibration technique, matching between $C_{\rm I}$ and $C_{\rm F}$ is relaxed by measuring the value of $H_1 = C_{\rm I}/C_{\rm F}$ by the back-end stages of ADC. Since it is a time-invariant variable, the value of H_1 can be measured at the ADC initialization such as power-up or production test, and be stored in ROM for ADC normal operation. In normal operation when digital background calibration is applied, the error δ is eliminated by referring calibration parameters b_1 and p_3 to H_1 instead of to k. Simulated spectrums of the ADC outputs are shown in Fig. 6(a) for the case of no calibration, in Fig. 6(b) for digital background calibration of interstage gain errors only, and in Fig. 6(c) for both digital background calibration and residual difference errors elimination for mismatch between $C_{\rm I}$ and $C_{\rm F}$. In these simulations, the input is a full-scaled 19.1-MHz sine wave, the sampling rate is 40-MS/s, and the mismatch between $C_{\rm I}$ and $C_{\rm F}$ is 2^{-9}. The SFDR improves by 18-dB between the no-calibration and digital background calibration cases and by another 5-dB when residual difference modification is applied,

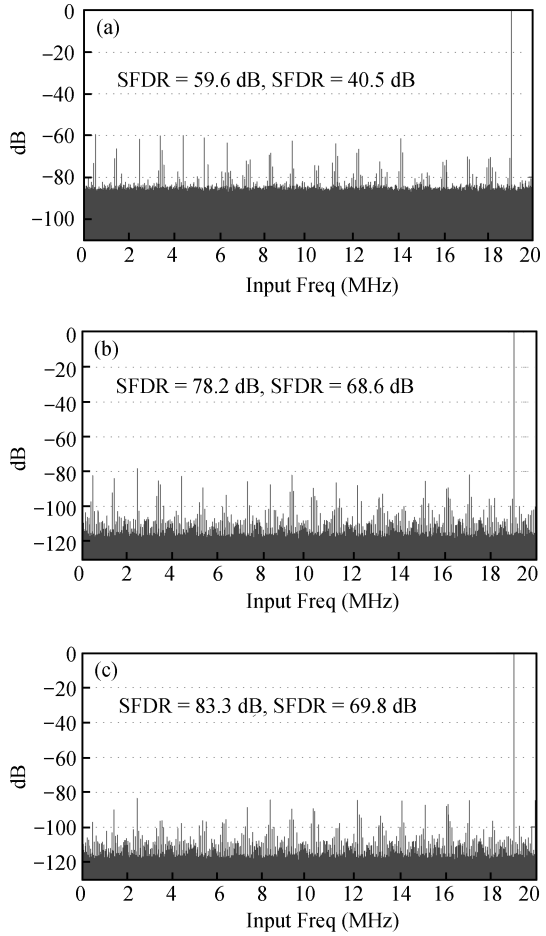

Fig. 6. Simulated output spectrum with 2^{-9} mismatch between C_I and C_F. (a) Without calibration. (b) With digital background calibration for interstage gain errors. (c) With both digital background calibration and residual difference error elimination for mismatch of C_I and C_F.

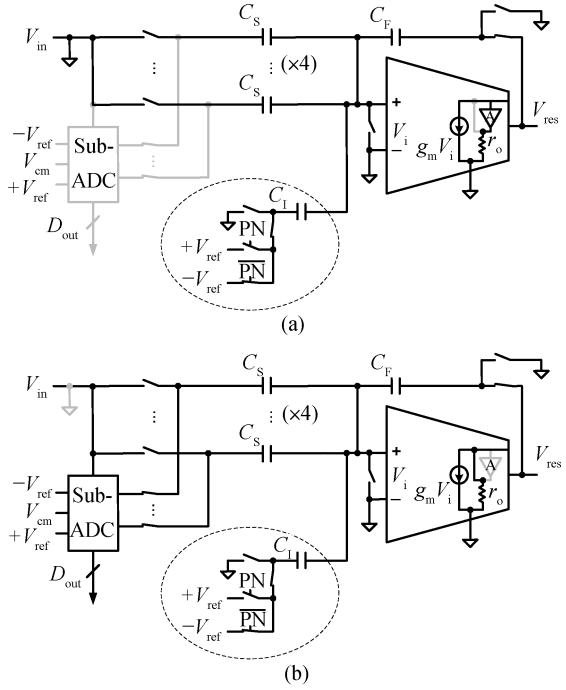

Fig. 7. System configuration. (a) Initialization mode. (b) Operation mode.

	Initialization Mode →	Calibration Mode
Sampling Clock	Hundreds of kHz	Tens to Hundreds of MHz
Object	Foreground calibration for C_I/C_F mismatch	Background calibration for C_S/C_F mismatch & opamp Finite Gain
Opamp	High DC-gain Narrow GBW	Low DC-gain Wide GBW
V_{in}	Short to GND	Connect to the input signal
C_I	Altematively connects to $+V_{ref}$ or $-V_{ref}$	Randomly switches between $+V_{ref}$ and $-V_{ref}$
Calibration Parameter	Stored in ROM	Iteratively updated

Fig. 8. Differences between the initialization mode and the operation mode.

while the SNDR increases by 28-dB with digital background calibration and by another 1-dB to 69.8-dB with residual difference modification.

In the presented design, the measurement of C_I/C_F is achieved by switching the stage under calibration into a slowbut-accurate topology at the initialization mode. Taking the first stage under digital calibration for example, the system configurations are shown in Fig. 7(a) for the initialization mode and in Fig. 7(b) for the operation mode. During the operation mode, the interstage gain errors of ADC are continually compensated by digital background calibration, and the reference value of residual difference voltage is replaced by the value of C_I/C_F stored in ROM. The opamp of the stage operates with a low DC gain and a high bandwidth, and the PN sequence is injected through capacitor C_I. At the initialization mode, the stage is converted into a slow-butaccurate topology to measure the value of C_I/C_F. To make the stage perform an accurate residue gain, a gain-enhancement circuit is connected to the opamp, as shown in Fig. 7(a). It is disconnected and powered off during the ADC normal operation, as shown in Fig. 7(b). The input of the stage is shortened to ground, and capacitor C_I is alternatively connected to reference voltages $+V_{ref}$ or $-V_{ref}$ to convert the value of C_I/C_F to DC voltages, which are to be measured by the back-end stages of ADC. Since both sampling capacitors (C_S) and sub-ADC are bypassed, the error of the measurement contains only of the quantization errors of the back-end ADC, which will approach zero as the amount of digital output sample increases. As described above, the accuracy of C_I/C_F measurement reaches the output resolution of the stage and satisfies the requirement of calibration. Since a small quantity of samples is sufficient for the measurement of the dc signal, the sampling frequency of ADC can be decreased, for instance, to hundreds of kHz to simplify the circuit implementation for the initialization mode, which will be described in detail in Section 3. The differences between the two modes are listed in Fig. 8. In practice, the conversion of two modes is achieved with the help of switches and simple logics.

As described above, the proposed PN injection scheme has several features: low residue output voltage range is produced

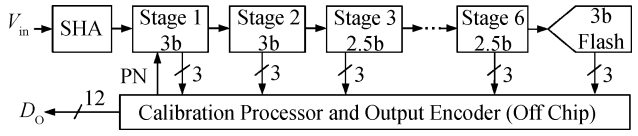

Fig. 9. Block diagram of the ADC prototype.

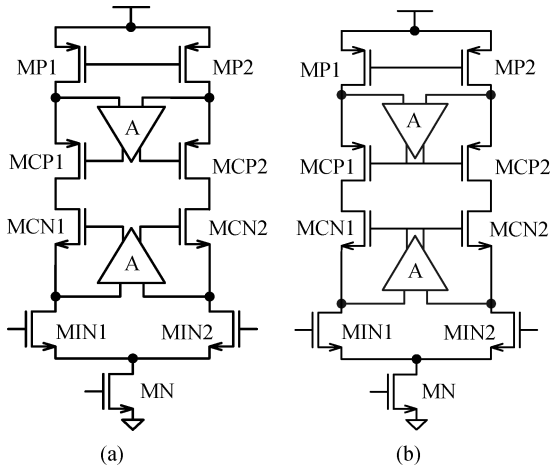

Fig. 10. Schematic of opamp in the first stage. (a) Initialization mode. (b) Operation mode.

to decrease the interstage gain nonlinearity; no additional comparators and digital circuits are used for dithering; the calibration accuracy is insensitive to the sub-ADC errors; and no complex implementation is required in analog domain to ensure the matching accuracy between C_I and C_F.

3. Prototype implementation

3.1. Pipeline structure

To demonstrate the calibration technique described in the previous section, an experimental ADC prototype is implemented. The prototype 12-bit 40-MS/s ADC consists of a sample and hold, two 3-bit stages, four 2.5-bit stages, followed by a 3-bit flash as shown in Fig. 9. The additional 3 bits are used to decrease the quantization error of the back-end ADC. All digital post-processing is implemented off-chip on a PC. In this prototype, only the first stage is designed to employ the proposed calibration scheme, even though the technique can be applied to the following stages as well. In the presented design, the third-order nonlinearity is negligibly small since the 3-bit/stage topology and PN injection scheme have enhanced the ADC linearity.

3.2. Opamp

In general, a single stage telescopic opamp offers excellent bandwidth with less power consumption at the cost of reduced signal swing compared with other types of opamps. In the presented design, the opamp of the first stage operates in two modes controlled by a group of switches. The schematic of opamps in the initialization mode and the operation mode are shown in Figs. 10(a) and 10(b), respectively. At the initialization mode, the ADC operates at a low sampling rate of

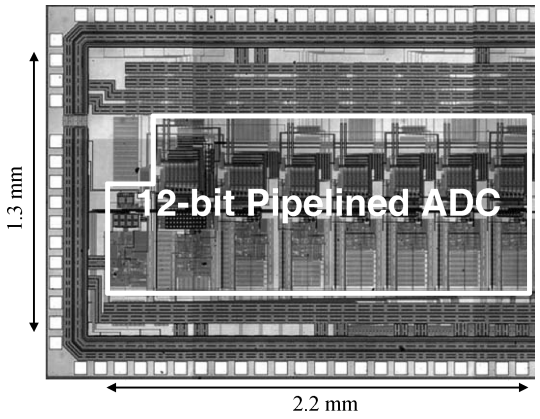

Fig. 11. Micrograph of the prototype ADC.

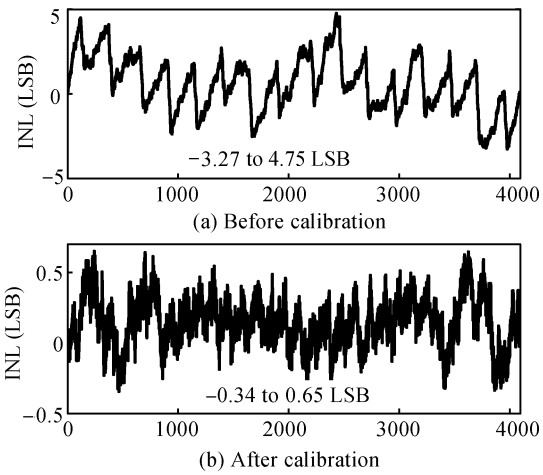

Fig. 12. Measured INL.

Table 1. Measured performance summary.

Parameter	Value	
Technology	0.18 μm CMOS	
Conversion rate	40 MHz	
Resolution	12 bit	
Total power	82.4 mW @ 3.3 V supply	
Core area	1.3 × 2.2 mm^2	
INL/LSB	Without calibration	With calibration
	–3.27 to 4.75	–0.34 to 0.65
SFDR @ f_{in} = 19.1 MHz (dB)	64.1	80
SNDR @ f_{in} = 19.1 MHz (dB)	52.2	66.2
ENOB	8.4	10.7

hundreds of kHz and measures DC voltages with the value of about 1/4 of full swing, thus narrow bandwidth and small output swing of opamps are sufficient. In this situation, the stability as well as voltage headroom of opamps is easy to be guaranteed. This condition gives the chance for gainenhancement techniques such as multi-stage or gain-boosting to be used in opamps to achieve the performance of high DC gain. For opamps with a low bandwidth and a small output swing, such techniques can be adopted in future CMOS technology to accommodate the reduction of power supply and intrinsic gain of MOSFET. In the proposed design, two gain boosters

Table 2. Performance comparison with other ADCs.

ADC	Bits	MS/s	Peak INL before calibration (LSB)	Peak INL after calibration (LSB)	SFDR @ Nyquist Input (dB)	SNDR @ Nyquist Input (dB)	Supply voltage (V)	Technology (μm)	Power** (Analog) (mW)	FOM*** (pJ/step)
Ref. [6]	12	100	2	0.6	75	60	1.8	0.18	196	0.27
Ref. [7]	12	75	19	0.9	76	67	3	0.35	290	0.35
Ref. [12]	12	20	4.21	0.47	80	64	3.3	0.35	226	1.23
Ref. [13]	12	80	20.5	0.24	80	71	2.5	0.25	755	0.81
Ref. [14]	12	75	NM*	0.95	71.2	63.5	3 0	35	273	0.40
This work	12	40	5 0	65	80	66	3.3	0.18	82.4	0.22

*NM: Not Mentioned. **Digital power is excluded. ***FOM = $\dfrac{\text{Power}}{10^{\text{SNDR}/20} \times 2 \times \text{BW}}$.

are connected to the opamp to provide high DC gain (>100 dB) at the initialization mode and are disconnected and powered off to provide a wide bandwidth at a low DC gain (< 60 dB) at the operation mode.

3.3. Measurement results

The ADC is fabricated in a 1P6M 0.18 μm CMOS process with core area of 1.3 × 2.2 mm^2. Figure 11 presents the die photograph. Figure12 shows the measured static performance. With digital background calibration, the INL reduces from 4.75 LSB to 0.65 LSB. Figure 13 shows the measured spectrum with 19.1-MHz input at 40-MS/s sampling frequency. With the proposed calibration, the SFDR improves from 64 to 80 dB and SNDR from 52 to 66 dB with Nyquist input. As indicated in Fig. 14, the ADC achieves more than 65 dB SNDR and above 80 dB SFDR performance within the first Nyquist zone at full sampling rate. After approximately 2^{19} sampling periods, which is about 13 ms for the proposed 12-bit 40-MS/s ADC, it achieves a stable performance with 10.71-bit mean value of ENOB. The measured performance of the ADC is summarized in Table 1, and is compared with performances of other ADCs in Table 2. In order to make it fair, only 12-b ADCs with calibration are compared. In Refs. [12, 13], the ADCs are calibrated in analog domain by nested or bootstrapped techniques, which increases the complexity of analog circuit and the consumption of power and area. Digital background calibration is adopted in Refs. [6, 7, 14] to reduce the complexity of analog circuit. In Ref. [6], the opamp of the stage under calibration is of a gain-boosted structure with a DC gain of 95 dB, which will face more difficulties with future CMOS technology. For high-speed high-resolution ADCs, wide-bandwidth performance of opamps is required. In this case, complicated structures of opamps such as multistage or gain-boosting are strictly limited in normal operation of ADCs due to the stability issues. In future CMOS technology, when power supply and intrinsic gain of MOSFET are reduced, it will be more and more difficult to guarantee high-DC-gain and wide-bandwidth performances for opamps at the same time. Open-loop amplifiers are used in Refs. [7, 14] to accommodate the challenges of future CMOS technology, but due to the bad linearity of the amplifiers, the SFDR of ADCs reach only 76 dB in Ref. [7] and 71.2 dB in Ref. [14] with Nyquist input frequency. This work adopts a single stage telescopic opamp with a DC gain of 58 dB for ADC normal operation, and the SFDR of ADC achieves

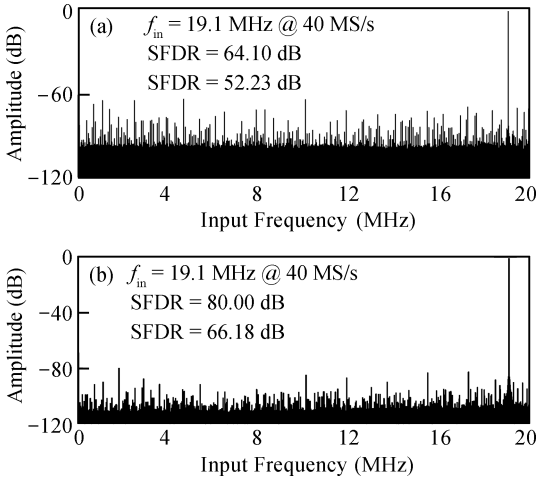

Fig. 13. Measured spectrum with a 19.1 MHz input at 40 MS/s. (a) Before calibration. (b) After calibration.

80 dB with Nyquist input. In this approach, a simple structure of opamp with low DC gain is allowed, thus is more compatible to the future CMOS technology. Besides, the proposed design also has some advantages on digital background calibration technique. In Ref. [6], the calibration operates when the amplitude of input signal is greater than $(-3/8 \cdot V_{\text{ref}}, +3/8 \cdot V_{\text{ref}})$, which is twice larger than that in this work. In Refs. [7, 14], the calibration accuracy is sensitive to sub-ADC errors, and it requires 1-bit redundancy in the following stage to accommodate the overrange of the stage residue output. As shown in Table 2, the presented ADC achieves the lowest FOM value. It achieves the best linearity performance with low power, low complexity of analog circuit, and high compatibility to the future CMOS technology, thus is the most efficient design among them.

4. Conclusions

A 12-bit 40-MS/s pipelined ADC with two-mode digital calibration has been described in this paper. The presented calibration scheme can correct both finite DC gains of opamps and capacitor mismatches. It is robust and simple since the calibration accuracy is insensitive to sub-ADC errors, the ADC design is compatible with future CMOS technology, and it has a low complexity of analog circuits. Adopting an opamp with a DC gain of 58-dB during the ADC normal operation, the ADC

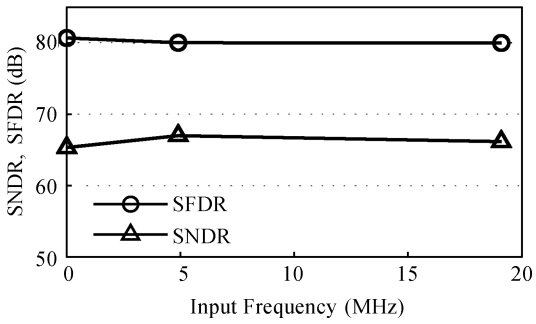

Fig. 14. ADC performance versus input frequency.

achieves 80-dB SFDR and 66-dB SNDR with Nyquist input frequency at full sampling rate.

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