High resolution interface circuit for closed-loop accelerometer*

Yin Liang(尹亮)[1,†], Liu Xiaowei(刘晓为)[1,2], Chen Weiping(陈伟平)[1,2], and Zhou Zhiping(周治平)[1]

[1]Department of Microelectronics, Harbin Institute of Technology, Harbin 150001, China
[2]Key Laboratory of Micro-Systems and Micro-Structures Manufacturing, Ministry of Education, Harbin 150001, China

Abstract: This paper reports a low noise switched-capacitor CMOS interface circuit for the closed-loop operation of a capacitive accelerometer. The time division multiplexing of the same electrode is adopted to avoid the strong feedthrough between capacitance sensing and electrostatic force feedback. A PID controller is designed to ensure the stability and dynamic response of a high Q closed-loop accelerometer with a vacuum package. The architecture only requires single ended operational amplifiers, transmission gates and capacitors. Test results show that a full scale acceleration of ± 3 g, non-linearity of 0.05% and signal bandwidth of 1000 Hz are achieved. The complete module operates from a ± 5 V supply and has a measured sensitivity of 1.2 V/g with a noise of floor of 0.8 $\mu g/\sqrt{\text{Hz}}$ in closed-loop. The chip is fabricated in the 2 μm two-metal and two-poly n-well CMOS process with an area of 15.2 mm^2. These results prove that this circuit is suitable for high performance micro-accelerometer applications like seismic detection and oil exploration.

Key words: closed-loop accelerometer; interface circuit; switched capacitor; low noise
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1. Introduction

In the past few years, there has been an increasing demand for low noise and small form-factor micro-g capacitive accelerometers for a number of applications, including inertial measurement units, low-frequency vibration measurements, and earthquake detection. The capacitive accelerometer for oil exploration needs to have a high dynamic range (> 120 dB), which compels the interface circuit to resolve 10^{-8} capacitive change of rest capacitance.

To realize a high stability, high linearity, and wide bandwidth accelerometer, the technique of electrostatic force feedback is adopted. The traditional control method is that the mass proof is controlled closed-loop by independent feedback electrodes, which reduces the area of sensing capacitors and makes the mechanical structure complex[1]. Another method is that the electrostatic feedback frequency is separated from the charge pick-up frequency by modulation without independent feedback electrodes, but it is difficult to separate the drive and sense operation entirely in the time domain[2]. The third method is sigma–delta modulation. The merit of the method is that we can achieve digital output directly. The demerit is that we have to design a high order structure of a closed-loop accelerometer in order to achieve a high dynamic range, which is very difficult to control the stability of the closed-loop accelerometer. Furthermore, the accelerometer is often packaged in vacuum to achieve sub micro-g resolution (mechanical noise is lower than 1 $\mu g/\sqrt{\text{Hz}}$, but decreasing the noise density decreases the mechanical damp coefficient, and the stability is more difficult to control[3]. In this paper, we adopt the time division multiplexing of capacitance sensing and electrostatic forcing at the middle electrode. The strong driving feedthrough is avoided by separating the drive and sense operation in the time domain, while using the same electrodes. By electrostatic force feedback of the PID circuits, we change the damp coefficient and spring coefficient of the closed-loop accelerometer to ensure the linearity and stability of the accelerometer.

The most common readout circuit for micromachined differential capacitive sensors is based on a fully differential charge sensitive amplifier. In this way, the voltage step is applied at the common node, and the charge difference is integrated into a fully differential integrator. This circuit is rather complex to implement since a fully differential operational amplifier with internal common node feedback is required. Further, an additional operational amplifier is required to control the common mode level at the differential amplifier inputs[4]. The proposed architecture only requires single ended operational amplifiers, transmission gates and capacitors. Further, a structure of high loop gain and force feedback is designed for suppression of $1/f$ noise of the amplifier, charge injection and clock feedthrough effects in the back-end circuits.

2. Interface circuits of closed-loop accelerometer

2.1. Topology

Figure 1 illustrates a capacitive accelerometer and interface circuits. The sensor includes a body including a top cover, a bottom cover, and a central mass supported by springs from a generally rectangular frame that receives the central mass therein between the top plate and the bottom plate. The sensing structure of the silicon accelerometer is a second order dynamic system whose equation of motion can be written as

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† Corresponding author. Email: yinliang2003@126.com
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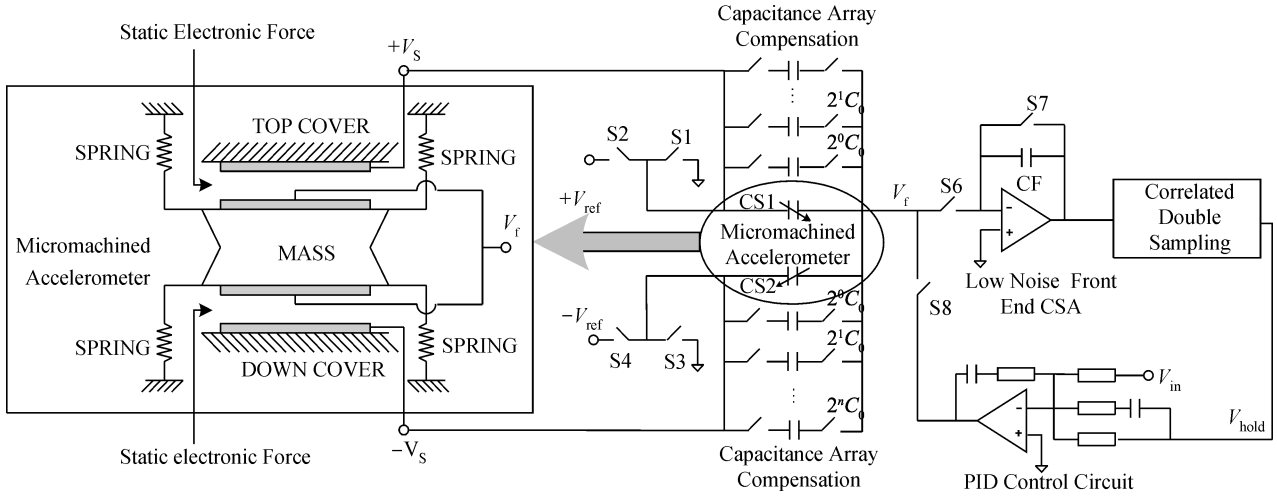

Fig. 1. Schematic of interface circuit for a closed-loop accelerometer.

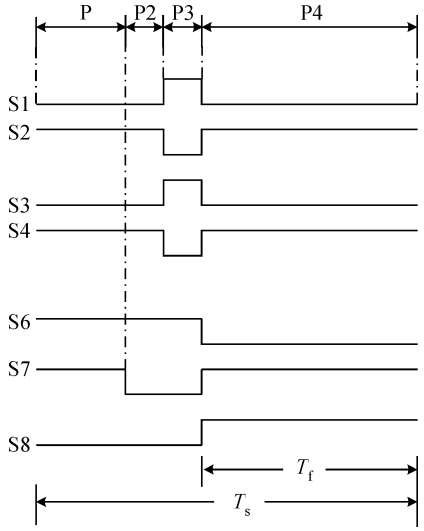

Fig. 2. Clock diagram for the switched-capacitor interface circuit for the accelerometer.

$$M\frac{\mathrm{d}^2x}{\mathrm{d}t^2}+b\frac{\mathrm{d}x}{\mathrm{d}t}+kx=Ma(t), \tag{1}$$

where M is the proof mass, b is the damping coefficient, k is the spring coefficient, x is the displacement of proof mass, and $a(t)$ is the applied acceleration. To improve the linearity and the dynamic range, a servo accelerometer with electrostatic force-balancing has been designed, as shown in Fig. 1. Figure 2 shows the clock diagram of the feedback control circuit. Each cycle starts with the end of the forcing period and begins with the first of several sensing phases. Each cycle includes four phases, namely, clear, autozero, sense, and drive. A structure of high loop gain and force feedback is proposed to achieve a high SNR. It suppresses the effects of the $1/f$ noise and offset voltage of the op-amp, as well as the kT/C charge noise from the parasitic capacitor, by using the CDS (correlated double sampling) technique and implementing large area PMOS transistors at the CSA (charge sensing amplifier) input stage. It also reduces charge injection and clock feedthrough effects.

2.2. Interface circuit overview

The operation of this sense interface involves four phases, namely, clear, autozero, sense, and drive. Figure 3 shows the simplified configurations of the sense amplifier in four respective phases. The clear phase [Fig. 3(a)] resets the input electrode voltage of the sense interface to ensure a correct bias point and discharges the capacitors to erase the memory from the previous cycle. During the autozero phase [Fig. 3(b)], the amplifier offset and flicker noise are amplified and stored in and to be subtracted in the subsequent sense phase. The top and bottom electrode voltages are, respectively, kept at V_s and $-V_s$. During the sense phase [Fig. 3(c)], electrodes voltage transit from $\pm V_s$ to zero. A small differential charge that is proportional to the input acceleration is produced and flows onto the integrating capacitor C_F, and the output of the sample and hold circuit is expressed as

$$V_{\mathrm{hold}}=\frac{V_S(C_{S1}-C_{S2})}{C_F}. \tag{2}$$

During the drive phase [Fig. 3(d)], electrode voltages are reset back to $\pm V_s$ to improve the voltage-to-force transduction. When an external acceleration a_{in} is applied to the accelerometer, the product of the electrostatic force and the time of feedback T_f equals the product of the external acceleration, the proof mass and the periodic time T_S.

$$F_f=\left[\frac{1}{2}\frac{\partial C_{S1}}{\partial x}(V_S-V_f)^2-\frac{1}{2}\frac{\partial C_{S2}}{\partial x}(V_S+V_f)^2\right]T_f\approx a_{in}MT_S, \tag{3}$$

where C_{S1}, C_{S2} is the rest capacitance of the accelerometer, x is the displacement of the proof mass, V_S is the supply voltage, T_f is the time of feedback of the electrostatic force, and T_S is the periodic time of sensing and feedback. As the open-loop gain of the accelerometer is large, the displacement of proof mass equals zero approximately. So we can consider approximately that $C_{S1}=C_{S2}=C_S$, and the sensitivity of the capacitive closed-loop accelerometer is

$$S=\frac{V_f}{a_{in}}=\frac{dMT_S}{2C_SV_ST_f}, \tag{4}$$

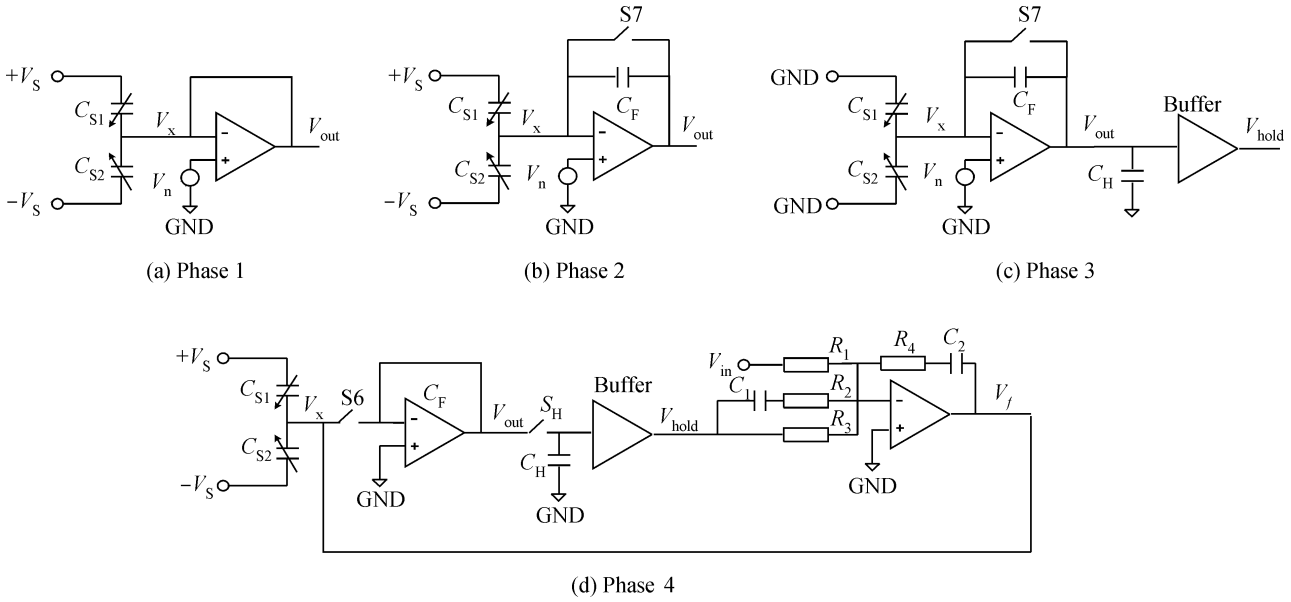

Fig. 3. Four-phase operation of capacitive sense interface circuit.

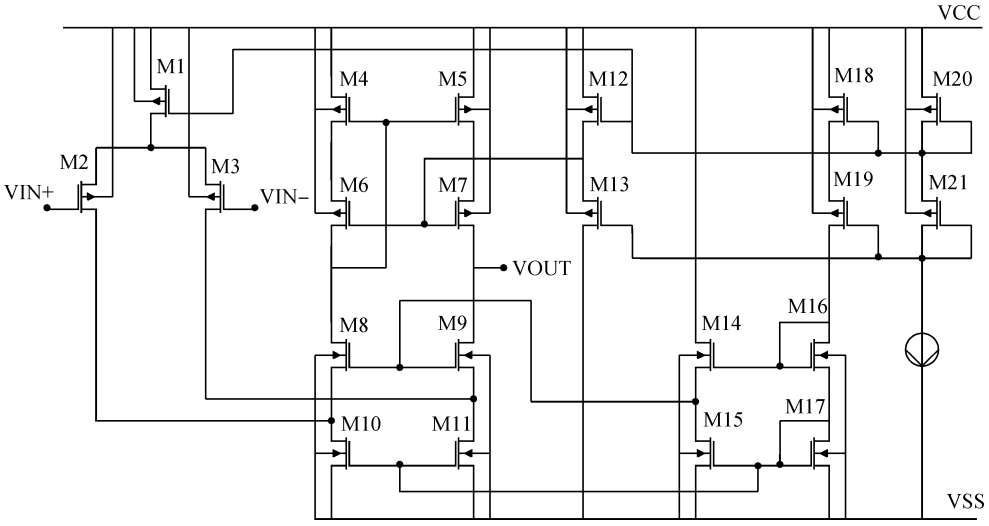

Fig. 4. Schematic view of the amplifier used in the front-end circuit.

where C_S is the rest capacitance, d is the space length of the capacitive polar plate, and M is the proof mass.

2.3. Charge sensitive amplifier

Figure 4 shows a schematic of the amplifier used in the front-end of the switched capacitor circuit. This is a single ended folded-cascode amplifier. The transistors in the biasing path do not contribute any noise. Transistors M6–M9 do not affect the total noise either, due to the large impedance in the source of these devices. The input-referred noise contribution of the remaining transistors can be derived by multiplying the noise power by the square of the ratio of that device's transconductance to the input device's transconductance. Therefore, the input-referred noise can be expressed as

$$e_n^2 \approx \frac{16k_BT}{3g_{m1}}\left(1+\frac{g_{m4}+g_{m10}}{g_{m1}}\right) \approx \frac{16k_BT}{3g_{m1}}, \quad (5)$$

where g_{m1}, g_{m4}, and g_{m10} are the transconductances of transistors M1, M4, and M10. The DC gain of the amplifier is 80dB so that the magnitude error is usually negligible. The bandwidth ω_0 of the charge sensing amplifier should be at least four times as large as the clock frequency so that the op-amp has enough time to settle[5]. To avoid unnecessary noise aliasing, ω_0 should not be chosen much larger than this value, which will be discussed in Section 3. In this paper, the unity gain bandwidth of the folded-cascode amplifier is 20 MHz.

2.4. PID feedback circuit

Figure 5 shows a schematic of the PID feedback circuit. The three-stage amplifier with capacitance feedback compen-

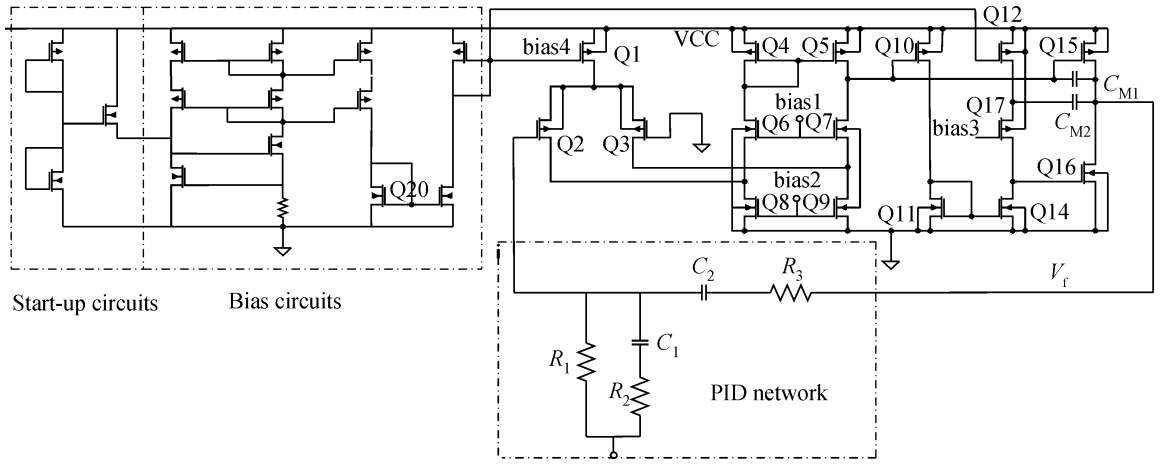

Fig. 5. Schematic of PID feedback circuit.

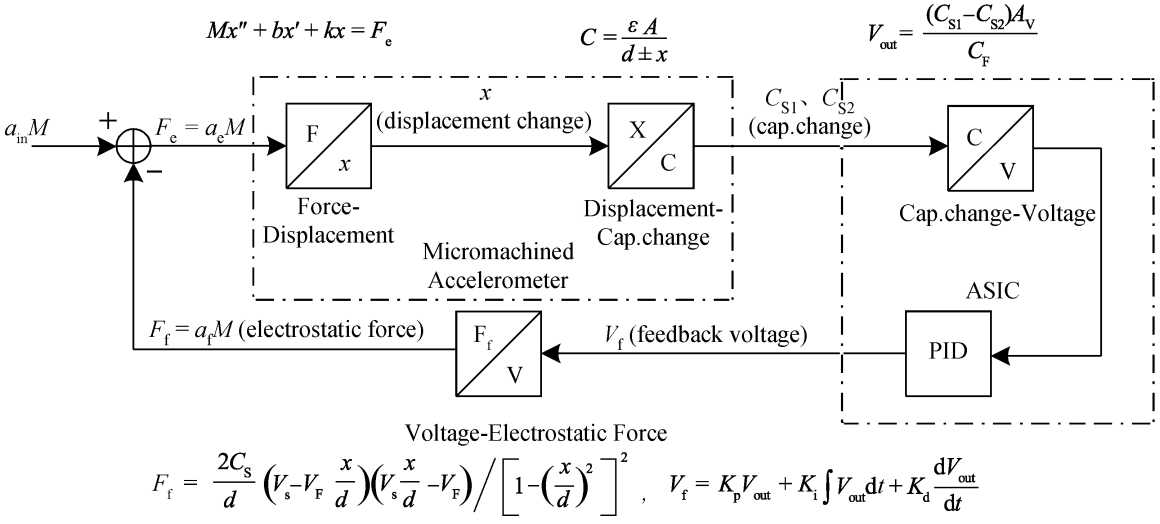

Fig. 6. Linear model of the closed-loop accelerometer.

sation is adopted. C_{m1} is the Miller capacitor forming the outer feedback loop. Capacitance C_{m2} along with the transconductance stage g_{m17} makes up the internal feedback loop[6]. The amplifier has more than 100 dB open-loop gain, which ensures the linearity and bias stability of the accelerometer. The transfer function of the PID circuit is

$$H_{PID}(s) = K_p + \frac{K_i}{s} + \frac{K_d s}{\frac{s}{\beta} + 1}$$
$$= \left(\frac{R_3}{R_1} + \frac{C_1}{C_2}\right) + \frac{1/R_1C_2}{s} + \frac{(R_3C_1 - R_2C_1^2/C_2)s}{R_2C_1s + 1}. \quad (6)$$

Because $C_2 \gg C_1$, so the resistance R_1, R_3 form the proportional part of the PID circuits, and R_1, C_2 form the integrator of the PID circuit. The resistance R_3 and the capacitor C_1 form the differentiator of the PID circuit approximately.

2.5. Transfer function and stability

The stability of the low noise accelerometer is crucial because the damp coefficient of the accelerometer is low in the vacuum package. To achieve the desired system behavior and dynamics, we adjust the closed-loop damp coefficient and spring coefficient by designing the coefficient of the PID control circuit carefully. The equivalent equation of the closed-loop accelerometer is

$$Mx'' + (b + b_e)x' + (k + k_e)x = a_{EXT}M, \quad (7)$$

where M is the proof mass, b is the damping coefficient, k is the spring coefficient, x is the displacement of the proof mass, and $a(t)$ is the applied acceleration. The proportional controller and integrator of the PID circuits are equivalent to the electric spring coefficient k_e, which improves the linearity of the accelerometer and prevents the bias drift from the process of the integrated circuits. The differentiator of the PID circuit is equivalent to the electric damp coefficient b_e, which ensures the stability of the accelerometer.

The linear model of the closed-loop accelerometer is shown in Fig. 6. The closed-loop stability of the accelerometer is usually dependent on the pole-zero location of the open-loop small-signal transfer function. The open-loop transfer function

for the accelerometer is

$$H(s) = \frac{A_0\left(\frac{s}{\omega_4}+1\right)\left(\frac{s}{\omega_5}+1\right)}{s\left(\frac{s}{\omega_1}+1\right)\left(\frac{s}{\omega_2}+1\right)\left(\frac{s}{\omega_3}+1\right)}, \tag{8}$$

$$p_0 = 0, \tag{9}$$

$$\omega_{1,2} = \frac{b \pm \mathrm{j}\sqrt{b^2 - 4Mk}}{2M}, \tag{10}$$

$$\omega_3 = \frac{1}{R_2 C_1}, \tag{11}$$

$$\omega_4 = \frac{1}{R_3 C_2}, \tag{12}$$

$$\omega_5 = \frac{1}{(R_1 + R_2)\, C_1}. \tag{13}$$

The dominant pole of the open-loop accelerometer is zero, and the phase variation of the dominant pole is compensated by zero ω_4. When the damp coefficient of the accelerometer is very low, pole ω_1 and ω_2 become a pair of complex poles. The imaginary part of the complex poles equals the resonant frequency ω_n of the accelerometer approximately.

$$\omega_\mathrm{n} = \sqrt{\frac{k}{M}}. \tag{14}$$

At the resonant frequency, the phase of the transfer function changes 180 ℃ approximately, which results in instability of the closed-loop accelerometer. We set the zero ω_5 smaller than the resonant frequency to compensate the changed phase of the complex poles, and set the pole ω_3 much larger than the resonant frequency to ensure the stability of the closed-loop accelerometer. Figure 7(a) shows the bode diagram of the open loop and closed-loop accelerometer, which proves that the closed-loop mode with PID spreads the bandwidth and reduces the quality factor of the accelerometer. Figure 7(b) shows the step response of the open loop and closed-loop accelerometer. The settling time and overshoot of the closed-loop accelerometer is 0.002 s and 32% respectively, which is much better than that of the open-loop accelerometer.

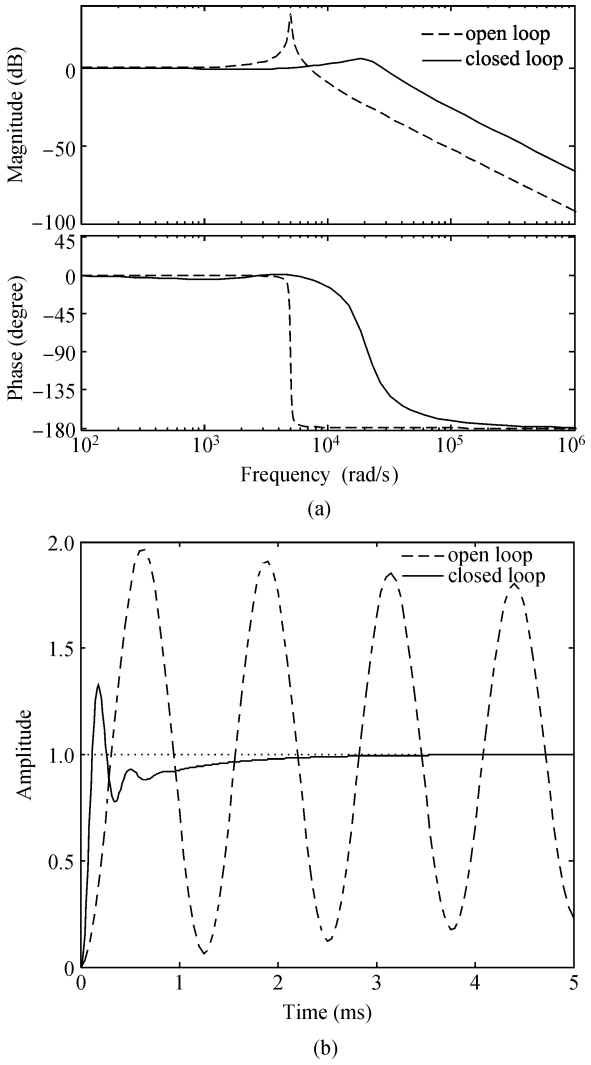

Fig. 7. Bode diagram and step response of the open-loop and closed-loop accelerometer. (a) Bode diagram of the open-loop and closed-loop accelerometer. (b) Step response of the open-loop and closed-loop accelerometer.

3. Noise analysis

3.1. Mechanical (Brownian) noise

Mechanical noise is generated by the proof mass itself. This Brownian noise corresponds to an equivalent acceleration noise,

$$a_\mathrm{n}^2 = \frac{4k_\mathrm{B}TB}{M}, \tag{15}$$

where k_B is the Boltzman's constant, T is the temperature in Kelvin, B is the damping coefficient in (N·m/s), and M is the proof mass. As the equation shows, this noise is totally dependent on the system mass and damping coefficient. In this paper, we adopt an accelerometer packaged in a vacuum environment, and the noise density of the accelerometer is less than 0.5 $\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$.

3.2. Front-end amplifier noise

The front-end amplifier noise includes two parts: thermal and flicker noise. Since CDS is employed in the switched-capacitor circuit, the amplifier flicker noise is reduced considerably, and hence the thermal noise is the dominant source. The expression of the thermal noise is in Eq. (5). Figure 8 shows the simplified diagram for the switched capacitor implementation of this amplifier for noise calculation. The amplifier thermal noise is sampled and folded and also filtered by the amplifier in this loop. The equivalent noise at the output of this circuit is

$$\begin{aligned} e_\mathrm{Amplifier} &= \sqrt{\frac{8k_\mathrm{B}T(C_\mathrm{S}+C_\mathrm{P}+C_\mathrm{F})}{3C_\mathrm{F}(C_\mathrm{F}+C_\mathrm{out})f_\mathrm{S}}} \\ &\approx \frac{1}{C_\mathrm{F}}\sqrt{\frac{8k_\mathrm{B}\mathrm{T}(C_\mathrm{S}+C_\mathrm{P}+C_\mathrm{F})}{3f_\mathrm{S}}} \quad (\mathrm{V}/\sqrt{\mathrm{Hz}}), \end{aligned} \tag{16}$$

Table 1. Theory value of electric noise density.

Noise source	Expression	Theory value
Mechanical noise	$a_n^2 = \frac{4k_BTB}{M}$	< 500 ng/$\sqrt{\text{Hz}}$
Front-end amplifier noise	$e_{\text{Amplifier}} = \frac{1}{C_F}\sqrt{\frac{8k_BT(C_S + C_P + C_F)}{3f_S}}$	1.4×10^{-7} V/$\sqrt{\text{Hz}}$
Reference voltage noise	$e_{RV} \approx \frac{V_n}{C_F}\sqrt{\frac{g_mC_S}{f_S}}$	9.8×10^{-7} V/$\sqrt{\text{Hz}}$
Switch resistance noise	$e_{SW} = \frac{1}{C_F}\sqrt{\frac{2k_BTR_{SW}g_mC_S}{f_S}}$	1.8×10^{-7} V/$\sqrt{\text{Hz}}$

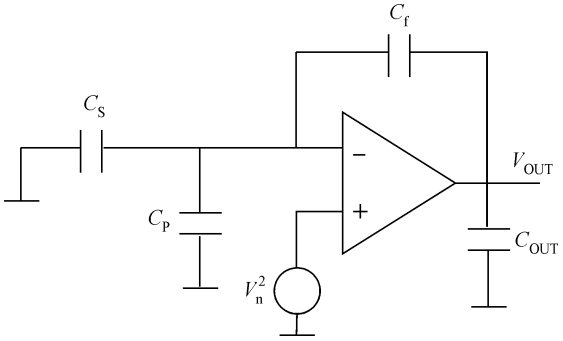

Fig. 8. Simplified schematic view of the readout circuit for the equivalent thermal noise calculation.

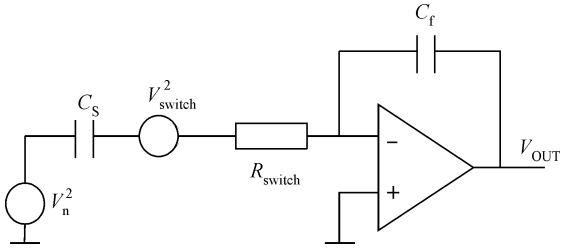

Fig. 9. Simplified schematic for SCRV noise and switch resistance thermal noise analysis.

where f_S is the sampling frequency. In Ref. [7], it is said that the equivalent noise due to amplifier thermal noise is independent of transistor parameters. This is mainly dependent on the capacitance values and sampling frequency. By increasing the sampling frequency and the integration capacitance, it is possible to reduce this noise. In fact, the input transconductance g_m has to be increased in order to set up a signal accurately when the sampling frequency or the value of C_f is increased.

3.3. Charging reference voltage noise

Sensor readout is performed by charging the sense capacitance with a fixed reference voltage in each cycle and detecting this charge by the interface electronics. Therefore, any noise on this reference voltage directly contributes to the overall noise performance, which is known as sensor charging reference voltage noise. Large, low-frequency components of this noise can easily dominate the system noise performance, while wide-band noise is folded to the base band due to sampling on the sense capacitor. Figure 8 shows the simplified circuit schematic for calculation of this noise. Note that, in this case, the finite bandwidth of the amplifier limits the noise bandwidth. The output equivalent noise can be represented by Eq. (17), which is different from Ref. [7] because $f_c \gg f_u$.

$$e_{RV} = \frac{C_SV_n}{C_F}\sqrt{\frac{2\pi C_Ff_u}{C_{Tf_S}}} \approx V_nC_F\sqrt{\frac{g_mC_S}{f_S}}\ (\text{V}/\sqrt{\text{Hz}}), \quad (17)$$

where f_u is the bandwidth of amplifier and V_n is the noise density of the charging reference voltage.

$$f_c = \frac{1}{2\pi R_{SW}C_S}. \quad (18)$$

3.4. Switch resistance noise

Switch resistance between the sense capacitors and the charge integrated also contributes white noise to the sensor output. The simplified schematic for switch resistance noise is given in Fig. 9. If the closed-loop integrator bandwidth f_u is less than f_c in Eq. (18), the noise due to switch resistance will be reduced to

$$e_{SW} = \frac{2C_S}{C_F}\sqrt{\frac{\pi k_BTR_{SW}f_uC_F}{f_S(C_S + C_P + C_F)}} \approx \frac{1}{C_F}\sqrt{\frac{2k_BTR_{SW}g_mC_S}{f_S}}\ (\text{V}/\sqrt{\text{Hz}}), \quad (19)$$

where R_{SW} is the resistance value of the switch. Equation (19) shows that noise from the switch resistance may be attenuated by making R_{SW} small. The switch resistance should also be made small to ensure $f_c \gg f_u$, so settling is limited by the charge integrator.

As can been seen from Table 1, the dominant noise source is reference voltage noise. The circuit has a calculated noise floor of 0.2 μg/$\sqrt{\text{Hz}}$, resulting in a capacitance resolution of better than 10 aF. Referring to Eqs. (2) and (16)–(19), the SNR of the interface circuit is

$$\text{SNR} = \frac{2\Delta C\,V_S/C_F}{\sqrt{e_{\text{Amp}}^2 + e_{RV}^2 + e_{SW}^2}} \approx \lambda\frac{\Delta C}{\sqrt{C_S}}, \quad (20)$$

where ΔC is the capacitive sensitivity of 1 gravity change and C_S is the rest capacitance of the accelerometer. From Eq. (20), it

Table 2. Performance parameters of the hybrid system.

Hybrid system	Parameter	Value
CMOS readout electronics	Sensitivity	10–50 (open-loop) V/pF
	Resolution	< 10 aF
MEMS accelerometer	Rest capacitance	180 pF
	Sensitivity	10 pF/g
MEMS device and interface circuit module	Sensitivity	1200 mV/g
	Full scale	±3 g
	Bandwidth	> 1000 Hz
	Noise density	0.8 $\mu g/\sqrt{Hz}$
	Non-linearity	0.05%

Table 3. Correspondence value of MCy and yield.

	Sensing method	Control method	Rest capacitance (pF)	Sensitivity (pF/g)	Noise floor ($\mu g/\sqrt{Hz}$)	Resolution
Ref. [3]	Continuous time	Open-loop	0.02	4×10^{-4}	50	10^{-6}
Ref. [7]	Switched-capacitor	Open-loop	38	4.9	1.08	1.4×10^{-7}
Ref. [1]	Switched-capacitor	Delta–sigma	12.7	5	4.0	1.6×10^{-7}
Ref. [2]	Continuous time	Closed-loop	12	3.8	0.3	9×10^{-8}
This work	Switched-capacitor	Closed-loop	180	10	0.8	4×10^{-8}

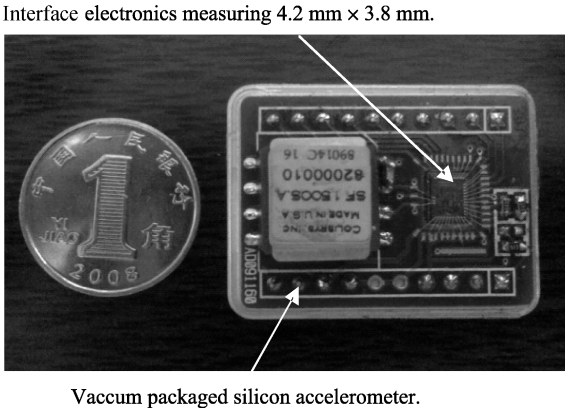

Fig. 10. Hybrid packaged accelerometer and the interface chip.

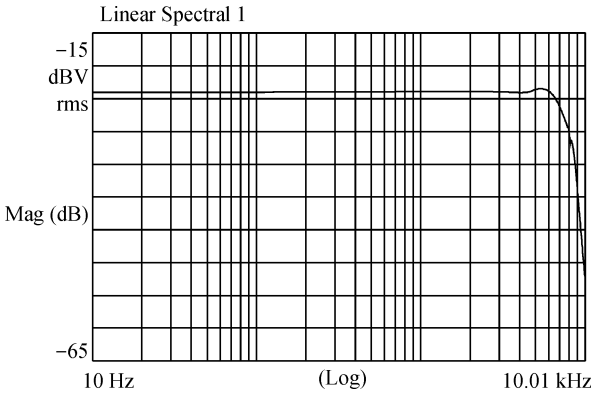

Fig. 11. Transfer function of the closed-loop accelerometer.

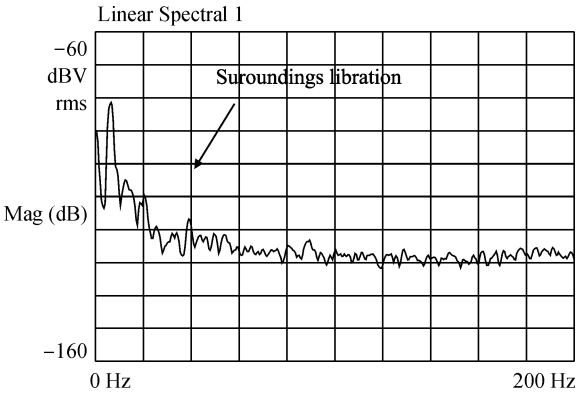

Fig. 12. Noise spectrum of the hybrid system.

is difficult to resolve much less changed capacitance when the rest capacitance C_S is large. Therefore, the resolution of the least capacitance relative to the rest capacitance is viewed as the merit to quantify the performance of the interface circuits, which is expressed as

$$\text{Resolution} = \frac{\Delta C_{MIN}}{C_S}, \tag{21}$$

where ΔC_{MIN} is the least resolved capacitance.

4. Hardware measurements

Figure 10 shows the hybrid packaged accelerometer of the interface chip in a 20-pin IC package. The mechanical part of the accelerometer is SF1500 with the vacuum package from Colibrys Inc. The interface chip of the accelerometer is fabricated in a 2 μm two-metal and two-poly n-well CMOS process with an area of 15.2 mm^2. Table 2 shows the performance parameters of the hybrid system. Test results show that a full scale acceleration of ±3 g and a signal bandwidth beyond 1000 Hz are achieved. The complete module operates from a ±5 V supply and has a measured sensitivity of 1.2 V/g with a noise of floor of 0.8 $\mu g/\sqrt{Hz}$ in closed-loop operation. The transfer function of the closed-loop accelerometer is shown in Fig. 11. The output noise of the hybrid module is measured by using an HP35670 dynamic signal analyzer, as shown in Fig. 12.

Table 3 lists a performance comparison of this work and

that of some state-of-art interface circuits of the accelerometer. Compared with the continuous time method of voltage sensing in Ref. [3], the proposed interface circuit is not affected by parasitic capacitance at the sensing electrode. The interface circuits of Ref. [7] achieve a low noise density in open-loop, but the circuit is very complex and it only achieves 10 $\mu g/\sqrt{Hz}$ noise density in closed-loop. Compared with the delta–sigma structure with a 95 dB measure range in Ref. [1], the dynamic range of the proposed interface circuit is beyond 120 dB. Compared with the continuous time interface circuits in Ref. [2], the proposed interface circuit does not need the complex sinusoidal generator and high pass filter, and the strong driving feedthrough is avoided by separating the drive and sense operation in the time domain.

5. Conclusion

This paper reports a low noise switched-capacitor CMOS interface circuit for the closed-loop operation of a capacitive accelerometer. The principle, stability, and noise density of an analog closed-loop accelerometer are presented. The time division multiplexing of the same electrode is adopted to avoid the strong feedthrough between capacitance sensing and electrostatic force feedback. Test results shows that a full scale acceleration of ± 3 g, non-linearity of 0.05% and signal bandwidth of 800 Hz are achieved. The complete module operates from a ± 5 V supply and has a measured sensitivity of 1.2 V/g with a noise of floor of 0.8 $\mu g/\sqrt{Hz}$ in closed-loop. The chip is fabricated in the 2 μm two-metal and two-poly n-well CMOS process with an area of 15.2 mm^2.

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