A differential low-voltage high gain current-mode integrated RF receiver front-end*

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Abstract: A differential low-voltage high gain current-mode integrated RF front end for an 802.11b WLAN is proposed. It contains a differential transconductance low noise amplifier (G_m-LNA) and a differential current-mode down converted mixer. The single terminal of the G_m-LNA contains just one MOS transistor, two capacitors and two inductors. The gate–source shunt capacitors, C_{x1} and C_{x2}, can not only reduce the effects of gate–source C_{gs} on resonance frequency and input-matching impedance, but they also enable the gate inductance $L_{g1,2}$ to be selected at a very small value. The current-mode mixer is composed of four switched current mirrors. Adjusting the ratio of the drain channel sizes of the switched current mirrors can increase the gain of the mixer and accordingly increase the gain of RF receiver front-end. The RF front-end operates under 1 V supply voltage. The receiver RFIC was fabricated using a chartered 0.18 μm CMOS process. The integrated RF receiver front-end has a measured power conversion gain of 17.48 dB and an input referred third-order intercept point (IIP3) of –7.02 dBm. The total noise figure is 4.5 dB and the power is only 14 mW by post-simulations.

Key words: low voltage; current mode; RF front end; transconductance LNA; switched current mirror
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1. Introduction

Recently, there have been significant developments in low voltage CMOS integrated receivers due to the high demand for increased battery life and lower cost solutions for applications such as Bluetooth and IEEE 802.11b[1]. There have been several reported implementations of the CMOS low voltage RF receiver the last few years[1–8]. However, these circuits belong to voltage-mode circuits. In voltage-mode circuits, the LNA converts the RF input voltage to current and then back into voltage, and the mixer converts the LNA output voltage into current for mixing and then converts the current into voltage for output. Thus, there are two V–I (voltage–current) conversions and two I–V (current–voltage) conversions, which means that the RF receiver has a complex structure, a high supply voltage and a deteriorative linearity.

Recently, current-mode RF receivers have been reported[9–11]. In current-mode RF receivers, the output current from the LNA is directly connected to the input of the current-mode mixer, there is no I–V conversion at the output terminal of the LNA and no V–I conversions at the input of the mixer required. Current-mode RF receivers have simpler architectures, a lower supply voltage and better linearity. Reference [9] proposed a current-mode RF receiver front-end which is composed of an LNA and a mixer. There are no I–V and V–I conversions at the interface of LNA and mixer. The circuit has a cascode structure, where the LNA and the mixer are stacked between a positive supply voltage and ground; therefore it needs high supply voltage of 2.7 V. Reference [10] realized the low voltage current-mode RF receiver front-end. The current from the LNA is coupled to the core of a Gilbert mixer by basic current mirrors, and there are no current-source transistors so as to reduce the number of stacked transistors. However, it still needs a higher supply voltage, which is 1.5 V when using a traditional Gilbert mixer core. Moreover, it has a very low IIP3, which is just –20.56 dBm. In 2010, Cheng *et al.*[11] presented a low voltage current-mode CMOS integrated receiver front-end which has a supply voltage of 1 V. It uses a G_m-LNA to produce the output current and the current is flowed into a current-mode mixer. The circuit has a cascaded structure, where the G_m-LNA and the mixer are folded, so it can operate under a very low supply voltage of just 1 V. This structure can also eliminate unnecessary I–V and V–I conversions, which makes the circuit simpler, the supply voltage lower and the linearity better. However, the mixer is still an improved Gilbert mixer, which substitutes RF current signal for RF voltage signal and eliminates the MOS transistor. It has a lower overall power conversion gain of just 11.4 dB and a higher noise figure of 5.87 dB. Moreover, circuit's LNA has a more complex two-stage structure.

In this paper, we propose a new differential low voltage current-mode RF receiver front-end with high gain. It contains a differential G_m-LNA and a differential current-mode mixer. A one-stage structure of differential G_m-LNA is used. The single side of the G_m-LNA comprises of one MOS transistor and several RLC elements. The current-mode mixer comprises of switched current mirrors. Adjusting the ratio of the drain channel sizes of the switched current mirrors can increase the gain of the mixer and, therefore, increase the gain of RF receiver front-end. The over-power gain of the receiver circuit is mea-

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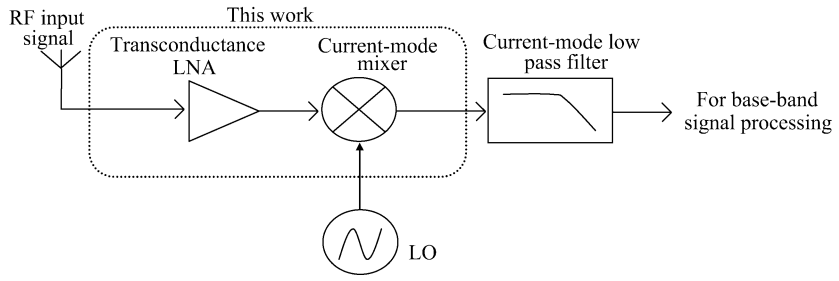

Fig. 1. Whole block diagram of current-mode RF receiver of direct conversion.

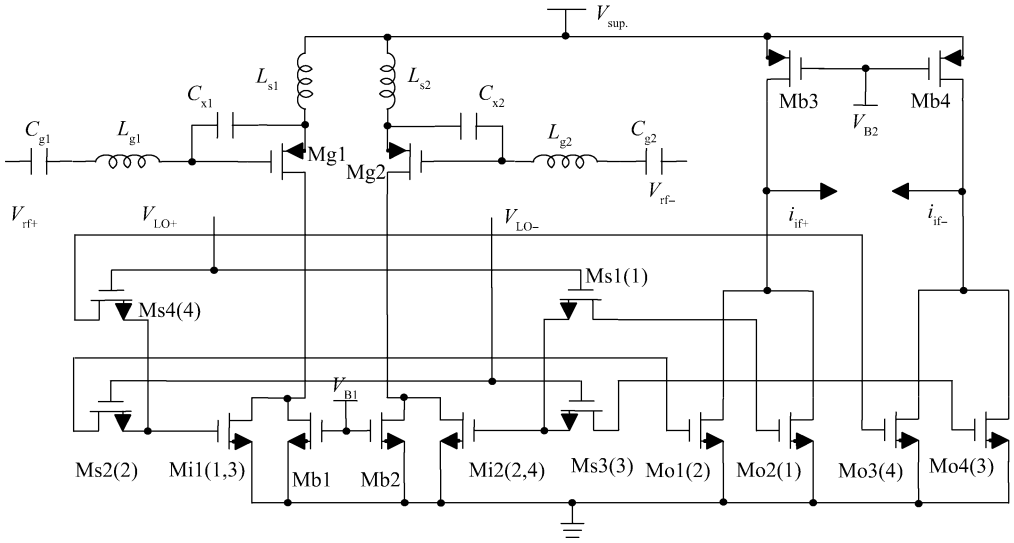

Fig. 2. Proposed low voltage current-mode RF receiver front-end circuit.

sured to be 17.48 dB. The noise is only 4.5 dB. Compared with Ref. [11], this circuit has a higher power gain, a simpler structure and a lower noise figure when using a one stage G_m-LNA and a new switched current mirror mixer; in addition, when compared with Refs. [9, 10], the circuit has a lower supply voltage and higher linearity.

2. Circuit implementation

Figure 1 is a whole block diagram of a direct-conversion current-mode RF receiver. The RF input signals from the antenna enters the transconductance LNA, which amplifies and converts the voltage signal to current signal. The current signals then enter the current-mode mixer and are mixed with signals from a local oscillator (LO). The output current signals from the mixer are processed by a current-mode low-pass filter. Finally, the filtered signals enter the base-band signal processing system. The dashed box contains the transconductance LNA and the current mixer researched in this paper.

The proposed low voltage current-mode RF receiver front-end circuit is shown in Fig. 2. It contains a differential G_m-LNA and a differential current-mode mixer. The differential G_m-LNA is composed of Mg1,2, $L_{g1,2}$, $L_{s1,2}$, $C_{g1,2}$, $C_{x1,2}$. It amplifies and converts the input RF voltage signal to current signal. The other active components form the differential switched current mirror current-mode mixer. The supply voltage V_{sup} is 1 V.

2.1. Differential transconductance low-noise amplifier

Figure 3 shows the proposed differential transconductance low-noise amplifier used in the receiver. It amplifies the input voltage signal and produces differential output current i_{rf+} and i_{rf-} for the current-mode mixer. By using the G_m-LNA, $I-V$ conversion of the LNA output can be eliminated and the current output of the LNA directly connected to the current-mode mixer input. This approach decreases the non-linearity of the receiver caused by several $I-V$ and $V-I$ conversions. The single-side of the G_m-LNA contains just one MOS transistor, two capacitors and two inductors. The gate–source shunt capacitors C_{x1} and C_{x2} can not only reduce the effects of gate–source C_{gs} on resonance frequency and input matching impedance, but can also make the gate inductance $L_{g1,2}$ to be selected at a very small value. Compared with previously reported similar G_m-LNA[10, 11], this circuit has the following advantages: (1) the circuit structure is much simpler due to its one-stage structure; (2) it is not easily affected by gate–source C_{gs} for introducing C_{x1} and C_{x2}; (3) the gate inductance $L_{g1,2}$ to be selected at a very small value.

In Fig. 3, $L_{s1,2}$ and $L_{g1,2}$, together with the capacitance $C_{gs1,2}$ and $C_{x1,2}$, form the impedance-matching network used to produce 50 Ω pure resistance in the resonance frequency. By choosing $C_{x1,2}$ and $L_{s1,2}$ appropriately, 50 Ω pure resistance can be easily achieved. The inductance $L_{g1,2}$ is used to make the input impedance of the LNA resonate, while $C_{x1,2}$ and $L_{s1,2}$ are chosen to make the input impedance of the LNA match

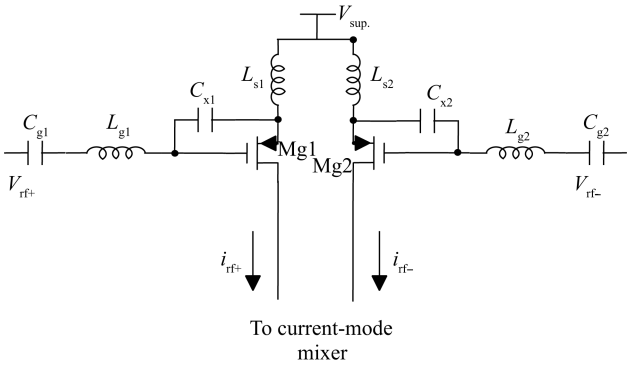

Fig. 3. Schematic diagram of the differential CMOS transconductance LNA.

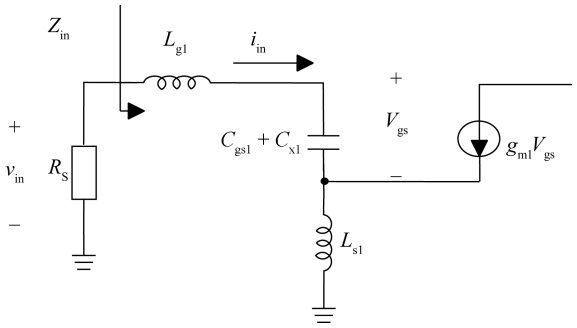

Fig. 4. Small signal equivalent circuit of the transconductance LNA's input port.

the 50 Ω pure resistance. $C_{gs1,2}$ is the intrinsic capacitance whose effect on resonance frequency ω_0 and match impedance Z_{in} can be weakened by introducing $C_{x1,2}$. If the block DC capacitor with a large value is neglected, the high-frequency small-signal equivalent circuit of a single-side transconductance LNA is shown in Fig. 4. Analyzing the circuit of Fig. 4 yields the input impedance of the transconductance LNA as shown in Eq. (1).

$$Z_{in}(s) = \frac{v_{in}}{i_{in}} = \frac{1}{sC'_{gs}} + s(L_{g1} + L_{s1}) + \frac{g_{m1}}{C'_{gs1}}L_{s1}, \quad (1)$$

where $C'_{gs1} = C_{gs1} + C_{x1}$.

At resonance

$$\omega_0 = \frac{1}{\sqrt{C'_{gs1}(L_{g1} + L_{s1})}}, \quad (2)$$

the matched input impedance can be obtained as shown in Eq. (3).

$$Z_{in} = \frac{g_{m1}}{C'_{gs1}}L_{s1}. \quad (3)$$

From $C'_{gs1} = C_{gs1} + C_{x1}$ in Eqs. (2) and (3), it can been seen that if C_{x1} is large enough, the effects of parasitic capacity C_{gs} on resonance frequency ω_0 and matching impedance can be greatly weakened. In addition, from Eq. (2), it is clear that the gate inductance $L_{g1,2}$ can be chosen as a very small value because of $C_{x1,2}$ contribution to ω_0.

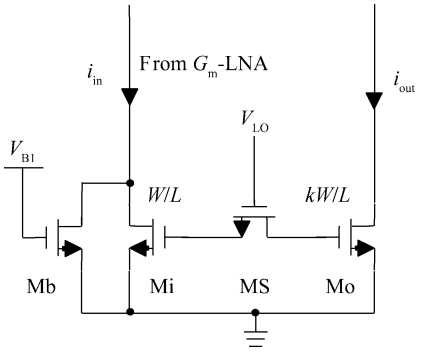

Fig. 5. Proposed switched current mirror—core of the switched current mirror current-mode mixer.

In order to achieve an optimum noise figure, the size of the transistors Mg1, Mg2 of G_m-LNA are set to the optimum value W_{opt}[12] as shown in Eq. (4).

$$W_{opt} = \frac{3}{2}\frac{1}{\omega_0 L_{eff} C_{ox} R_s Q_{sp}}, \quad (4)$$

where ω_0 denotes resonance frequency, L_{eff} is the effective channel length of the fabrication process, C_{ox} is the capacitance per unit area, R_s is source resistance and Q_{sp} denotes the optimum of Q_L for a fixed-power dissipation P_D where $Q_L = \frac{\omega_0(L_{s1}+L_{g1})}{R_s}$.

2.2. Differential current-mode mixer

A conventional CMOS Gilbert cell mixer cannot operate with a 1 V supply voltage due of its three stacked transistors. One direct method used to solve this problem is to reduce the number of stacked connected transistors. Reference [11] proposed a current-mode CMOS mixer which only requires two cascade connected transistors. It eliminates one cascode-connected transistor by using a current input. This approach eliminates an unnecessary V–I conversion in the mixer and therefore reduces overall DC supply voltage. However, its frequency conversion gain is lower and its noise figure is higher.

In this paper, a high gain differential current-mode mixer is proposed, as shown in Fig. 2 except for the G_m-LNA.

In the circuit shown in Fig. 2, the current-mode mixer consists of DC bypass transistors (Mb1, Mb2), switched current mirror input NMOS transistors (Mi1, Mi2), switched transistors (Ms1–Ms4) and switched current mirror output NMOS transistors (M01–M04) and a DC bias current mirror (Mb3, Mb4). The DC bypass transistors (Mb1, Mb2) are used to avoid DC bias currents from the input stage flowing fully into the output stage of the mixer using switched current mirrors.

In Fig. 2, the mixer contains four switched current mirrors which are SM1–SM4. The SM1 consists of Mi1, Ms1, Mo2, the SM2 consists of Mi2, Ms2, Mo1, the SM3 consists of Mi1, Ms3, Mo4 and the SM4 consists of Mi2, Ms4, Mo3. The numbers inside the brackets beside Mi1–Mi2, Ms1–Ms4 and M01–M04 correspond to the number of every switched current mirror. For convenience, one switched current mirror, namely the core of the switched current mirror mixer is drawn in Fig. 5. It contains an input NMOS (Mi), an output NMOS (Mo), a switch transistor (Ms) and a DC bypass transistor (Mb).

In Fig. 5, if $v_{\rm LO} > 0$, Ms is on, current mirrors Mi and Mo can operate, then $i_{\rm out} = Ki_{\rm in}$, where the factor K denotes size ratio of the two MOS transistor channels. If $v_{\rm LO} < 0$, Ms cuts off, then current mirrors Mi and Mo can not operate, $i_{\rm out} = 0$.

According to the above analysis, the following equation can be obtained, as shown in Eq. (5).

$$i_{\rm out} = \begin{cases} ki_{\rm in}, & v_{\rm LO} > 0, \\ 0, & v_{\rm LO} < 0. \end{cases} \tag{5}$$

Equation (6) forms the basic theory of switched current mirrors.

In Fig. 2, RF current signal and local oscillator signal are supposed that

$$\begin{cases} i_{\rm rf+} = -i_{\rm rf-} = I_{\rm rf}\cos(\omega_{\rm rf}t), \\ v_{\rm LO+} = v_{\rm LO-} = v_{\rm LO}\cos(\omega_{\rm LO}t). \end{cases} \tag{6}$$

If $v_{\rm LO+} > 0$ and $v_{\rm LO-} < 0$, the switched current mirrors SM1 and SM4 are on, and SM2 and SM3 are off. According to the principle of Fig. 5, Mo1 and Mo4 are cut off. The output current $i_{\rm if+}$ originates from the current of Mo2, which is equal to $Ki_{\rm rf}$, and the output current $i_{\rm if-}$ originates from Mo3, which is equal to $Ki_{\rm rf+}$.

If $v_{\rm LO-} > 0$ and $v_{\rm LO+} < 0$, the switched current mirrors SM2 and SM3 are on, and SM1 and SM4 are off. According to the principle of Fig. 5, Mo2 and Mo3 are cut off. The output current $i_{\rm if+}$ originates from the current of Mo1, which is equal to $Ki_{\rm rf+}$, and the output current $i_{\rm if-}$ originates from Mo4, which is equal to $Ki_{\rm rf-}$.

From the above analysis, it is clear that in the full period of $v_{\rm LO+}$ and $v_{\rm LO-}$, the following equation can be obtained.

$$i_{\rm if-} = -i_{\rm if+} = \begin{cases} KI_{\rm rf}\cos(\omega_{\rm rf}t), & \cos(\omega_{\rm LO}t) > 0, \\ -Ki_{\rm rf}\cos(\omega_{\rm rf}t), & \cos(\omega_{\rm LO}t) < 0. \end{cases} \tag{7}$$

Equation (6) can be written as

$$i_{\rm if-} = -i_{\rm if+} = Ki_{\rm rf}{\rm sgn}[\cos(\omega_{\rm LO}t)], \tag{8}$$

where ${\rm sgn}(x)$ is a symbol function, which is ${\rm sgn}(x) = 1$ when $x > 0$ and ${\rm sgn}(x) = -1$ when $x < 0$.

In Eq. (7), after expanding the symbol function to Fourier series[13], the following equations can be obtained.

$$\begin{aligned} i_{\rm if-} &= -i_{\rm if+} = Ki_{\rm rf}{\rm sgn}[\cos(\omega_{\rm LO}t)] \\ &= KI_{\rm rf}\cos(\omega_{\rm rf}t) \times \sum_{n=1}^{\infty} \frac{\sin(n\pi/2)}{n\pi/4}\cos(n\omega_{\rm LO}t) \\ &= \underbrace{\frac{2KI_{\rm rf}}{\pi}\cos(\omega_{\rm LO} - \omega_{\rm rf})t}_{\text{down converted signal: IF}} \\ &+ \underbrace{\frac{2KI_{\rm rf}}{\pi}\cos(\omega_{\rm LO} + \omega_{\rm rf})t + \frac{2KI_{\rm rf}}{3\pi}\cos(3\omega_{\rm LO} \pm \omega_{\rm rf})t + \cdots}_{\text{higher order harmonic signal}} \end{aligned} \tag{9}$$

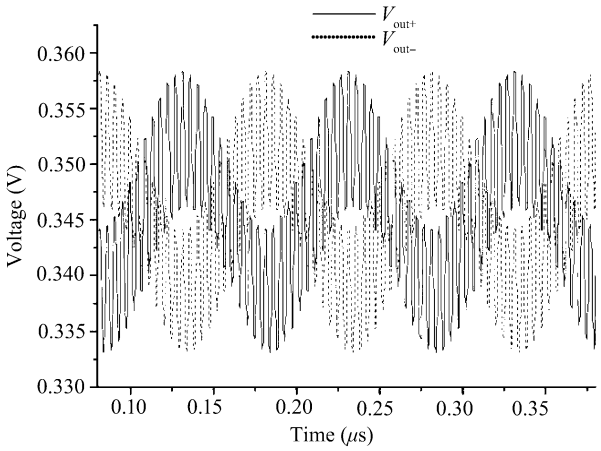

Fig. 6. Post-simulated differential output of the current-mode RF receiver front-end.

From Eq. (9), it can be known that this circuit has a realized down-converted frequency function. Moreover, the conversion gain can be enhanced by adjusting the current mirror factor K. Compared with the mixer of Ref. [11], a larger conversion gain can be obtained in this circuit.

3. Simulation and measurement results

3.1. Simulation results

The performance of the circuit shown in Fig. 2 has been simulated using Spectre in cadence design systems. Transistors are modeled using a standard chartered 0.18 μm RF CMOS process. The layout follows Chartered's Design Rule, YI-093-DR001_Rev1V_1.8V-3.3V. Chartered's Spice Model spec, yi093dr001_1v_00_20090731a is used. Taking into account all of the parasitic elements of the circuit, the post-layout simulation results have satisfied the original design requirements and achieved desired circuit performances under realistic conditions. The simulation results are shown as follows.

3.1.1. Transient simulation in time domain

To verify the mixer function, the transient post-simulation of the current-mode RF receiver front-end in a time domain is made. Its result is shown in Fig. 6 where $V_{\rm out+}$ and $V_{\rm out-}$ denote the positive and negative outputs when the load resistors are equal to 50 Ω. It can be known that Figure 6 contains a down-converted signal (base-band wave) and higher-order harmonic signals which accords with theory, Eq. (9).

3.1.2. Simulations of S parameters

Figure 7 illustrates the simulated results of S parameters S_{11}, S_{22} and S_{21}. S_{11} and S_{22} are equal to –15 dB at 2.4 GHz (RF input of $G_{\rm m}$-LNA) and –24 dB at 10 MHz (output of the current-mode mixer), respectively. From S_{21}, we can know the simulated power conversion gain of the receiver at IF = 10 MHz is about 21 dB.

3.1.3. Post-simulation of noise figure

Figure 8 shows the noise-figure post-layout simulation result of the current-mode RF receiver front-end. It can be known

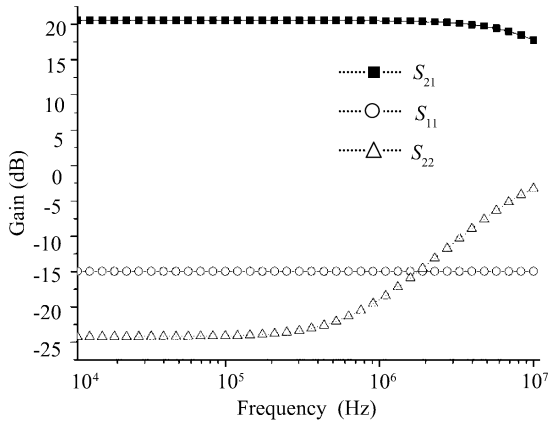

Fig. 7. Post-simulated S parameters of the current-mode RF receiver front-end.

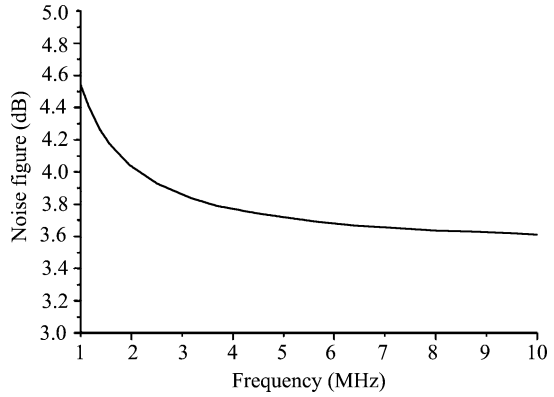

Fig. 8. Post-simulated noise of the current-mode RF receiver fron-end.

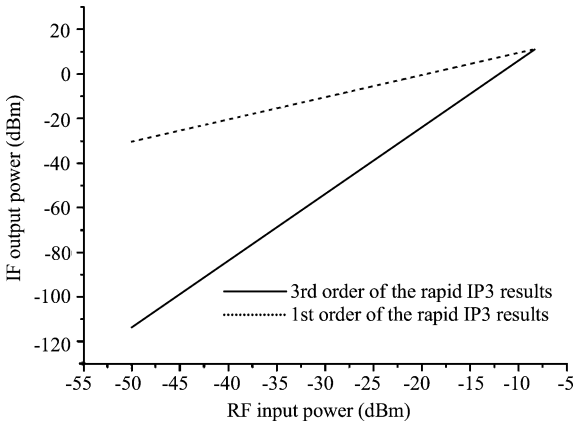

Fig. 9. Post-simulated IIP3 of the current-mode RF receiver front-end.

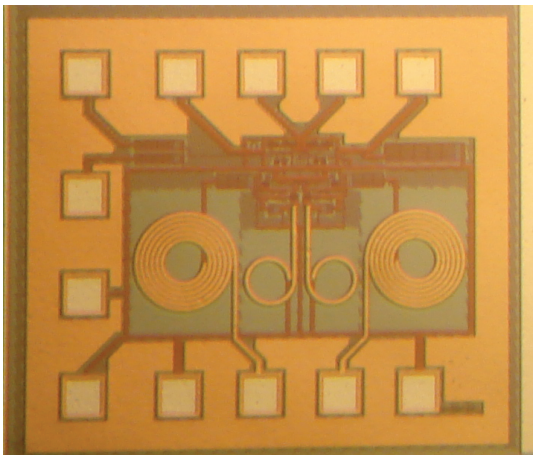

Fig. 10. Microphotograph of the current-mode RF receiver front-end.

that the noise figure at 10 MHz IF is 4.5 dB.

3.1.4. Post-simulation of IIP3

The post-simulation result is shown in Fig. 9. From Fig. 9, it can be known that the post-simulation result of IIP3 is equal to –7.5 dBm. It is much larger than the IIP3 of the circuit in Refs. [9, 10].

3.2. Measurement results

The receiver RFIC has been fabricated using a chartered 0.18 μm CMOS process. A photomicrograph of the current-mode RF receiver front-end chip is shown in Fig. 10. The die size of the test chip including pads is 1200 $\times$ 1200 μm.

In order to verify the current-mode RF receiver front-end, the input (around 2.4 GHz) and output (around 10 MHz) frequency spectrums are measured. In the measurement, the local oscillation frequency is 2.41 GHz. A 3 096 000 sym/s QPSK (quadrature-phase-shift keying) signal with a 2.4 GHz carrier wave and a 4 MHz bandwidth is used as the input signal. Measured input and output frequency spectrums are shown in Fig. 11. From Fig. 11, it is known that the output signal is undistorted and the mixer realized the frequency translation function. In addition, the spectrum intensity of the input signal at 2.4 GHz is –30 dBm, and of an output signal of 10 MHz is –12.52 dBm, so the power gain is 17.48 dB.

Figure 12 shows the measurement result of the third-order input intercept point (IIP_3) by using the two-tone method. In the measurement, the two-tone input RF signals injected into the receiver are at 2.400 GHz and 2.401 GHz. The local oscillation signal frequency is 2.39 GHz. The two fundamental components are down-converted to 10 MHz and 11 MHz respectively. At the same time, the two third order inter modulation products are generated at 9 MHz and 12 MHz respectively.

From Fig. 12, it is easy to calculate that the IIP3 is –7.02 dBm which is basically in agreement with the post-simulation result shown in Fig. 9.

Table 1 outlines the performance of this design and previously published RF receiver front-ends. From this table, it can be seen that compared to previously published voltage mode RF receiver front-ends, the current-mode RF receiver front-end in this paper works at a lower voltage supply. Compared to other published current-mode RF receiver front-ends, this current-mode RF receiver front-end can work with a larger gain and a lower noise figure. Moreover, the die size is small.

4. Conclusions

This paper describes the design of a low voltage current-mode RF front-end with high power gain. The receiver has been simulated and fabricated using standard chartered

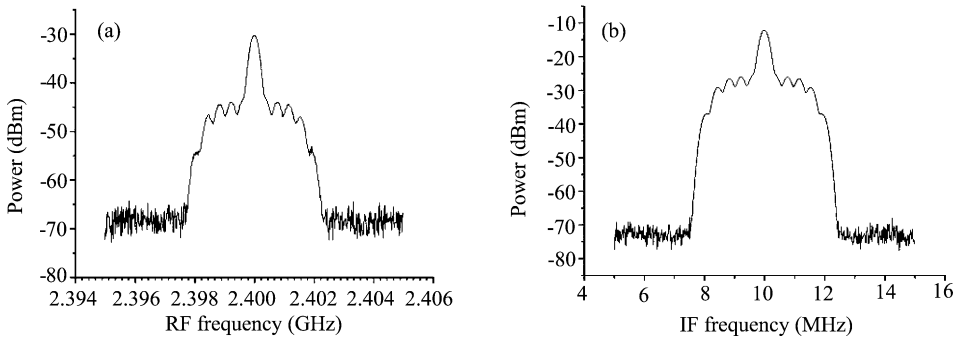

Fig. 11. Measured spectra of the (a) input and (b) output frequency.

Table 1. Performance summaries and comparisons of every RF receiver fron-ends.

Parameter	This work	Ref. [9]	Ref. [8]	Ref. [11]	Ref. [10]
Technology	0.18 μm CMOS	0.35 μm CMOS	0.09 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Supply voltage (V)	1	2.7	1.2	1	1.5
Gain (dB)	17.48	23	12.1	11.4	15.7
IIP3 (dBm)	–7.02	–1.5	–2.8	6.1	–20.56
OIP3 (dBm)	10.46	21.5	9.3	17.5	–4.86
NF (dB)	3.9	3.4	5.4	5.87	4.8
Die size (mm^2)	1.2×1.2	–	0.88	1.3×2.1	–
Power (mW)	14	21.6	9.8	40.9	17.2
Mode	Current mode	Voltage mode	Current mode	Current mode	Current mode

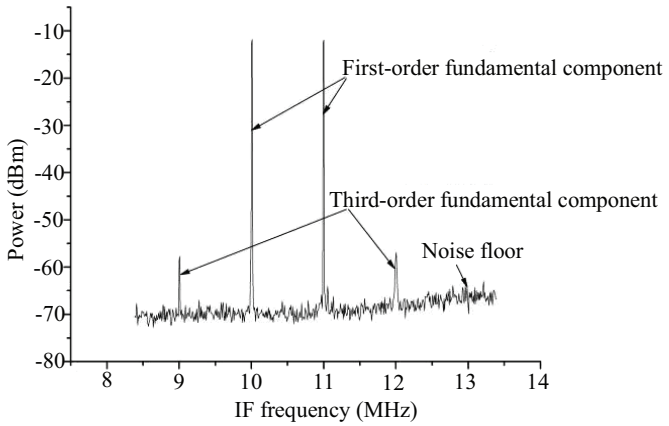

Fig. 12. Measured spectrum for calculating the IIP3 of the current-mode RF receiver front-end.

0.18 μm CMOS technology. The supply voltage is 1 V. The total measured power gain of the receiver is equal to 17.48 dB and the measured input-referred third-order intercept point (IIP3) is equal to –7.02 dBm. The total noise figure is equal to 4.5 dB. All these satisfy the requirements of the RF circuit very well. The power consumption of the circuit is 14 mW with a 1 V supply voltage, meeting the current demand for low supply voltage and low power consumption.

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