A fully integrated direct-conversion digital satellite tuner in 0.18 μm CMOS*

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Abstract: A fully integrated direct-conversion digital satellite tuner for DVB-S/S2 and ABS-S applications is presented. A broadband noise-canceling Balun-LNA and passive quadrature mixers provided a high-linearity low noise RF front-end, while the synthesizer integrated the loop filter to reduce the solution cost and system debug time. Fabricated in 0.18 μm CMOS, the chip achieves a less than 7.6 dB noise figure over a 900–2150 MHz L-band, while the measured sensitivity for 4.42 MS/s QPSK-3/4 mode is –91 dBm at the PCB connector. The fully integrated integer-N synthesizer operating from 2150 to 4350 MHz achieves less than 1 ℃ integrated phase error. The chip consumes about 145 mA at a 3.3 V supply with internal integrated LDOs.

Key words: direct-conversion; CMOS RF; tuner; noise-canceling LNA; passive mixer
DOI: 10.1088/1674-4926/32/4/045004 **EEACC:** 1205; 1250; 2570D

1. Introduction

Although mobile TV systems, such as DVB-T/H and CMMB, are hot topics nowadays, digital satellite TV systems are still in great demand, especially after China's self-dominated digital satellite standard, advance broadcasting system-satellite (ABS-S), started operation.

Over the last decade, digital satellite TV receivers have moved from early high-IF dual-conversion architecture[1, 2] to direct-conversion implementation[3, 4]. The high-IF dual-conversion architecture suffers from a high level of complexity (two mixing stages in the RF front-end), high power dissipation due to the extra circuitry operating at a relatively high IF frequency, and the requirement for an off-chip SAW filter to improve the noise and image rejection performance. A direct-conversion tuner in which the RF signal is down-converted in a single step to the baseband does not suffer from image rejection issues since the signal is its own image. Furthermore, it simplifies the tuner architecture considerably by eliminating the off-chip SAW filter, the second IF mixer and the high-IF gain stages. This reduces both the die area and the power dissipation. As such, direct-conversion tuner architecture has also achieved a tremendous reduction in external component count and cost.

This paper presents the implementation of a direct-conversion digital satellite radio tuner using 0.18 μm CMOS technology, supporting the DVB-S/S2 and ABS-S standards. The system requirements are stated, and an overview of the selected architecture is given. The detailed circuit implementation, including the RF front-end, the analog baseband and the integer-N PLL synthesizer, is described.

2. System specification and tuner architecture

Unlike other digital TV broadcasting systems, such as DVB-T/H, the DVB-S/S2 requirements were not well defined. However, several important RF specifications for digital satellite TV tuners are well known, such as sensitivity, CNR threshold at a given RF input power (–60 dBm) and selectivity. Sensitivity is defined as the minimum input modulated signal power with 5.5 dB CNR that can be demodulated with a predefined BER, which is a little different from some other RF receivers where sensitivity is defined without a CNR limit. The CNR threshold is limited by the obtained SNR at –60 dBm input, which is usually determined by phase noise, NF, linearity, image rejection, group delay variation, etc.

The tuner adopts the direct-conversion architecture to fulfill small physical size and low power consumption. The block diagram of the tuner is shown in Fig. 1. The signal received from the LNB is amplified, down-converted and filtered into the baseband, and finally produces I/Q balanced output for further signal processing at the baseband demodulator.

The single-ended input differential-output low-noise amplifier (LNA), or Balun-LNA, facilitates the connection to the F-connector and to the following fully differential mixer. It eliminates the need for an off-chip balun in front of the LNA for a low noise figure and low external BOM. Also, it needs no on-chip balun after the LNA, effective for low distortion as well as low power consumption. In this design, analog continuously controlled variable gain function is included in both the front-end and the analog baseband. The AGC control distribution block, as shown in Fig. 1, is responsible for producing a group of gain control voltages for each gain block. And the RF specifications, such as NF and linearity, can be balanced by programming an AGC sequence through the AGC control distribution block. This AGC algorithm provides flexibility to obtain the best SNIR over the whole range.

3. Circuit implementation

3.1. RF front-end

The RF front-end consists of a broadband LNA and I/Q mixers. Figure 2 shows the simplified schematic.

* Project supported by the National High Technology Research and Development Program of China (No. 2007AA01Z280).
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Received 7 September 2010, revised manuscript received 30 November 2010

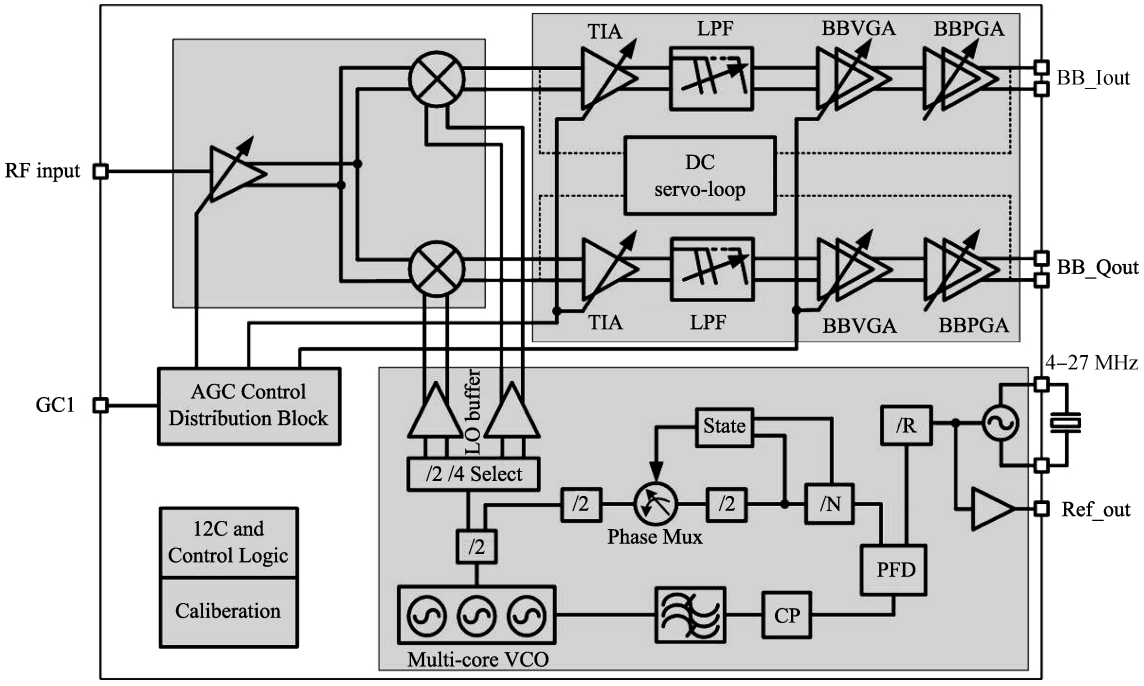

Fig. 1. Block diagram of the designed RF tuner.

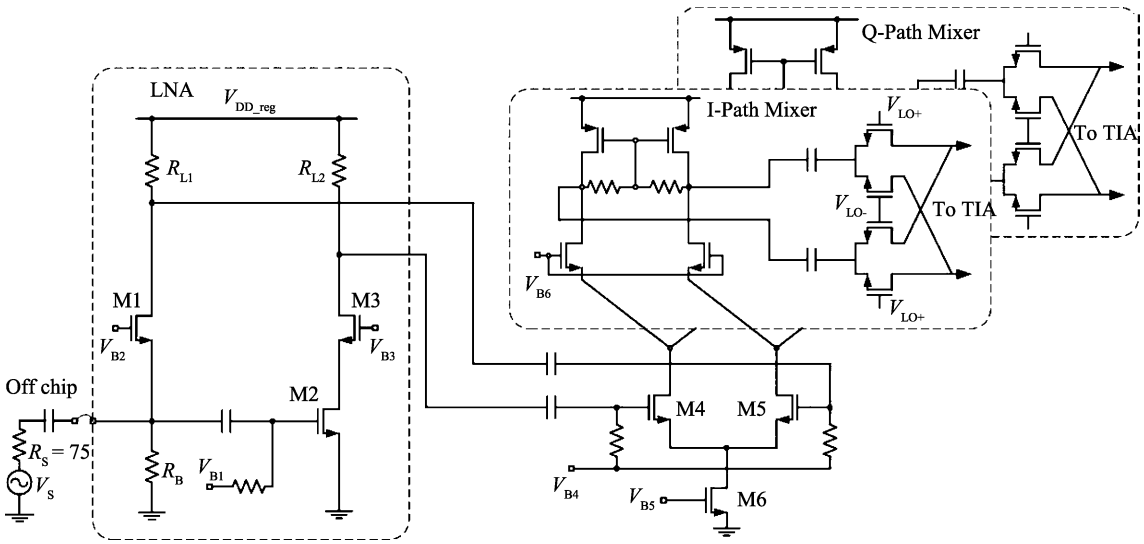

Fig. 2. Simplified schematic of the RF front-end.

Recently, the Balun-LNA has been demonstrated successfully by using the hybrid common-gate and common-source amplifier topology[5−7], which exhibits not only broadband single-to-differential conversion but also noise and nonlinear cancellation. The input impedance is dominated by the CG amplifier M1. If $1/g_{m1} = R_s = 75\,\Omega$, broadband impedance matching is achieved. A balanced voltage output is obtained if $g_{m1}R_{L1} = g_{m2}R_{L2}$. As a result, the differential output voltage gain is $2R_{L1}/R_s$. As for noise performance, the noise from M1 appears as the common-mode signals at the differential outputs in a balanced condition. So does drain current nonlinearity from M1. In order to maximize the noise cancellation capability with given current, the g_{m1} of the CG amplifier M1 is chosen a little smaller than $1/R_s$ with small v_{dsat}, while g_{m2} is larger than g_{m1} with a large v_{dsat}, to achieve better noise/nonlinear cancellation and to keep the current consumption under control at the same time. The voltage controlled variable gain function can be easily introduced into the LNA by using current-wasting method, more than 20 dB gain range can be easily provided as long as the minimum DC current in the load resistor is large enough to sustain signal current. The same gain control scheme can be utilized in the following mixer transconductor stage. The designed LNA exhibits a noise figure of 3.5 dB, a nominal gain of 21 dB, and IIP3 of 1.5 dBm while drawing about 6.5 mA.

Instead of using a Gilbert mixer, a current-mode passive mixer is utilized to achieve high linearity and low flicker noise, as shown in Fig. 2. The quadrature mixer is composed of a

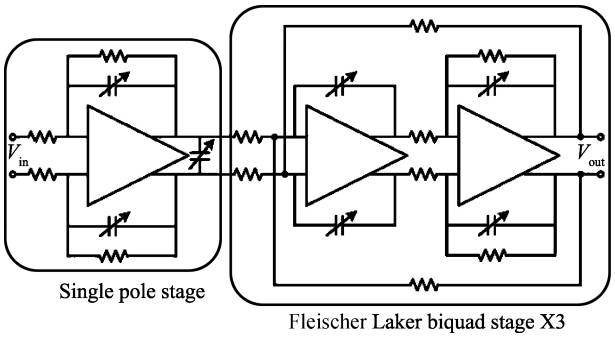

Fig. 3. Architecture of seventh-order Butterworth low-pass filter.

transconductance amplifier with two separate sets of output, I/Q mixing quads and TIAs, which are not shown in Fig. 2. Such a topology can provide isolation between the I/Q path while introducing less mismatches in contrast to two independent transconductance amplifiers. Some linearity improvement schemes can be utilized for the transconductor, such as source degeneration and nonlinear cancellation.

3.2. Analog baseband

The analog baseband blocks include channel selection LPFs and variable/programmable amplifiers for both in-phase and quadrature-phase signal processing.

The channel filter is a seventh-order Butterworth type implemented by OpAmp-RC topology, as shown in Fig. 3, and the cutoff frequency is tunable from 4 to 25 MHz.

Two VGA stages following the channel filter provide more than 40 dB gain range, and its gain control voltage is provided by the AGC control distribution block in Fig. 1. Then the following two PGA stages provide some extra gain range. The PGA gain is directly programmed by digital code through an I2C control bus, which is used to shift the signal chain gain curve over the whole range to realize optimal performance.

DC-offset cancellation is indispensable in a direct-conversion receiver because DC offset may saturate the baseband output and degrade the dynamic range. In this design, a single-loop continuous DC servo-loop is utilized with off-chip loop capacitors. The high-pass cutoff frequency is set almost constant at 1 kHz for all gain settings by keeping the gain of the feedback loop inversely proportional to that of the signal chain.

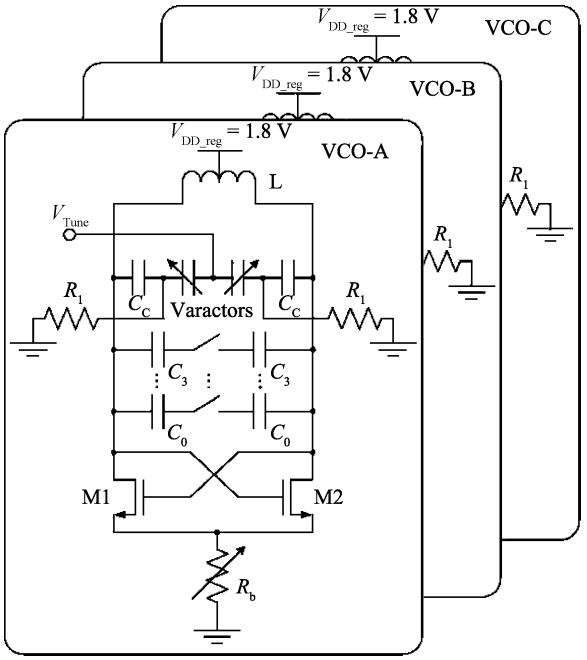

Fig. 4. Schematic of the multi-core VCO.

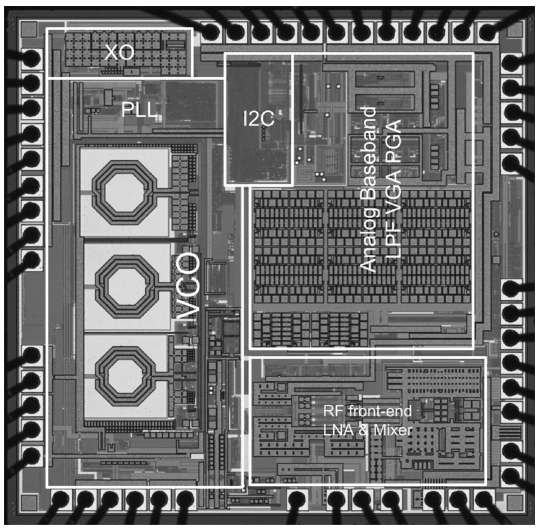

Fig. 5. Die photograph.

3.3. Frequency synthesizer

An integer-N PLL synthesizer with an on-chip loop filter is employed in the tuner, and its block diagram is given in Fig. 1. The PLL provides in-phase and quadrature-phase LO signals through divider-by-2/4 to cover the whole L-band frequency range.

The 3-core VCO covers a frequency range from 2150 to 4350 MHz using NMOS cross-coupled pairs with a resistor current source and a MOS varactor for tuning, as shown in Fig. 4. A NMOS only cross-coupled differential pair has higher g_m under the same bias current and is easier for oscillation to start even when the tank parallel resistance R_p is low. Also, NMOS only VCO has smaller capacitance from active devices and is good for high frequency digital tuning. However, NMOS only VCO generally has a worse $1/f^3$ corner than NMOS-PMOS VCO or PMOS only VCO. In this design, a resistor current source instead of a NMOS current source is used for better noise performance. Furthermore, the resistor value can be digitally controlled to set the optimum bias current in the VCO. Also, as shown in Fig. 4, binary weighted MIM capacitors digitally coarse-tune the VCO. The VCO supply is regulated through a simple on-chip regulator to isolate supply noise and to achieve lower supply pushing.

An 8/9 dual mode phase-multiplexer-based prescaler is used in the PLL, and a QLO divider is a part of the prescaler, as shown in Fig. 1.

Table 1. Measurement performance summary, typical conditions.

Parameter	Measured
Input return loss (dB)	–12 to –9
NF @ Max gain (dB)	5.8–7.6
Gain MAX (dB)	79
RF range/BB range (dB)	42/36
Baseband low-pass filter cutoff frequency range (MHz)	4–45
IIP2 @ Max gain/(Max RF-20 dB) (dBm)	0/16
IIP3 @ Max gain/(Max RF-20 dB) (dBm)	–25/–3
PLL tuning range (GHz)	0.9–2.15
Integrated phase error (1 kHz–10 MHz)	$< 1.3°$
Sensitivity [a] (dBm)	–91
Maximum input (dBm)	10
Current consumption (mA)	145

[a] QPSK-3/4 4.42 MS/s.

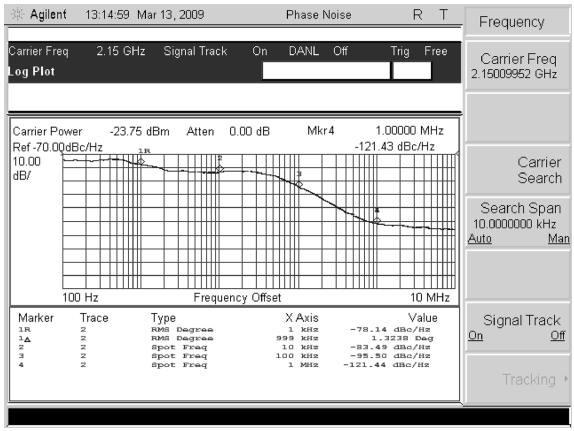

Fig. 6. Phase noise profile measured at QLO output, f_{lo} = 2.15 GHz.

4. Measurement results

The tuner chip was fabricated in a 0.18 μm CMOS process. A micrograph of the die is shown in Fig. 5. The measured AC performance referred to the SMA connector input from a single 3.3 V supply is summarized in Table 1.

The measured NF ranges are from 5.8 to 7.6 dB over the whole L-band, which includes PCB and line losses. The gain tilting from 0.9 to 2.2 GHz is less than 3 dB.

The measured phase noise spectrum of the QLO output is shown in Fig. 6. An integrated phase error from 1 kHz to 10 MHz is 1.3° at the maximum LO frequency, and is better than this value over the whole L-band.

Figure 7 gives a measured IQ transient output with a sine-wave single tone input at the RF port. The RF input is –60 dBm at 1.6 GHz, and the LO is 1.601 GHz. From the large signal transient waves, amplitude and phase mismatches between I and Q paths cannot be recognized easily, while in Monte Carlo simulation the amplitude and phase mismatches are less than 0.2 dB and 0.6° separately and the DC offset is within 100 mV.

Table 2 summarizes a performance comparison with other DVB-S tuners. The presented tuner achieves a low noise figure and low I/Q matching while having the smallest chip area.

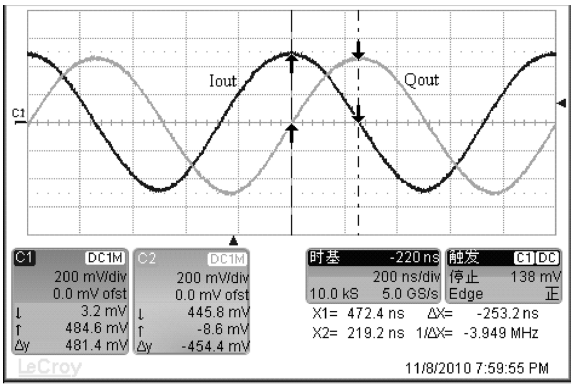

Fig. 7. I/Q output, f_{input} = 1.601 GHz, f_{lo} = 1.6 GHz.

Table 2. DVB-S tuners'performance comparison.

Parameter	Ref. [4]	Ref. [8]	This work
Technology	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS
Architecture	Zero-IF	Low-IF	Zero-IF
Noise figure (dB)	10.5	10	7.6
IIP3 @ G_{min} (dBm)	9	25	26
I/Q matching (dB/°)	0.38/1	1/0.8	0.2/0.6
Power dissipation (mA)	100	160	145
Supply voltage (V)	1.8/3.3	1.8/3.3	3.3
Die area (mm^2)	Tuner-only 7	8.6	4.1

5. Conclusion

A highly integrated RF tuner for DVB-S/S2 and ABS-S applications in 0.18 μm CMOS technology is demonstrated. Implemented in direct-conversion architecture, the tuner consumes 145 mA. Together with system and circuit design techniques, the tuner can be successfully utilized in digital satellite broadcasting systems. Currently, the designed tuner is now in engineering sampling status and considered seriously to be in mass production.

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