A dual mode charge pump with adaptive output used in a class G audio power amplifier*

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Abstract: A dual mode charge pump to produce an adaptive power supply for a class G audio power amplifier is presented. According to the amplitude of the input signals, the charge pump has two level output voltage rails available to save power. It operates both in current mode at high output load and in pulse frequency modulation (PFM) at light load to reduce the power dissipation. Also, dynamic adjustment of the power stage transistor size based on load current at the PFM mode is introduced to reduce the output voltage ripple and prevent the switching frequency from audio range. The prototype is implemented in 0.18 μm 3.3 V CMOS technology. Experimental results show that the maximum power efficiency of the charge pump is 79.5% @ 0.5x mode and 83.6% @ 1x mode. The output voltage ripple is less than 15 mV while providing 120 mA of the load current at PFM control and less than 18 mV while providing 300 mA of the load current at current mode control. An analytical model for ripple voltage and efficiency calculation of the proposed PFM control demonstrates reasonable agreement with measured results.

Key words: class G audio amplifier; charge pump; output voltage ripple; PFM; segmented power stage
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1. Introduction

Modern portable electronics incorporate hands-free operation, MP3 music playback and DMB reception, leading to a demand for highly integrated and power efficient audio amplification. Class D audio power amplifiers have overwhelming advantages over other kinds of audio amplifiers at the cost of slightly reduced performance and a level of switching noise, which might, in some cases, interfere with RF functions, such as mobile phone, GPS or FM radio reception[1]. Traditional class-AB amplifiers, which are still largely used, are not suited to meet high efficiency demand. The efficiency of a class-AB audio amplifier can theoretically be about 78.5% for a rail-to-rail sine wave, but for real-life music and speech signals, it is much lower: 15%–20%[2].

During the last few years, class G amplification[3−5] was developed in portable audio applications to reduce the power dissipation while keeping the advantages of class AB amplifiers, such as good linearity, low cost and free of EMI. Class G amplifiers work off the fact that music and voice signals have a high peak to mean ratio with most of the signal content at low levels. They use multiple voltage rails and switches to the appropriate voltage rail as required by the instantaneous output voltage level. In this way, they can reduce the voltage drop at output power transistors to improve the power efficiency.

It is preferred to design a class G audio amplifier using a charge pump to generate the supply rails. The charge pump uses only a few small, low cost capacitors to provide the voltage conversion. It eliminates the cost, size and radiated EMI related to inductor based converters, or the power loss of linear regulators. Since the charge pump has discrete conversion gains, the average efficiency may be too low when outputting a continuous voltage of a wide range. The optimal strategy is to output a few discrete supply rails. In this paper, the system analysis of the proposed charge pump is introduced, and a function description and some simulation results are presented.

2. System analysis of the proposed charge pump

The simplified diagram of the class G audio power amplifier is shown in Fig. 1. It is a linear audio amplifier with an embedded discrete adaptive power supply. The dashed block is the output stage of a class AB amplifier. The charge pump is to generate the adaptive supply rails of the class AB output stage. The output voltage of the charge pump changes adaptively according to the amplitude of the input signal. When inputting a low level signal, the charge pump is controlled to output a low voltage rail. Otherwise, a high voltage rail outputs to power the output stage. There are two main requirements for a charge pump in a class G audio amplifier application. Firstly, the charge pump should have a relatively high efficiency at all load conditions. Secondly, the output voltage ripple should be small, especially at light loads, when the output voltage of the audio amplifier has a small amplitude.

The average efficiency of this kind of linear amplifier with discrete supply voltages depends upon both the supply voltage transition point and the amplitude distribution of the input signal[6]. A 0.5x/1x dual mode charge pump is preferably used

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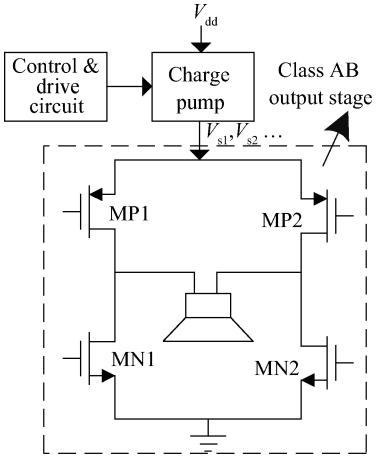


Fig. 1. Topology of class G amplification using a charge pump.

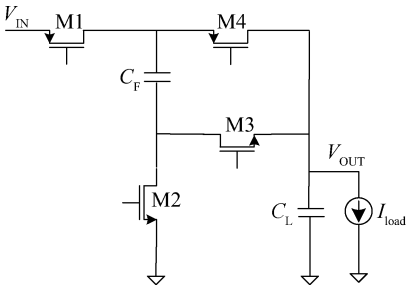


Fig. 2. Power stage of the charge pump with 0.5x/1x modes.

Table 1. Switch sequence of the charge pump.

Conversion ratio	Charging phase	Discharging phase
0.5x	M1, M3	M2, M4
1x	M1 switching, M4 always on, M2, M3 always off	M1 switching, M4 always on, M2, M3 always off

to implement the supply of a class G amplifier from the design complexity and available efficiency viewpoint. The power stage of the charge pump is shown in Fig. 2. It can easily be implemented using a charge pump with two external capacitors and four switches. M1 and M4 are P-channel transistors. M2 and M3 are N-channel transistors. C_F is the flying capacitor and C_L is the output capacitor.

It can operate in two modes: 0.5x and 1x mode. In our design, two power supply levels of 1.4 V and 2.8 V can output from the charge pump. The switch sequence is shown in Table 1.

2.1. Efficiency consideration

The dissipation in the charge pump can be divided into four kinds of loss: switching loss, dynamic loss, conduct loss and control loss. Switching loss is the power dissipation that drives the power transistors on and off. The switching loss is given as

$$P_{sw} = f_s(C_{gate,N}V_{gs,N}^2 + C_{gate,P}V_{sg,P}^2), \quad (1)$$

where $C_{gate,N} \propto (W \cdot L)_N$ and $C_{gate,P} \propto (W \cdot L)_P$ are the PMOS and NMOS lumped capacitance associated with charging and discharging the MOSFET gates, including the relevant transistors within the gate drivers.

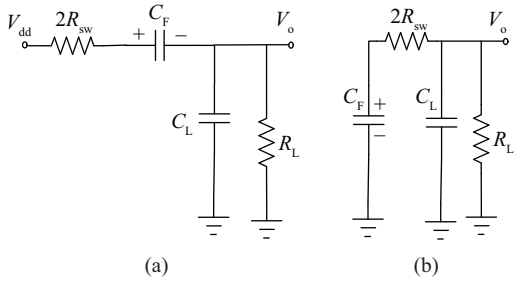


Fig. 3. (a) Charging phase. (b) Discharging phase.

And the conduction loss is about a constant value when V_{in}, V_{out} and P_{out} are set. It can be described as

$$P_{cond} = P_{out}\left(\frac{kV_{in}}{V_{out}} - 1\right), \quad (2)$$

where K is the gain of the charge pump. The dynamic loss is introduced by the switching of the parasitic capacitances of the power stage of the charge pump. It can be described as

$$P_{dyn} = f_s \sum C_{par,i}V_{dd}^2. \quad (3)$$

The control loss is the power loss dissipated in the control circuit of the charge pump. Unlike the inductive SMPS, the conduction loss in our charge pump cannot be optimized since the output and input are preset. Then only the switching loss, dynamic loss and control loss can be optimized. The switching loss and dynamic loss are independent of load current and related to the switching frequency and gate capacitances or node capacitances.

The audio signals have a Gaussian-like amplitude distribution and a large PAR (peak to average power ratio) value in most types, which means that most audio signals are concentrated in the low level range[2]. Take an audio signal with maximum amplitude of 2.4 V and PAR of 15 dB, for example: 98.1% of the signal amplitude is lower than 1 V. For our design, it is significant to improve the efficiency of the charge pump when operating at 0.5x mode with a supply voltage of 1.4 V.

2.2. Power efficiency and output voltage ripple comparison

In this section, the power efficiency and output voltage ripple of a 0.5x mode charge pump are calculated at different control strategies. Nowadays, pulse frequency modulation (PFM)[7] and current mode (CM)[8, 9] control are usually used to regulate the charge pump. Pulse width modulation (PWM) is rarely used in charge pump operation since the regulation is difficult at a light load because of the exponential nature of the current charging the capacitors[10]. The simplified description of the work states in different phases is shown in Fig. 3.

The derivation process is similar to the ripple and quiescent current derivation of the voltage doubler in Ref. [11]. The specific derivation is shown in Appendix A. The output voltage can be written as shown in Eq. (A9).

$$V_{OUT} = \frac{1}{2}V_{IN} - \frac{1}{2}I_{load}\left(1 + \frac{t_w}{T}\right)\sum_{i=1}^{4} R_{Mi}. \quad (4)$$

The on-resistance of power MOS R_{Mi} is regulated in CM control to stabilize the output while the skipping time t_w is regulated in PFM control. Now the output ripple and efficiency will be compared between the two control strategies: CM control and PFM control.

In CM control, there is no skipping phase except the small dead time interval, and the transfer current is equal to the load current. Then there is no current flow into or out of the output capacitor C_L. The charge pump with current control has no ripple ideally. Actually it has a small ripple due to the parasitic resistance of the output capacitor and other non-ideal effects. The power efficiency of current control is given as

$$\eta = \frac{P_{load}}{P_{total}} = \frac{I_{load}V_{OUT}}{V_{IN}(I_{IN}+I_Q)} = \frac{I_{load}V_{OUT}}{V_{IN}(I_{load}/2+I_Q)}, \quad (5)$$

$$I_Q = I_{QB} + I_{QS} = I_{QB} + f_s V_{IN}\sum_{i=1}^{4} C_{Mi}, \quad (6)$$

where I_Q is the quiescent current of the charge pump, which contains two parts: the control current I_{QB} dissipated in the control block and the switching drive current. C_{Mi} is the gate capacitance of the power MOS in the power stage of the charge pump.

In PFM control, the output capacitor is charged by the current difference between the transfer current I_p and the load current I_{load} in phases A and B, as shown in Fig. A1. Then the output ripple can be written as

$$V_{ripple} = \frac{(I_P - I_{load})\,T}{C_L} = \frac{I_{load}t_w}{C_L}. \quad (7)$$

From Eqs. (4) and (7), we can get

$$V_{ripple} = \frac{I_{load}t_w}{C_L} = \frac{\dfrac{V_{IN}-2V_{OUT}}{\sum_{i=1}^{4} R_{Mi}} - I_{load}}{f_s C_L}. \quad (8)$$

The power efficiency of PFM control is given as

$$\eta = \frac{P_{load}}{P_{total}} = \frac{I_{load}V_{OUT}}{V_{IN}(I_{IN}+I_Q)} = \frac{I_{load}V_{OUT}}{V_{IN}(I_{load}/2+I_Q)}, \quad (9)$$

$$I_Q = I_{QB} + I_{QS} = I_{QB} + \frac{1}{T+t_w}V_{IN}\sum_{i=1}^{4} C_{Mi}. \quad (10)$$

From the aforementioned analysis, the charge pump with PFM control has a larger ripple than that with CM control due to the skipping phase t_w. The ripple gets much larger when the load gets lighter. At a certain load condition, the efficiency is mainly affected by the quiescent current of the charge pump. The quiescent current of PFM control is smaller than that of CM control also due to the skipping phase t_w, which has a lower switching loss. From the power efficiency viewpoint, it is preferable to implement PFM control at 0.5x mode operation to reduce the power dissipation. Figure 4 depicts the calculated efficiency and ripple versus the load current for both modes of operation, CM and PFM control. There must be a tradeoff between the efficiency and the output ripple of PFM control. Conventional PFM control has a higher efficiency, especially at a light load but also the larger output voltage ripple, which is unfavorable in audio applications.

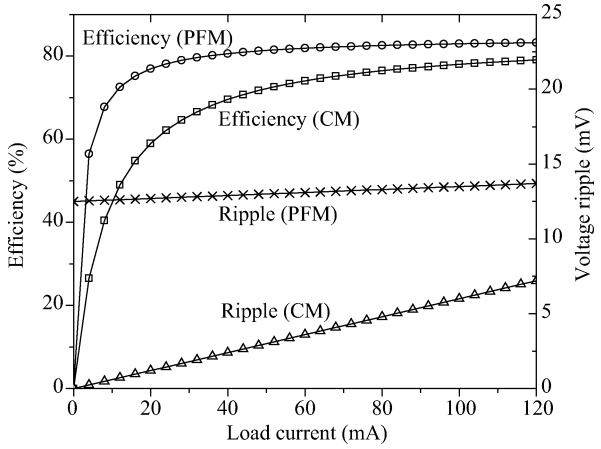


Fig. 4. Efficiency and ripple comparison between CM and PFM.

2.3. Proposed PFM control with segmented power stage

From Eq. (8), if $\sum_{i=1}^{4} R_{Mi}$ increases according to the load current, then the voltage ripple can become smaller. This is the case in our proposed PFM control with segmented power stage. The ripple and efficiency comparison will be derived between normal PFM without segment and the proposed control strategy.

Assuming the same load condition, PFM control with segmented power stage has a power MOS size $1/N$ times as large as traditional PFM control. The on-resistance $\sum_{i=1}^{4} \overline{R}_{Mi}$ of the proposed control is N times as large as that in traditional PFM control and gate capacitance $\sum_{i=1}^{4} \overline{C}_{Mi}$ of the proposed control is $1/N$ times as large as that in traditional PFM control. Then the output ripple and output voltage of the proposed control are modified as follows,

$$V'_{ripple} = \frac{I_{load}t_w}{C_L} = \frac{\dfrac{V_{IN}-2V_{OUT}}{N\sum_{i=1}^{4} R_{Mi}} - I_{load}}{f_s C_L}, \quad (11)$$

$$V'_{OUT} = \frac{1}{2}V_{IN} - \frac{1}{2}I_{load}\left(1+\frac{t_w}{T}\right)N\sum_{i=1}^{4} R_{Mi}. \quad (12)$$

The steady period can be calculated as

$$(t_w+T)' = \frac{V_{IN}-2V_{OUT}}{I_{load}N\sum_{i=1}^{4} R_{Mi}}T. \quad (13)$$

If Eq. (13) is combined with Eq. (10), the quiescent current of the proposed control can be expressed as

$$I'_Q = I_{QB} + \frac{1}{(T+t_w)'}V_{IN}\frac{1}{N}\sum_{i=1}^{4} C_{Mi}$$
$$= I_{QB} + f_s\frac{V_{IN}I_{load}}{V_{IN}-2V_{OUT}}\sum_{i=1}^{4} R_{Mi}\sum_{i=1}^{4} C_{Mi}. \quad (14)$$

From Eq. (14), it can be seen that the quiescent current of PFM control with segmented power stage is the same as traditional PFM control. But the ripple is much smaller, which is

Table 2. Size of the power transistors at the different modes and different load current conditions.

	0.5x mode I_{load} < 15 mA	0.5x mode (15–30 mA)	0.5x mode (30–60 mA)	0.5x mode (60–125 mA)	1x mode
M1	2.2 m/0.3 μm	4.4 m/0.3 μm	8.8 m/0.3 μm	17.6 m/0.3 μm	17.6 m/0.3 μm
M2	0.75 m/0.35μm	1.5 m/0.35 μm	3 m/0.35 μm	6 m/0.35 μm	NA
M3	1. 5 m/0.35 μm	3 m/0.35 μm	6 m/0.35 μm	12 m/0.35 μm	NA
M4	2 m/0.3 μm	4 m/0.3 μm	8 m/0.3 μm	16 m/0.3 μm	16 m/0.3 μm

Note: NA indicates that the power transistor does not operate in the mode.

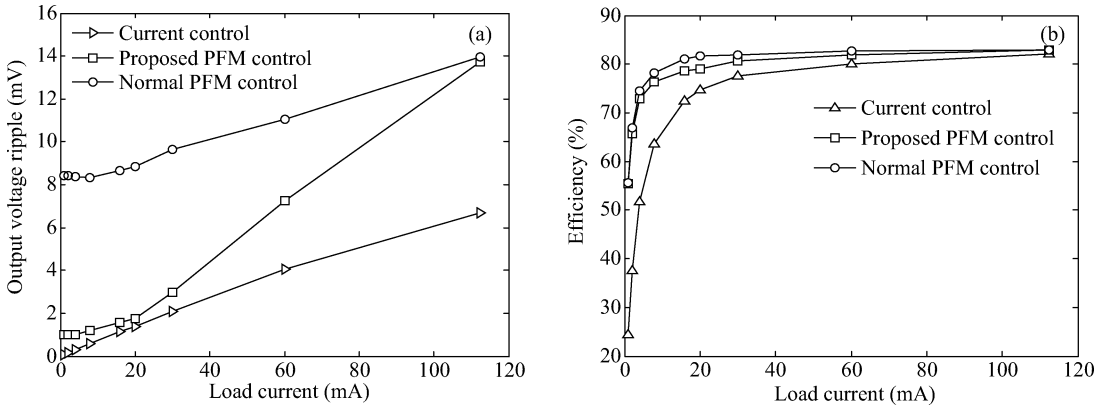


Fig. 5. (a) Ripple comparison among three control strategies. (b) Efficiency comparison.

related to the scaling factor N. It should be noted that the factor should be as large as possible. Actually the charge pump should supply enough current when segmenting the size of the power MOS. So the optimized condition is when the charge pump can just supply the load current at the corresponding size of the power transistors.

The choices of whole power transistor aspects are based on the current handling capacity. The optimized sizes of all power transistors are given in Table 2. The PFM control is used to regulate the output at 0.5x mode and the power transistors are segmented into 4 more parts according to the load current, besides the last segment according to the different operation modes. CM control is used to regulate the output at 1x mode to reduce the output voltage ripple. The optimization goal is to achieve the minimum chip area when meeting the load current capability in different operation modes. The specific optimized process is implemented in MATLAB.

The efficiency and output voltage ripple of three control strategies are simulated in Spectre. The comparison results among the three control strategies are shown in Fig. 5. At the light load current range, the output voltage ripple of the proposed PFM control is much smaller than that of normal PFM control but has almost the same efficiency as normal PFM control. The little difference between the two control methods is due to the slightly larger control current of the proposed PFM control. Current control has the smallest ripple but also the worst efficiency at the load range of 0.5x mode. Figure 5 shows that the simulated results are consistent with the theoretical analysis.

In our class G application, the charge pump is used to supply a class AB amplifier with a speaker load. The impedance of the audio speakers varies greatly among different manufacturers due to the electromechanical nature of the system. But for the common moving coil speaker, it is found that even a crude resistive approximation of load impedance can lead to a reasonably accurate prediction of the charge pump load current. Measured impedances of two common 8 Ω speakers (GC0251K and GC0351K) are given in Ref. [12]. It can be found that, in both cases, the magnitude of the impedance remains well within 13% of the nominal 8 Ω over the specified frequency operating range, giving fairly good justification for using the resistive approximation. The load current of our charge pump is proportional to the input audio signals if we consider the loudspeaker as an equivalent resistive load. However, the proposed PFM control is easy to extend to other DC–DC converter applications when a current sense circuit is available.

There is a potential problem with traditional PFM control that the switching frequency will enter into audio frequency range at the light load, which will introduce audio noise, especially in sensitive audio applications. The proposed PFM control with segmented power stage can reduce the transistor size according to the load current. It will lessen the skipping cycles and the switching frequency cannot drop too low to the audio frequency range. In our design, the lowest switching frequency of the charge pump operating at PFM mode is about 150 kHz when only supplying the quiescent current of the class AB amplifier, which is the actual load of the charge pump in the class G audio amplifier.

3. Function description and simulation results of charge pump

The simplified diagram of the proposed charge pump system is shown in Fig. 6. The charge pump has a feed-forward control path to select the different modes and power MOS sizes according to the amplitude of the input signal and the load current. As mentioned above, the load current can be predicted by the amplitude of the input audio signal when considering

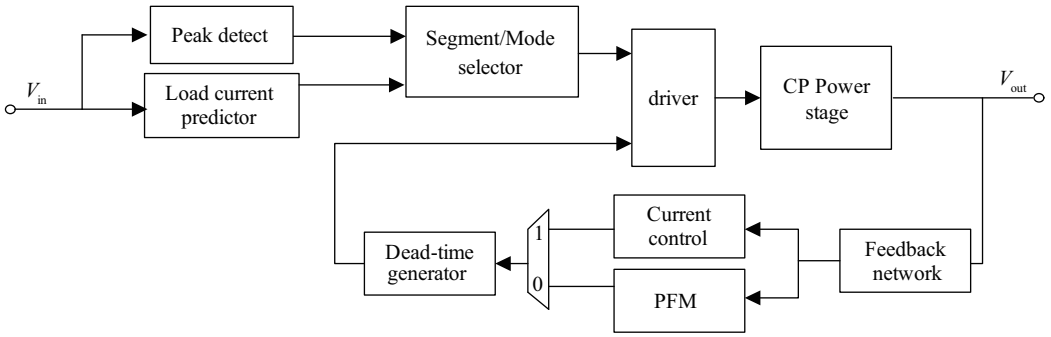


Fig. 6. Block diagram of the proposed charge pump system.

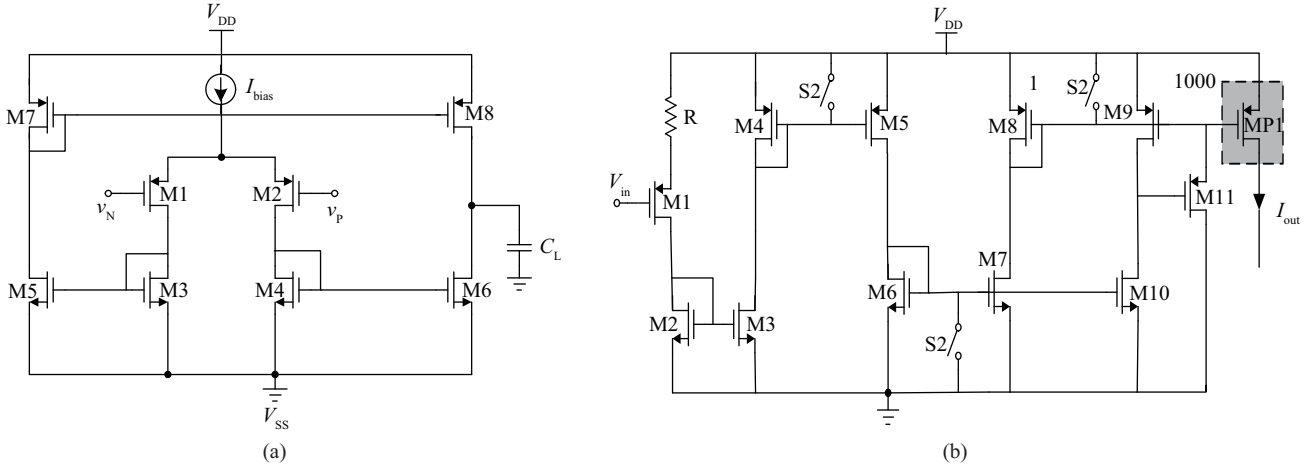


Fig. 7. (a) Schematic of error amplifier. (b) Schematic of V to I conversion.

the loudspeaker as an equivalent resistive load. There are two feedback control loops to regulate the output voltage. The PFM control is adopted when operating at 0.5x mode. Current mode control is realized when operating at 1x mode. The charge pump is shut off when it transits from 1x mode to 0.5x mode to reduce power dissipation. Under these conditions, the load capacitor discharges free to power the load.

The current mode control block has two parts: an error amplifier and a voltage to current converter. The output of the feedback divider inputs to the error amplifier. It is a normal current amplifier, as shown in Fig. 7(a). The motivation to choose this type of amplifier is that it has a relatively large dominant pole that makes the compensation of the whole system easier. The V to I conversion circuit is to convert the error signal to the corresponding current signal, which will regulate the output to the preset value. The circuit diagram is shown in Fig. 7(b). The transistor MP1 is the power transistor of the power stage. This circuit works normally only in the charge phase.

The diagram of PFM control is shown in Fig. 8(a). At each clock rising edge, the output of the feedback divider is compared with the reference voltage while the PFM control is enabled. When the output voltage is above the required value, all power transistors are shut off and the output capacitor discharges freely at this cycle. Otherwise, the power stage switches normally. The dead time generator is shown in Fig. 8(b). The gate drive signals CP and CN must not overlap or there will be large current spikes.

The current capability is simulated at different operation

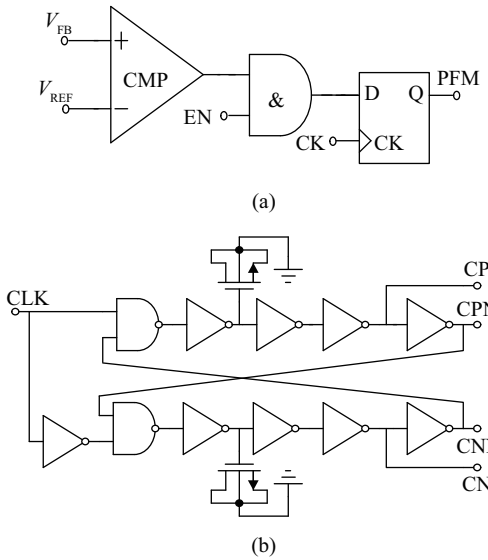


Fig. 8. (a) Diagram of PFM control. (b) Diagram of non-overlapping clock generation.

modes and the results are shown in Fig. 9. The bottom line is the load current waveform and the top line is the output voltage waveform. The output voltage ripple changes according to the threshold value of the segment and the mode transition.

The output voltage and ripple values at different load currents are summarized in Table 3.

The load regulation is simulated when input different mag-

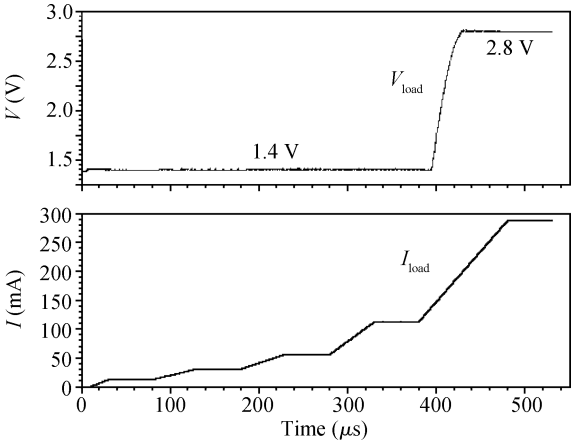


Fig. 9. Current capability simulated waveforms.

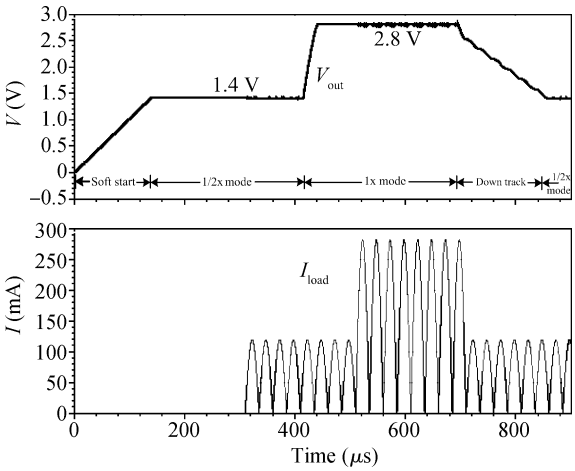


Fig. 10. Soft start and load regulation simulated waveforms.

Table 3. Output voltage and ripple at different load currents.

Load current (mA)	15	30	60	112.5	287.5
Conversion ratio	0.5x	0.5x	0.5x	0.5x	1x
DC output voltage (V)	1.4	1.4	1.4	1.399	2.794
Output ripple (mV)	2.9	5.2	10.3	12.6	16.4

nitudes sine wave. The simulation results are shown in Fig. 10. The lower line is the load current waveform and top line is the output voltage waveform. The voltage change is smaller than 11.7 mV at the current range of 1x mode and there is a small overshoot when the output reaches the pre-set value at 1x mode. When the charge pump transits from 1x mode to 0.5x mode, the charge pump is shut off and only the output capacitor provides the power to the load, which is shown as the down track phase in Fig. 10. The simulation bench is with the parasitic inductor, resistor of the pad and ESR of the load capacitor.

4. Experimental results

The proposed charge pump is implemented in a SMIC 0.18 μm 3.3 V CMOS process. The microphotograph of the die is shown in Fig. 11.

The operational waveforms of the charge pump in 0.5x mode are shown in Fig. 12(a). The test condition is to sink the

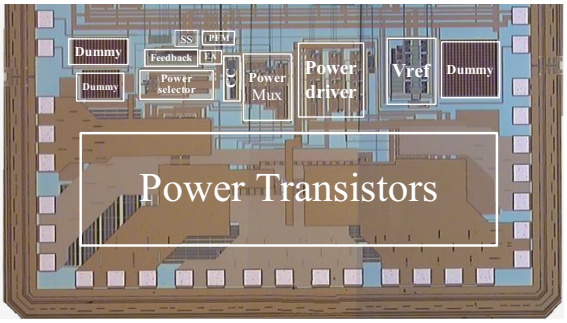
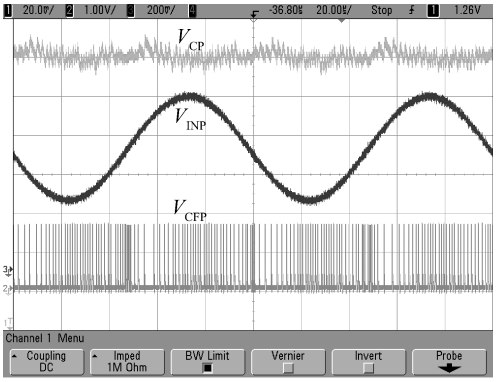
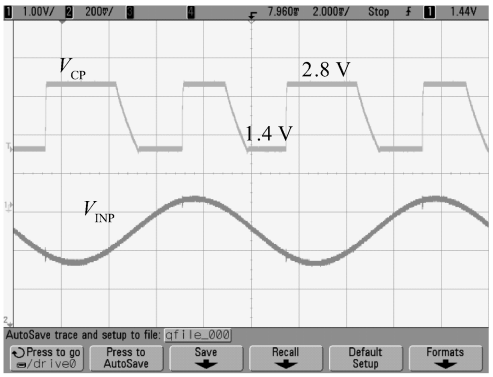


Fig. 11. Chip microphotograph.



(a)



(b)

Fig. 12. (a) Waveforms of V_{CP}, V_{OUT}, V_{CFP}. (b) Waveforms of V_{CP}, V_{INP}.

charge pump with a class AB amplifier and input a sine wave to change the power stage segment. The conduct cycles and ripple voltage are detected to determine the function of the proposed PFM control. V_{CP}, V_{INP} and V_{CFP} represent the output voltage of the charge pump, the input signal and the positive terminal voltage of the flying capacitor, respectively. Figure 12(b) shows the output voltage of the charge pump V_{CP} transits between 1.4 V and 2.8 V according to the amplitude of the input signal. The falling edge is slower due to the free discharge of the output capacitor.

Figure 13 shows the measured output ripple voltage comparison between the proposed PFM control with segment and the normal PFM control. From the measured results, the ripple of the proposed control is smaller than that of the normal PFM control, especially at light load. The ripple difference between the two PFM control methods becomes smaller when

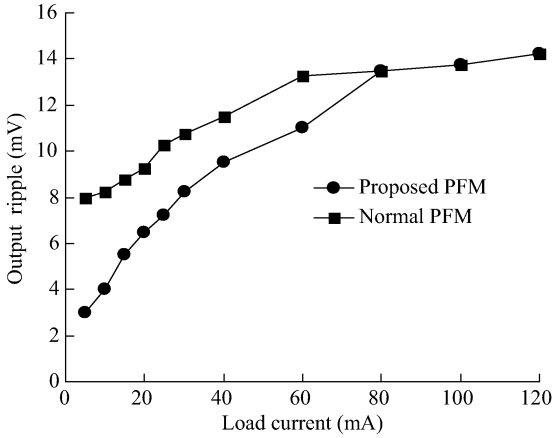


Fig. 13. Test output voltage ripple versus load current.

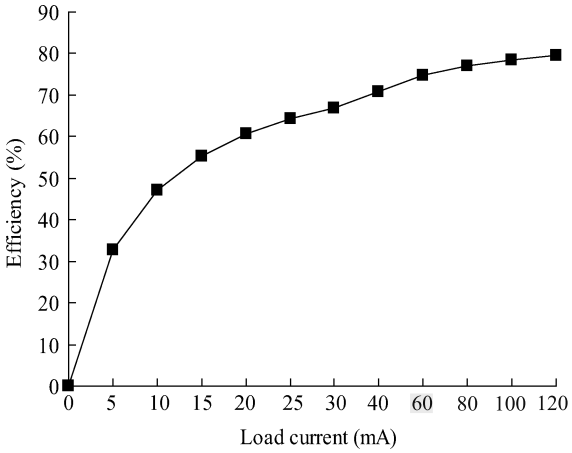


Fig. 14. Test efficiency versus load current @ 0.5x mode.

loading larger current. When the load current is larger than 60 mA, the same size power MOS transistors are required in the two control methods and there is equal output voltage ripple. The measured efficiencies in these two methods are almost the same except for a small control current difference.

The measured power efficiency of the charge pump at 0.5x mode and 1x mode are shown in Figs. 14 and 15, respectively. The efficiency is higher than 60% when the load current is larger than 20 mA. The ratio of switching and dynamic power loss over the output power will increase when the load current becomes smaller. As a result, the power efficiency degrades as the load current decreases.

Table 4 summarizes the performance characteristics of the proposed charge pump.

Figure 16 shows the class G amplifier (the proposed charge pump with a class AB amplifier as its load) efficiency versus output power when inputting a 1 kHz sine wave. The measured results display the classical non-monotonic behavior of class G: better than 30% efficiency is achieved at the output power range from 40 to 360 mW. The class G efficiency is twice that of the traditional class AB amplifier when the output power is smaller than 80 mW. The actual voice or music signal has a large PAR and its average power always concentrates at the low power range, which means that class G operation is preferred to actual audio signal amplification.

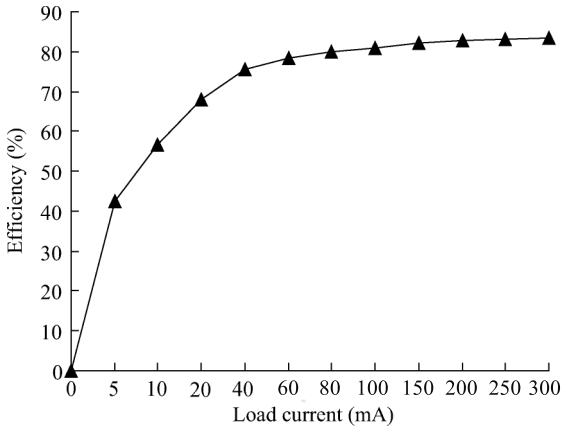


Fig. 15. Test efficiency versus load current @ 1x mode.

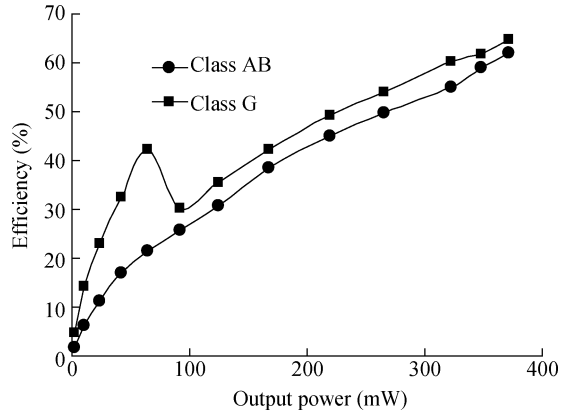


Fig. 16. Class G efficiency versus class AB.

Table 4. Performance summary of the proposed charge pump.

Parameter	Value	
Supply voltage (V)	3.3	
Process	0.18 μm, 3.3 V CMOS	
Output voltage (V)	1.4 @ 0.5x	2.8 @ 1x
Switching frequency (MHz)	0.15–2	2
Maximum output current (mA)	125	300
Output ripple voltage @ 10 μF (mV)	< 15	< 18
Load regulation (mV/mA)	0.4	0.3
Peak efficiency (%)	79.5	83.6
Chip area (mm^2)	1.08	

5. Conclusion

A dual mode regulated charge pump with two output voltage levels applied at a class G audio amplifier is presented in this paper. The proposed charge pump operates at PFM mode at 0.5x to improve the power efficiency. A novel PFM control with segmented power stage is introduced to reduce the output voltage ripple. The optimized power MOS size is selected according to enough current capacity and minimum area aim. The proposed PFM control is easy to extend to other DC–DC converter applications when a current sense circuit is available. The proposed charge pump is implemented in a 3.3-V 0.18-μm CMOS process. The test chip generates 1.4 V output with a supply up to 125 mA of the load current and 2.8 V output with a supply up to 300 mA of the load current. Its ripple is

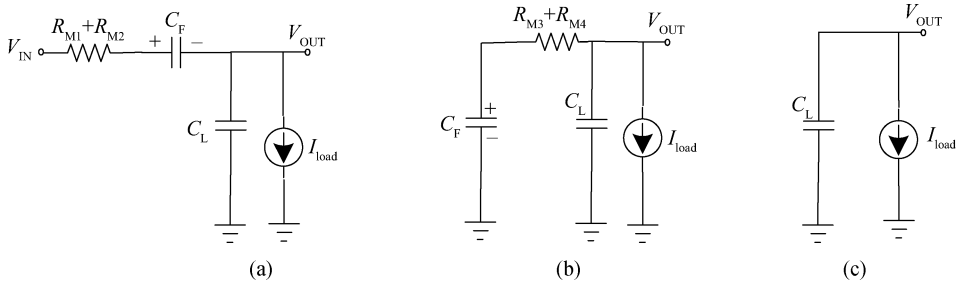


Fig. A1 (a) Equivalent circuit of phase A. (b) Equivalent circuit of phase B. (c) Equivalent circuit of phase C.

much smaller than that of traditional PFM control, especially at a light load. The peak power efficiency is 79.5% @ 0.5x mode and 83.6% @ 1x mode. The proposed charge pump is used as the adaptive power supply in the class G audio power amplifier. The measured efficiency of class G is about twice that of the traditional class AB amplifier at the low power range and is an obvious improvement even though at a higher output power range.

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Appendix A

A single operation cycle of a charge pump can be divided into three phases. The equivalent circuit is shown in Fig. A1.

Phase A (charging phase; M1 and M2 are on): C_F is charged from V_{IN}. The average voltage across C_F is the input voltage V_{IN} reduced by the voltage losses across the on-resistances R_{M1}, and R_{M2} of M1 and M2 and V_{OUT}.

$$V_{C_F} = V_{IN} - I_A(R_{M1} + R_{M2}) - V_{OUT}. \tag{A1}$$

Phase B (transfer phase; M3 and M4 are on): C_F is placed in parallel with C_L and discharged into the load capacitor C_{OUT}. The average voltage C_{OUT} is

$$V_{OUT} = V_{C_F} - I_B(R_{M3} + R_{M4}). \tag{A2}$$

Phase C (skipping phase; M1 ... M4 are off): no energy transfer from V_{IN} to C_F and C_{OUT}; V_{CF} = const. The load is supplied by C_{OUT}.

In steady state, the average voltage across C_F stays constant, which means that the charge on C_F keeps conservation when the charge pump operates steadily. Then the following equation must be satisfied,

$$|\Delta Q_{CF}|_{(\text{Phase A})} = |\Delta Q_{CF}|_{(\text{Phase B})}. \tag{A3}$$

Assuming that a 50% duty-cycle is applied to the charge pump, then the duration of phase A is equal to the duration of phase B, which is equal to $T/2$. Therefore the average charging current of C_F is equal to the average discharging current. Provided that the time constants in charging phase A and transfer phase B are big enough, this means

$$(R_{M1} + R_{M2})C_F \geqslant 10\left(\frac{T}{2}\right), \tag{A4}$$

and

$$(R_{M3} + R_{M4})C_F \geqslant 10\left(\frac{T}{2}\right). \tag{A5}$$

This is satisfied completely in the proposed charge pump when operating at 0.5x mode. Then

$$|I_A| = |I_B| = |I_P|. \tag{A6}$$

When the charge pump operates in a closed loop system, and the output voltage V_{OUT} has stabilized, the charge on the capacitors keeps constant and the whole charge that the pump delivers must be equal to the charge consumed by the load. Then the transfer current and load current satisfy the following equation,

$$I_P\frac{T}{2} + (I_P - I_{load})\frac{T}{2} = I_{load}(T + t_w), \tag{A7}$$

where t_w is the skipping time in phase C. Therefore the input current I_P during the transfer phase can be written as

$$I_P = I_{load}\left(1 + \frac{t_w}{T}\right). \tag{A8}$$

The average input current of the charge pump can be calculated as

$$I_{IN} = \frac{I_P T/2}{t_w + T} = \frac{I_{load}\left(1 + \frac{t_w}{T}\right)T/2}{t_w + T} = \frac{I_{load}}{2}. \tag{A9}$$

From Eqs. (A1), (A3), (A6) and (A8), the output voltage can be written as

$$V_{OUT} = \frac{1}{2}V_{IN} - \frac{1}{2}I_{load}\left(1 + \frac{t_w}{T}\right)\sum_{i=1}^{4} R_{Mi}. \tag{A10}$$

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